PHILIPS

Data handbook

PHILIPS Electronic components and materials

# Integrated circuits

Book IC01N 1985
New series

TDA TDA

TEA

## Radio, audio and associated systems

## Bipolar, MOS

NEW HANDBOOK SERIES

**Elcoma** – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

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# RADIO, AUDIO AND ASSOCIATED SYSTEMS
# BIPOLAR, MOS

# DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

| | |
|---|---|
| ELECTRON TUBES | BLUE |
| SEMICONDUCTORS | RED |
| INTEGRATED CIRCUITS | PURPLE |
| COMPONENTS AND MATERIALS | GREEN |

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

# ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

| | |
|---|---|
| T1 | **Tubes for r.f. heating** |
| T2a | **Transmitting tubes for communications, glass types** |
| T2b | **Transmitting tubes for communications, ceramic types** |
| T3 | **Klystrons** |
| T4 | **Magnetrons for microwave heating** |
| T5 | **Cathode-ray tubes**<br>Instrument tubes, monitor and display tubes, C.R. tubes for special applications |
| T6 | **Geiger-Müller tubes** |
| T7 | **Gas-filled tubes** (will not be reprinted) |
| T8 | **Picture tubes and components**<br>Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display |
| T9 | **Photo and electron multipliers** |
| T10 | **Plumbicon camera tubes and accessories** |
| T11 | **Microwave semiconductors and components** |
| T12 | **Vidicon and Newvicon camera tubes** |
| T13 | **Image intensifiers** |
| T14 | **Infrared detectors** |
| T15 | **Dry reed switches** |

Data collations on these subjects (T13–T15) are available now.
Data Handbooks will be published in 1985.

| | |
|---|---|
| T16 | **Monochrome tubes and deflection units**<br>Black and white TV picture tubes, monochrome data graphic display tubes, deflection units |

# SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

**S1 Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

**S2a Power diodes**

**S2b Thyristors and triacs**

**S3 Small-signal transistors**

**S4a Low-frequency power transistors and hybrid modules**

**S4b High-voltage and switching power transistors**

**S5 Field-effect transistors**

**S6 R.F. power transistors and modules**

**S7 Surface mounted semiconductors**

**S8 Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

**S9 Power MOS transistors**

**S10 Wideband transistors and wideband hybrid IC modules**

**S11 Microwave semiconductors** (to be published in this series in 1985)
At present available in Handbook T11

**S12 Surface acoustic wave devices**

# INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

| EXISTING SERIES | | Superseded by: |
|---|---|---|
| IC1 | **Bipolar ICs for radio and audio equipment** | IC01N |
| IC2 | **Bipolar ICs for video equipment** | IC02N |
| IC3 | **ICs for digital systems in radio, audio and video equipment** | IC01N and IC02N |
| IC4 | **Digital integrated circuits**<br>CMOS HE4000B family | |
| IC5 | **Digital integrated circuits — ECL**<br>ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs | IC08N |
| IC6 | **Professional analogue integrated circuits** | |
| IC7 | **Signetics bipolar memories** | |
| IC8 | **Signetics analogue circuits** | IC11N |
| IC9 | **Signetics TTL logic** | IC09N and IC15N |
| IC10 | **Signetics Integrated Fuse Logic (IFL)** | IC13N |
| IC11 | **Microprocessors, microcomputers and peripheral circuitry** | |

## NEW SERIES

| | | |
|---|---|---|
| IC01N | **Radio, audio and associated systems**<br>Bipolar, MOS | (published 1985) |
| IC02N | **Video and associated systems**<br>Bipolar, MOS | (published 1985) |
| IC03N | **Telephony equipment**<br>Bipolar, MOS | (published 1985) |
| IC04N | **HE4000B logic family**<br>CMOS | |
| IC05N | **HE4000B logic family uncased integrated circuits**<br>CMOS | (published 1984) |
| IC06N | **High-speed CMOS; PC54/74HC/HCT/HCU**<br>Logic family | (published 1985) |
| IC07N | **PC54/74HC/HCU/HCT uncased integrated circuits**<br>HCMOS | |
| IC08N | **10K and 100K logic family**<br>ECL | (published 1984) |
| IC09N | **Logic series**<br>TTL | (published 1984) |
| IC10N | **Memories**<br>MOS, TTL, ECL | |
| IC11N | **Linear LSI** | (published 1985) |
| IC12N | **Semi-custom gate arrays & cell libraries**<br>ISL, ECL, CMOS | |
| IC13N | **Semi-custom**<br>Integrated Fuse Logic | (published 1985) |
| IC14N | **Microprocessors, microcontrollers & peripherals**<br>Bipolar, MOS | |
| IC15N | **Logic series**<br>FAST TTL | (published 1984) |

**Note**

Books available in the new series are shown with their date of publication.

# COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

| | |
|---|---|
| **C1** | **Programmable controller modules**<br>PLC modules, PC20 modules |
| **C2** | **Television tuners, coaxial aerial input assemblies, surface acoustic wave filters** |
| **C3** | **Loudspeakers** |
| **C4** | **Ferroxcube potcores, square cores and cross cores** |
| **C5** | **Ferroxcube for power, audio/video and accelerators** |
| **C6** | **Synchronous motors and gearboxes** |
| **C7** | **Variable capacitors** |
| **C8** | **Variable mains transformers** |
| **C9** | **Piezoelectric quartz devices** |
| **C10** | **Connectors** |
| **C11** | **Non-linear resistors**<br>Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC) |
| **C12** | **Potentiometers, encoders and switches** |
| **C13** | **Fixed resistors** |
| **C14** | **Electrolytic and solid capacitors** |
| **C15** | **Ceramic capacitors** |
| **C16** | **Permanent magnet materials** |
| **C17** | **Stepping motors and associated electronics** |
| **C18** | **Direct current motors** |
| **C19** | **Piezoelectric ceramics** |
| **C20** | **Wire-wound components for TVs and monitors** |
| **C21** | **Assemblies for industrial use**<br>HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices |
| **C22** | **Film capacitors** |

# INTRODUCTION

This new edition of the data handbook for radio, audio and associated systems has been expanded to include MOS as well as bipolar integrated circuits as the use of MOS circuits in radio and audio equipment is becoming more and more widespread (remote control, digital tuning, etc.).

This volume contains an index, associated information and package outlines.

The data handbook now includes dedicated radio, audio circuits and general purpose products (microcontrollers, display circuits, etc.) that find application in these systems. Full specifications are provided for the dedicated circuits; in some cases the general purpose circuits have short-form specifications. More detailed information can be found in the relevant data sheets and handbooks.

**$I^2C$ bus compatible ICs**

Some of the ICs in this handbook are $I^2C$ bus compatible (indicated by the logo shown below). The following clause applies:

Purchase of Philips' $I^2C$ components conveys a license under the Philips' $I^2C$ patent to use the components in the $I^2C$ system provided the system conforms to the $I^2C$ specifications defined by Philips.

# FUNCTIONAL AND NUMERICAL INDEX

# SELECTION GUIDE BY FUNCTION

| type number | description | page |
|---|---|---|
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| TDA1072A | AM receiver circuit | 421 |
| TEA5550 | AM car radio receiver circuit | 681 |
| TEA5570 | RF/IF circuit for AM/FM radio | 705 |
| **FM channels** | | |
| TCA420A | FM/IF combination | 245 |
| TDA1574 | integrated FM tuner for radio circuits | 539 |
| TDA1576 | FM/IF amplifier | 547 |
| TDA7000 | FM radio circuit; $f_i$ = 70 kHz; $V_o$ = 75 mV; DIL-18 | 609 |
| TDA7010T | FM radio circuit; $f_i$ = 70 kHz; $V_o$ = 75 mV; SO-16 | 617 |
| TDA7020T | FM stereo/mono radio circuit; $f_i$ = 76 kHz; $V_o$ = 90 mV | 625 |
| TEA5560 | FM/IF system | 693 |
| TEA5570 | RF/IF circuit for AM/FM radio | 705 |
| TEA6000 | FM/IF system and $\mu$C-based tuning interface; $I^2C$ bus compatible | 723 |
| **AM/FM combined channels** | | |
| TEA5570 | RF/IF circuit for AM/FM radio | 705 |
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| TEA5580 | PLL stereo decoder | 719 |
| **Interference suppressors** | | |
| TDA1001B; BT | interference and noise suppression circuit for FM receivers | 287 |

* Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Fransisco, California (U.S.A.).

* Compact Disc digital audio system.

# NUMERICAL INDEX

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| HEF4751VT | universal divider | SO-28; SOT-136A | 29 |
| MAB8400B | single-chip 8-bit $\mu$C; 128 RAM bytes | 28/28 "Piggy back" | 31 |
| MAB8400WP | single-chip 8-bit $\mu$C; 128 RAM bytes | 68-PLCC; SOT-188A | 31 |
| MAB8401B | like MAB8400 but with 8-bit LED driver | 28/28 "Piggy back" | 31 |
| MAB8401WP | like MAB8400 but with 8-bit LED-driver | 68-PLCC; SOT-188A | 31 |
| MAB8411P | single-chip 8-bit $\mu$C; 1K ROM/64 RAM bytes | SOT-117A | 31 |
| MAB8411T | single-chip 8-bit $\mu$C; 1K ROM/64 RAM bytes | SO-28; SOT-136A | 31 |
| MAB8421P | single-chip 8-bit $\mu$C; 2K ROM/64 RAM bytes plus 8-bit LED driver | SOT-117A | 31 |
| MAB8421T | single-chip 8-bit $\mu$C; 2K ROM/64 RAM bytes plus 8-bit LED driver | SO-28; SOT-136A | 31 |
| MAB8422P | single-chip 8-bit $\mu$C; 2K ROM/64 RAM bytes | SOT-146 | 33 |
| MAB8441P | single-chip 8-bit $\mu$C; 4K ROM/128 RAM bytes plus 8-bit LED driver | SOT-117A | 31 |
| MAB8441T | single-chip 8-bit $\mu$C; 4K ROM/128 RAM bytes plus 8-bit LED driver | SO-28; SOT-136A | 31 |
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| MAF8441P | single-chip 8-bit $\mu$C; 4K ROM/128 RAM bytes plus 8-bit LED driver; extended temperature | SOT-117A | 31 |
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| MAF84A42P | single-chip 8-bit $\mu$C; 4K ROM/128 RAM bytes; reduced frequency; extended temperature | SOT-146 | 33 |
| MAF8461P | single-chip 8-bit $\mu$C; 6K ROM/128 RAM bytes plus 8-bit LED driver; extended temperature | SOT-117A | 31 |

$\mu$C = microcontroller

* The package outline is included in the device data sheet.

* The package outline is included in the device data sheet.

** Compact Disc digital audio system.

* The package outline is included in the device data sheet.

* Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Fransisco, California (U.S.A.).

# GENERAL

**Type designation**
**Rating systems**
**Handling MOS devices**

# PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

*THREE LETTERS FOLLOWED BY A SERIAL NUMBER*

**FIRST AND SECOND LETTER**

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

**Notes**

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

**THIRD LETTER**

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

**SERIAL NUMBER**

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

*A VERSION LETTER*

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

*FIRST LETTER*: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

*SECOND LETTER*: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

# RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

## DEFINITIONS OF TERMS USED

*Electronic device.* An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

*Characteristic.* A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

*Bogey electronic device.* An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

*Rating.* A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

*Rating system.* The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

## ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

## DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

## DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

## HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

*Caution*

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

### Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

### Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

### Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

### Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

### Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

### Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

### Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

# DEVICE DATA

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# FREQUENCY SYNTHESIZER

The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers, e.g. in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- High-performance phase comparator — low phase noise — low spurii.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
  frequency offsets
  ROM compatible
  fractional channel capability.
- Programme range 6½ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

## APPLICATION INFORMATION

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and navaids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

## SUPPLY VOLTAGE

| rating | recommended operating |
|---|---|
| –0,5 to + 15 | 9,5 to 10,5 V |

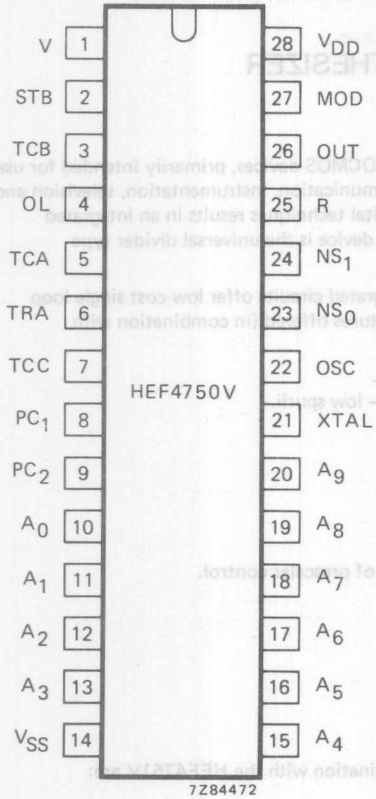



Fig. 1 Pinning diagram.

HEF4750VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).

PINNING

| | |
|---|---|
| R | phase comparator input, reference |
| V | phase comparator input |
| STB | strobe input |
| TCA | timing capacitor $C_A$ pin |
| TCB | timing capacitor $C_B$ pin |
| TCC | timing capacitor $C_C$ pin |
| TRA | biasing pin (resistor $R_A$) |
| $PC_1$ | analogue phase comparator output |
| $PC_2$ | digital phase comparator output |
| MOD | phase modulation input |
| OL | out-of-lock indication |
| OSC | reference oscillator/buffer input |
| XTAL | reference oscillator/buffer output |
| $A_0$ to $A_9$ | programming inputs/programmable divider |
| $NS_0$, $NS_1$ | programming inputs, prescaler |
| OUT | reference divider output |

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# UNIVERSAL DIVIDER

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷ 10/11 prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leqslant M \leqslant 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format.
To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.
The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D.
The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

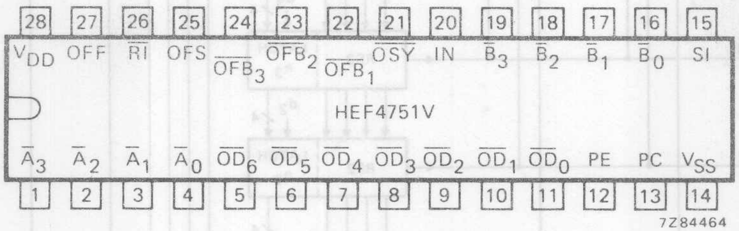



Fig. 1 Pinning diagram.

HEF4751VP : 28-lead DIL; plastic (SOT-117).
HEF4751VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).
HEF4751VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

SUPPLY VOLTAGE

| rating | recommended operating |
|---|---|
| −0,5 to +18 | 4,5 to 12,5 V |

FAMILY DATA
$I_{DD}$ LIMITS category LSI
} see Family Specifications

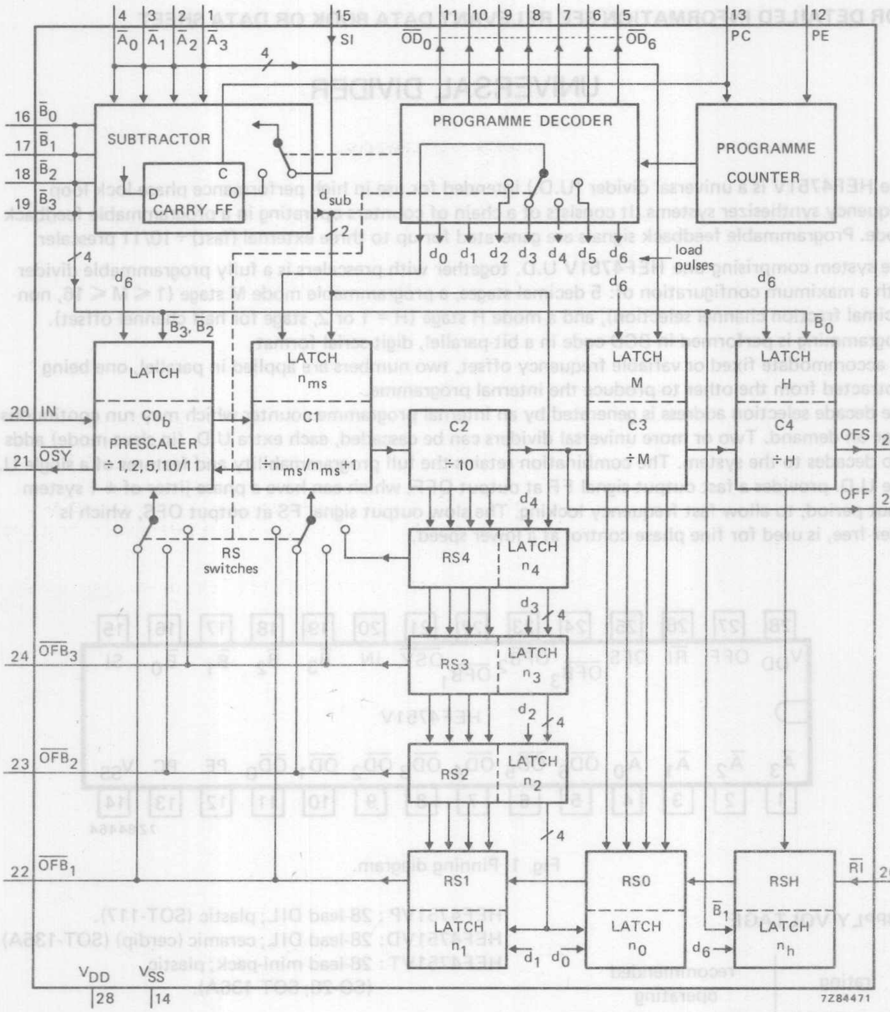



Fig. 2 Block diagram.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# SINGLE-CHIP 8-BIT MICROCONTROLLER

## DESCRIPTION

The MAB84XX family of microcontrollers is fabricated in NMOS. The family consists of 8 devices:

- MAB8400 – 128 RAM bytes, external program memory
- MAB8401 – like 8400 but with 8-bit LED-driver (10 mA), emulation of MAB/F8422/42* possible
- MAB/F8411 – 1K ROM/ 64 RAM bytes
- MAB/F8421 – 2K ROM/ 64 RAM bytes plus 8-bit LED-driver
- MAB/F8441 – 4K ROM/128 RAM bytes plus 8-bit LED-driver
- MAB/F8461 – 6K ROM/128 RAM bytes plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "Users manual Single-chip microcomputers" (supplied upon request).

* See data sheet on MAB/F8422/42.

### Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

| | | |
|---|---|---|
| | 0 to + 70 °C | MAB84XX family |
| | −40 to + 85 °C | MAF84XX family |
| | −40 to + 110 °C | MAF84AXX family |

## PACKAGE OUTLINES

MAB8400/01B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top)
MAB8400/01WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT-188A)
MAB/F8411/21/41/61P: 28-lead DIL; plastic (SOT-117D)
MAB8411/21/41T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

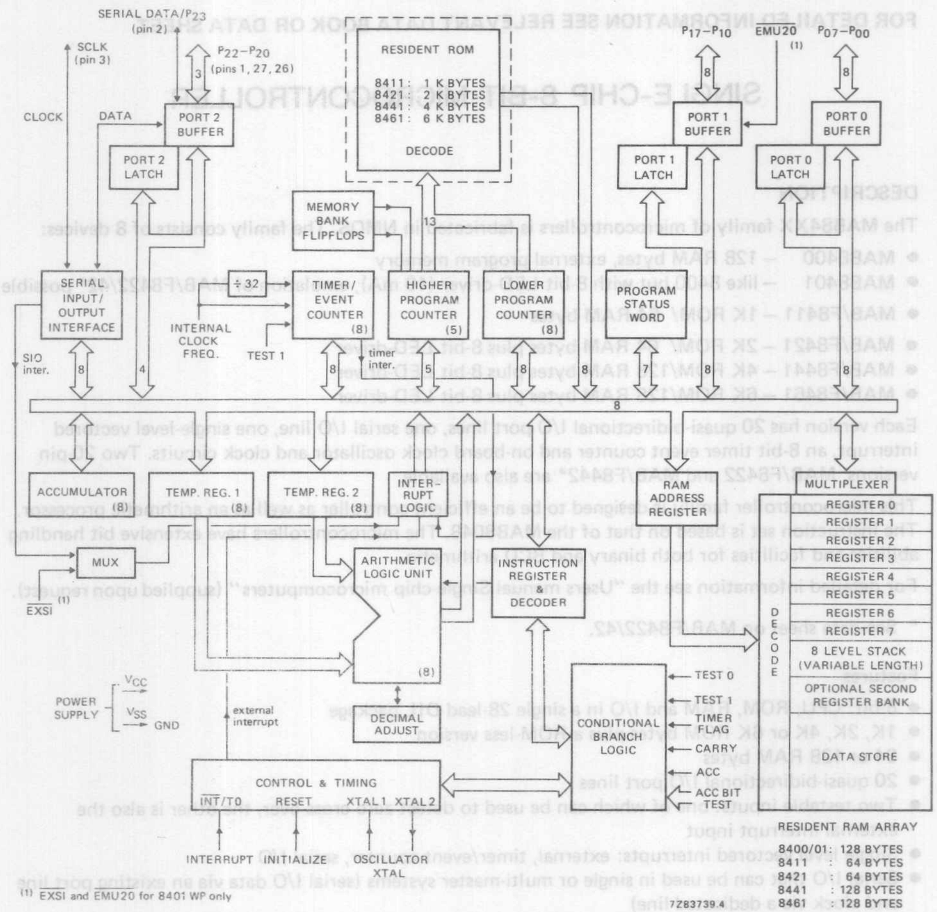
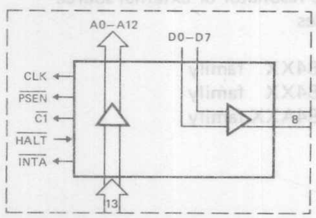



Fig. 4(a) Block diagram of the MAB84XX family.



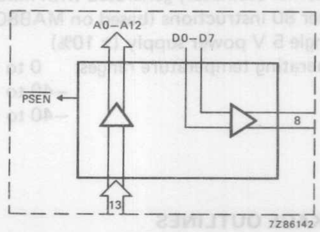




Fig. 4(b) Replacement for dotted part in Fig. 4(a) for the MAB8401WP bond-out version.

Fig. 4(c) Replacement of dotted part in Fig. 4(a) for the MAB8400B/01B 'Piggy-back' version.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# SINGLE-CHIP 8-BIT MICROCONTROLLER

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8420/8440 microcontrollers. The versions are:

- MAB8422 - 2K ROM/64 RAM bytes
- MAB8442 - 4K ROM/128 RAM bytes

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P10 and P11 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P20-P22) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is $I^2C$ compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for $I^2C$-bus control is available on request.

**Features**

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K ROM/64 RAM bytes
- MAB8442: 4K ROM/128 RAM bytes
- 13 quasi-bidirectional I/O port lines
- Two testable inputs $\overline{INT}$/T0 and T1
- High current output on P0 ($I_{OL}$ = 10 mA at $V_{OL}$ = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- $I^2C$-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P10 and P11 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single 5 V power supply
- 0 to 70 °C operating temperature range, also versions for −40 to 85 °C and −40 to 110 °C

**PACKAGE OUTLINES**

MAB/F8422/42P: 20-lead DIL; plastic (SOT-146).
MAF84A22/A42P: 20-lead DIL; plastic (SOT-146).

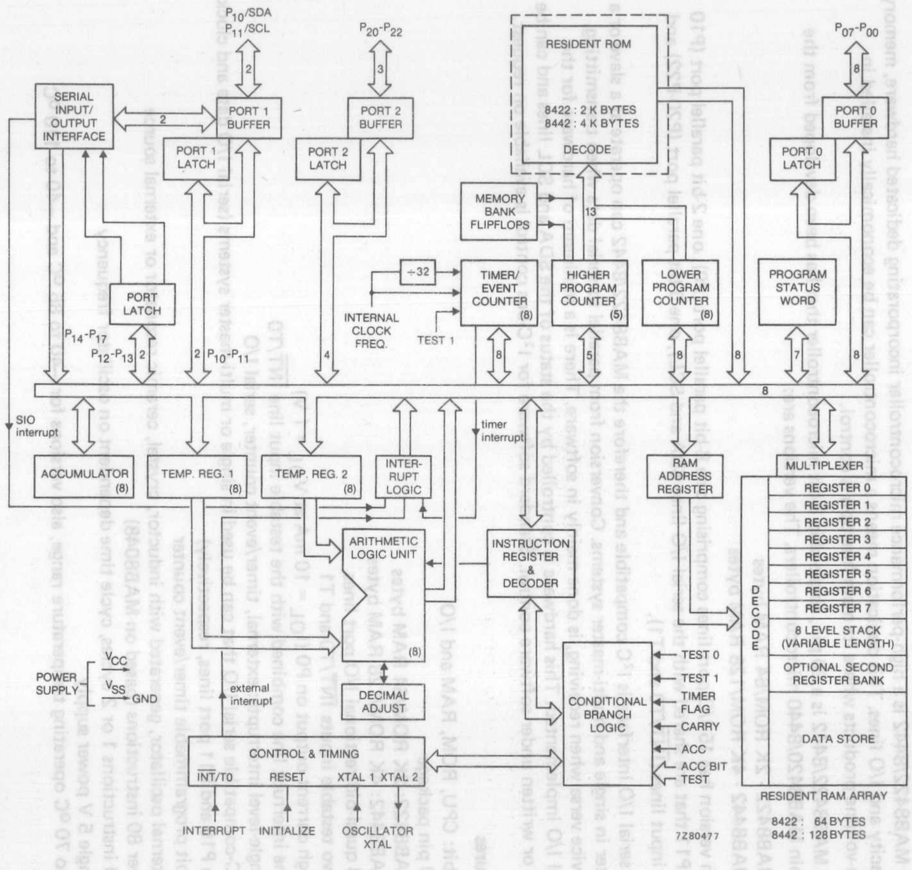



Fig. 1 Block diagram of the MAB8422/8442.

# VOICE SYNTHESIZER

## GENERAL DESCRIPTION

The MEA8000 is a 24-pin N-MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.

### Features

- Interfaces easily with most popular microprocessors and microcomputer
- 8-bit wide data bus
- 32-bit wide data buffer holding speech frame codes
- Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths
- Programmable amplitudes
- Programmable duration of each frame; 8, 16, 32 or 64 ms
- Synthesis occupies less than 1% of control processor time
- Capable of sophisticated unvoiced sound generation
- Crystal controlled oscillator or external (TTL) clock
- Minimal external audio filter requirement
- Single + 5 V power supply

## QUICK REFERENCE DATA

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply voltage | pin 13 | $V_{DD}$ | 4,5 | 5,0 | 5,5 | V |
| Supply current | no audio load | $I_{DD}$ | – | 30 | 50 | mA |
| **Inputs** | | | | | | |
| Input voltage | HIGH | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage | LOW | $V_{IL}$ | –0,5 | – | 0,8 | V |
| Input capacitance | | $C_I$ | – | – | 7 | pF |
| **Outputs** | | | | | | |
| Output voltage | $-I_{OH}$ = 100 $\mu$A | $V_{OH}$ | 2,4 | – | – | V |
| Output voltage | $I_{OL}$ = 1,6 mA | $V_{OL}$ | – | – | 0,4 | V |
| Capacitance | | $C_L$ | – | – | 30 | pF |
| Operating ambient temperature range | | $T_{amb}$ | 0 | – | + 70 | °C |

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

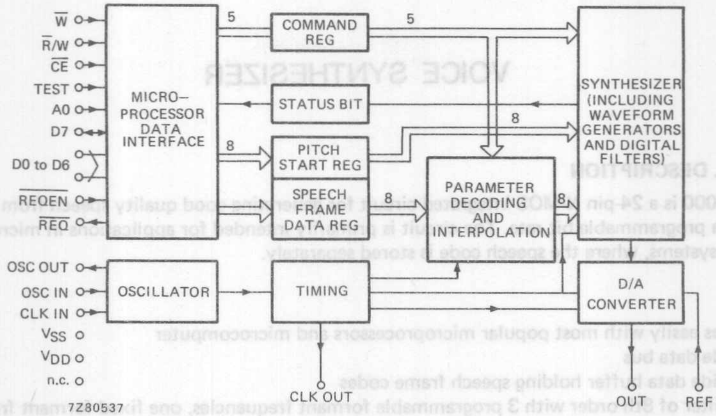



Fig. 1 Block diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{SS}$ | ground |
| 2 | $\overline{REQ}$ | data request |
| 3 | D7 | data bus |
| 4 | D6 | |
| 5 | D5 | |
| 6 | D4 | |
| 7 | D3 | |
| 8 | D2 | |
| 9 | D1 | |
| 10 | D0 | |
| 11 | A0 | data/control input |
| 12 | $\overline{CE}$ | chip enable |
| 13 | $V_{DD}$ | supply voltage |
| 14 | $\overline{REQEN}$ | request enable input |
| 15 | N.C. | not connected |
| 16 | OSC IN | internal oscillator |
| 17 | OSC OUT | |
| 18 | CLK IN | clock input |
| 19 | REF | reference current |
| 20 | OUT | speech output |
| 21 | CLK OUT | internal clock output |
| 22 | $\overline{R}$/W | read/write |
| 23 | $\overline{W}$ | write |
| 24 | TEST | test use only |

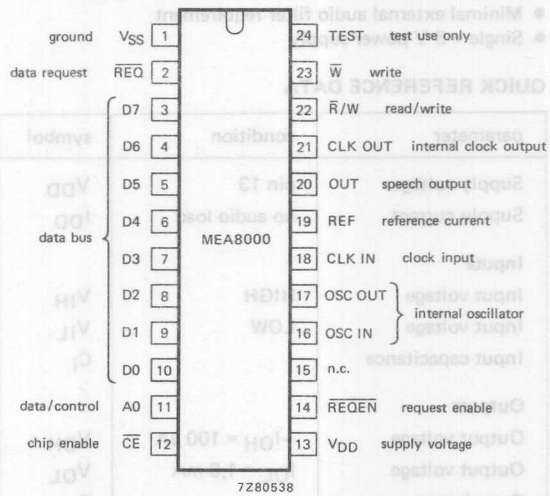



Fig. 2 Pinning diagram.

## FUNCTIONAL DESCRIPTION (pin number)

### Control

| | | |
|---|---|---|
| D0 to D7 | (10 to 3) | Data bus to which command or speech can be written. |
| D7 | (3) | Data port via which the status can be read. |
| $\overline{CE}$ | (12) | Chip enable (chip select). |
| $\overline{W}$ | (23) | Write. |
| $\overline{R}$/W | (22) | Read/Write<br>The control signals $\overline{W}$ and $\overline{R}$/W allow connections to most microcomputers or microprocessors (see timing diagrams). |
| A0 | (11) | Data/control input: discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation. |
| $\overline{REQ}$ | (2) | Data request (open drain output); output signal which follows inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external $\overline{REQEN}$ pin. |
| $\overline{REQEN}$ | (14) | Request enable input; $\overline{REQEN}$ = '0' enables the status REQ output, independent of the status of the command register. |

### Timing

| | | |
|---|---|---|
| OSC IN | (16) | Connections for internal clock oscillator; nominal crystal frequency 4 MHz. |
| OSC OUT | (17) | |
| CLK IN | (18) | Clock input for external clock, TTL compatible, 4 MHz. |
| CLK OUT | (21) | A buffered output for the internal clock cycle (which is equal to CLK divided by 3). May be used as a clock, for a microprocessor, for example. |

### Output

| | | |
|---|---|---|
| REF | (19) | Input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply. |
| OUT | (20) | Speech output; this output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3 V. |

### Supply

| | | |
|---|---|---|
| $V_{DD}$ | (13) | Single supply voltage, nominally 5 V, but battery operation is possible. |
| $V_{SS}$ | (1) | Ground. |
| TEST | (24) | Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation. |
| NC | (15) | It is recommended to ground this pin. |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| parameter | conditions | symbol | min. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage range | | $V_{DD}$ | –0,5 | + 7 | V |
| Voltage with respect to $V_{SS}$ | on any pin | $V_I$ | –0,5 | + 7 | V |
| Output voltage | pins 2 and 20 | $V_{REQ}$, $V_{OUT}$ | | 15 | V |
| Storage temperature range | | $T_{stg}$ | –20 | + 125 | °C |
| Operating ambient temperature range | | $T_{amb}$ | 0 | + 70 | °C |

## CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_{DD}$ = 5 V, unless otherwise specified; all voltages referenced to $V_{SS}$

| parameter | conditions | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Symbol** | | | | | | |
| Supply voltage | note 1 | $V_{DD}$ | 4,5 | 5,0 | 5,5 | V |
| Supply current | no audio load | $I_{DD}$ | – | 30 | 50 | mA |
| **Inputs** | | | | | | |
| **D0 to D7, A0, $\overline{CE}$, $\overline{W}$, R/$\overline{W}$, $\overline{REQEN}$, CLK IN** | | | | | | |
| Input voltage HIGH | | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage LOW | | $V_{IL}$ | –0,5 | – | 0,8 | V |
| Input leakage current | note 2 | $I_{IR}$ | – | – | 10 | μA |
| Input capacitance | | $C_I$ | – | – | 7 | pF |
| **Outputs** | | | | | | |
| **D7 (I/O), CLK OUT** | | | | | | |
| Output voltage HIGH | $-I_{OH}$ = 100 μA | $V_{OH}$ | 2,4 | – | – | V |
| Output voltage LOW | $I_{OL}$ = 1,6 mA | $V_{OL}$ | – | – | 0,4 | V |
| Output load capacitance | | $C_L$ | – | – | 50 | pF |
| **$\overline{REQ}$** | | | | | | |
| Output voltage HIGH | open drain | $V_{OH}$ | – | – | 13,2 | V |
| Output voltage LOW | $I_{OL}$ = 1,6 mA | $V_{OL}$ | – | – | 0,4 | V |
| Output load capacitance | | $C_L$ | – | – | 50 | pF |
| **Audio output** | | | | | | |
| Reference current | pin 19; note 8 | $I_{REF}$ | – | – | 0,3 | mA |
| Output current | pin 20; peak value | | | | | |
| | $I_{REF}$ = 0 mA | $I_{OUT}$ | – | 100 | – | μA |
| | $I_{REF}$ = 0,1 mA | $I_{OUT}$ | – | 1,7 | – | mA |
| | $I_{REF}$ = 0,3 mA | $I_{OUT}$ | – | 5 | – | mA |
| Output voltage | pin 20; for linear operation; note 3; $I_{REF}$ = 0,1 mA | $V_{OUT}$ | 2,5 | – | 13,2 | V |
| **Oscillator** | | | | | | |
| Crystal frequency | internal | $f_{XTAL}$ | – | | 4,00 | MHz |
| Clock frequency | external | $f_{CLK}$ | – | | 4,00 | MHz |

## TIMING CHARACTERISTICS (note 4) (Figs 6 and 7)

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Write enable | | $t_{WR}$ | 200 | – | – | ns |
| Address set-up | | $t_{AS}$ | 30 | – | – | ns |
| Address hold | | $t_{AH}$ | 30 | – | – | ns |
| Data set-up for write | | $t_{DS}$ | 150 | – | – | ns |
| Data hold for write | | $t_{DH}$ | 30 | – | – | ns |
| Request hold | note 5 | $t_{RH}$ | – | – | 350 | ns |
| Request next | note 6 | $t_{RN}$ | – | – | 3 | μs |
| | clock frequency = 3,84 MHz | | | | | |
| Read enable | | $t_{RD}$ | 200 | – | – | ns |
| Data delay for read | note 7 | $t_{DD}$ | – | – | 150 | ns |
| Data floating for read | note 7 | $t_{DF}$ | – | – | 150 | ns |
| Request valid before write | | $t_{RV}$ | 0 | – | – | ns |
| Request output enable response | | $t_{ROE}$ | – | – | 750 | ns |
| Control set-up | | $t_{CS}$ | – | – | 20 | ns |
| Control hold | | $t_{CH}$ | – | – | 20 | ns |

### Notes

1. The circuit will continue to operate from a supply of up to 6,5 V, but without necessarily meeting the specification.
2. This is also valid for $V_{DD}$ = 0 V.
3. This permits the connection of the output load to a supply higher than that supplying the synthesizer.
4. Timing reference level is 1,5 V.
5. An external pull-up resistor is required, as this is an open drain output. The time ($t_{RH}$) to reach 2,0 V is specified at a load to 5 V of 3,3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2,0 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2,5 V.

## OPERATION PRINCIPLE

The MEA8000 has been designed for a vocal tract modelling technique of voice synthesis. This method gives the lowest possible bit rate for speech quality which is acceptable for most industrial applications.

Figure 3 shows a simplified electronic model of the human vocal tract as a formant synthesizer. A combination of a periodic signal, representing the pitch of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech. Both these signals are fed to a variable filter comprising four resonantors (via an amplifier which controls the amplitude of the synthesized sound). The resonators model the sound in accordance with the formats in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth.

The information required to control the synthesizer is:

- pitch
- amplitude — excitation source (vocal cords)
- voice/unvoiced source selector
- filter control — spectrum shaping (vocal tract)

A good replica of the original speech is obtained by periodic updating of this control information.

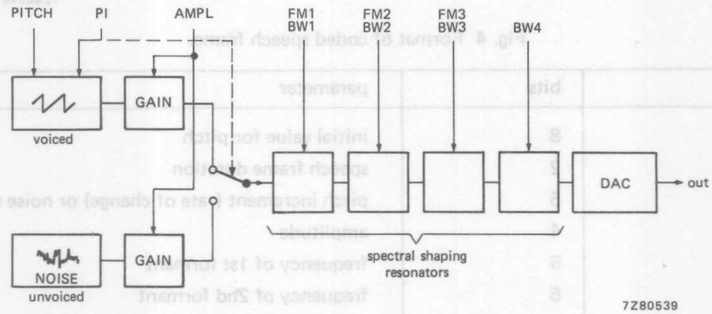



Fig. 3 Electronic model of human vocal tract.

## OPERATION

Speech is generated by suitable filtering of a relatively low frequency sawtooth waveform for voiced sounds, or of random noise for unvoiced sounds. New parameters for both the digital waveform generator and the digital filter are supplied to the synthesizer in coded groups of 4 bytes via the data bus. The code group also contains the duration of the next speech frame to be produced (8, 16, 32 or 64 ms).

The output sample rate is 64 kHz or 8 times the internal sample rate with linear interpolation in between. This greatly reduces the need for an external analogue output filter.

### Modes of operation

1. STOP mode: characterised by a silent output and the status REQ bit set to '1'. This mode is entered from power up or by STOP command. The mode is entered automatically if at the end of an active speech frame the next four parameter bytes are not yet received while the CONT bit in the command register is a '0'. In the latter case the final speech frame will be repeated once but with a decaying amplitude and the same pitch.
2. ACTIVE mode: a speech sample is being produced.
3. CONTINUOUS mode: entered if an active speech frame is finished and new data is not supplied in time while the CONT bit in the command register is a '1'. The synthesizer will repeat the last speech frame indefinitely until all four new data bytes are received, or a STOP command, or a reset of the CONT bit.

### Speech code input buffer

Speech code is written to the synthesizer when $\overline{CE}$ and $\overline{W}$ are both '0', while $\overline{R}$/W = '1' and A0 = '0'. Also the status $\overline{REQ}$ bit must read a '1', otherwise the synthesizer is still busy and will not react to a data write operation.
Starting from the STOP mode, the first data will be interpreted as a starting value for the PITCH. Thereafter every four successive data bytes are treated as a group of speech code. The coded speech frame format is shown in Fig. 4.

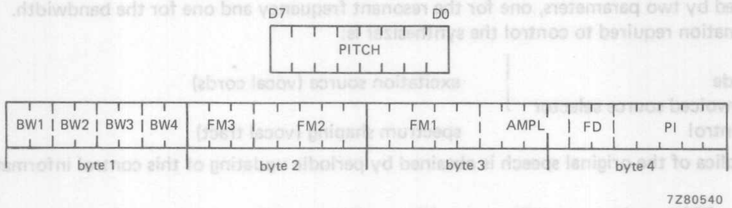



Fig. 4 Format of coded speech frame.

| code | bits | parameter |
|---|---|---|
| PITCH | 8 | initial value for pitch |
| FD | 2 | speech frame duration |
| PI | 5 | pitch increment (rate of change) or noise selection |
| AMPL | 4 | amplitude |
| FM1 | 5 | frequency of 1st formant |
| FM2 | 5 | frequency of 2nd formant |
| FM3 | 3 | frequency of 3rd formant |
| FM4 | 0 | frequency of 4th formant (fixed) |
| BW1 | 2 | bandwidth of 1st formant |
| BW2 | 2 | bandwidth of 2nd formant |
| BW3 | 2 | bandwidth of 3rd formant |
| BW4 | 2 | bandwidth of 4th formant |

During each data write operation, the status REQ bit will be cleared to '0'.
It appears within a few microseconds, requesting the next byte of the group.
The request for the first byte of the next group always appears shortly after the beginning of the current speech frame, and all four bytes must be provided before it finishes. This leaves the control circuit (i.e. microprocessor) enough time to use polling, instead of interrupts, as the minimum time of a speech is 8 ms.
When in the STOP mode the synthesizer will commence producing sound after receipt of 1 + 4 bytes.

### Status bit

The status bit is accessed at $\overline{CE}$ = $\overline{R}$/W = '0'.
The status of $\overline{W}$ and A0 are arbitrary.
Pin D7 reveals the request for a (next) speech code byte: '0' = busy, '1' = request for data.

### Command register

A command is written to the synthesizer at $\overline{CE}$ = $\overline{W}$ = '0' while A0 = $\overline{R}$/W = '1'.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| | | | STOP | CONT enable | CONT | ROE enable | ROE |
| NOT USED | | | '0' = INVALID<br>'1' = STOP | 00 = INVALID<br>01 = INVALID<br>10 = SLOW STOP<br>11 = CONTINUE | | 00 = INVALID<br>01 = INVALID<br>10 = DISABLE $\overline{REQ}$ OUTPUT<br>11 = ENABLE $\overline{REQ}$ OUTPUT | |

STOP — Stop mode. This results in an immediate reset of the synthesizer to the STOP mode. The ROE and CONT are not affected by this command.

CONT — Continuous mode. This bit can be set or cleared only if the corresponding CONT enable bit is programmed as a '1'. In the continuous mode the synthesizer will not revert to the STOP mode if all four parameters are not received before the end of the current speech frame, but repeat it indefinitely.

If CONT = '1' the last frame will be repeated once with decaying amplitude and the same pitch before the stop mode is entered.

ROE — Request Output Enable. This can be set or cleared only if the corresponding ROE enable bit is a '1'. ROE determines whether the request in the status bit appears on the $\overline{REQ}$ pin.

Note: the same can be achieved by connecting the $\overline{REQEN}$ pin (request enable) to a '0'.

After power on, the command register bits CONT and ROE will both be zero. Thus power on equals the command 00011010 = 1 A (hexadecimal).

### Control signals

With the three control signals $\overline{CE}$, $\overline{W}$ and $\overline{R}$/W the synthesizer is made compatible with most microprocessors and microcomputers.

| $\overline{CR}$ | $\overline{W}$ | $\overline{R}$/W | A0 | | Operation |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | | WRITE DATA |
| 0 | 0 | 1 | 1 | | WRITE COMMAND |
| 0 | X | 0 | X | | READ STATUS |
| 0 | 1 | 1 | X | | 3-STATE DATA BUS |
| 1 | X | X | X | | 3-STATE DATA BUS |

### Power supply

During (slow) power up or power down the circuit will not produce any spurious sound. As soon as the supply is high enough for reliable operation, the circuit will be in the STOP mode with ROE = CONT = '0'.

### Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance, with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the $\overline{RD}$ and $\overline{WR}$ strobe inputs.

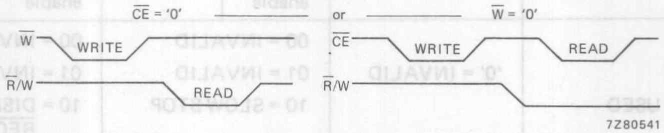



Fig. 5 Typical waveforms of the control signals.

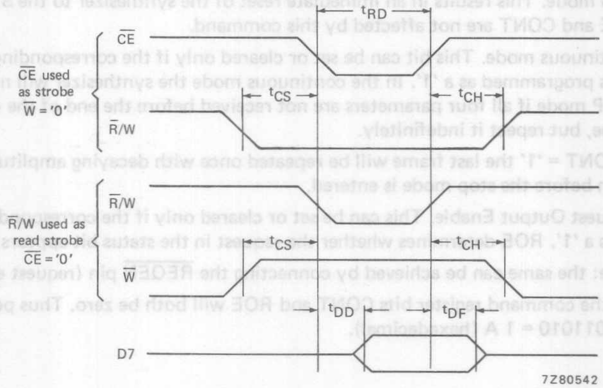



Fig. 6 Read timing.

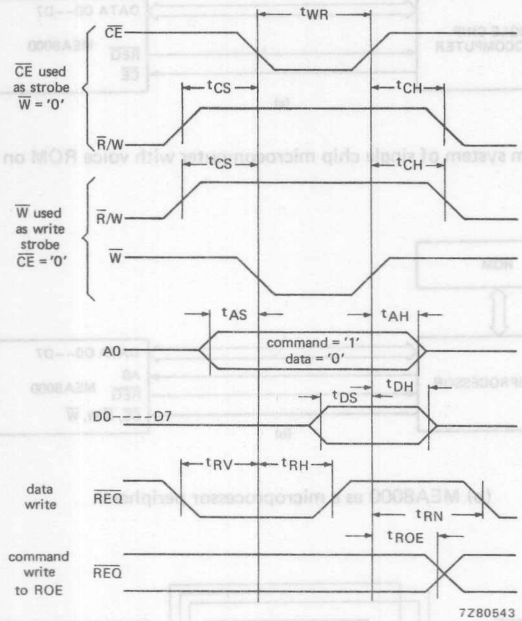
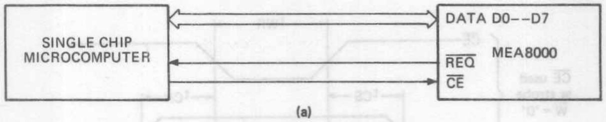
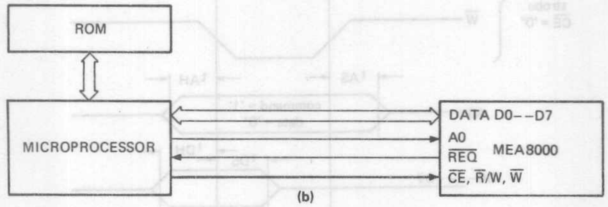


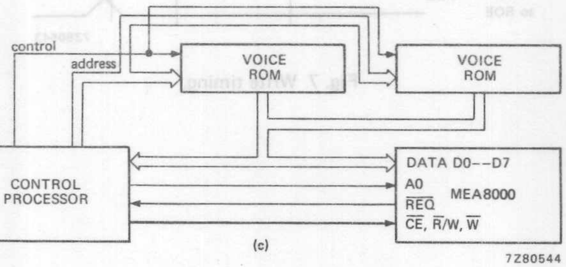

Fig. 7 Write timing.




(a) Minimum system of single chip microcomputer with voice ROM on board.




(b) MEA8000 as a microprocessor peripheral.




(c) Applications using separate voice ROMs.

Fig. 8 Typical applications.

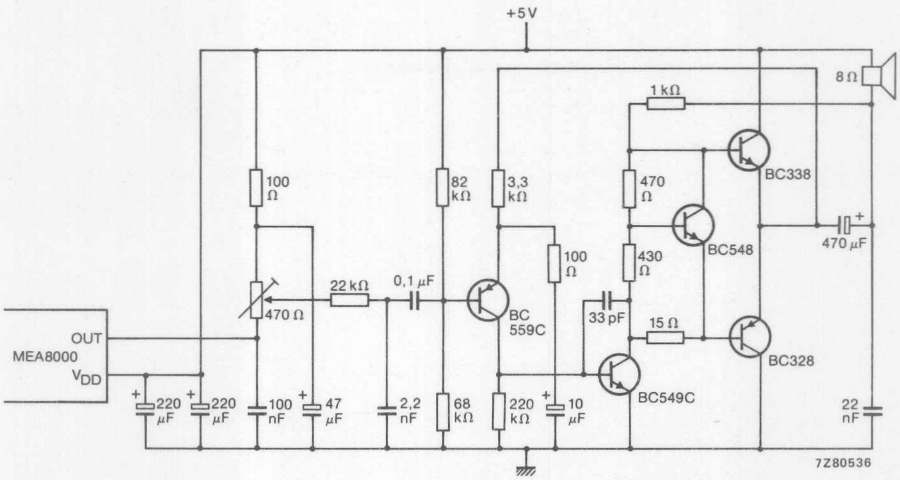



Fig. 9 Typical output applications.

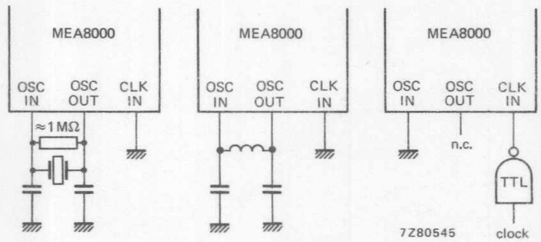



Fig. 10 Oscillator/clock configurations.

# INTEGRATED AMPLIFIER

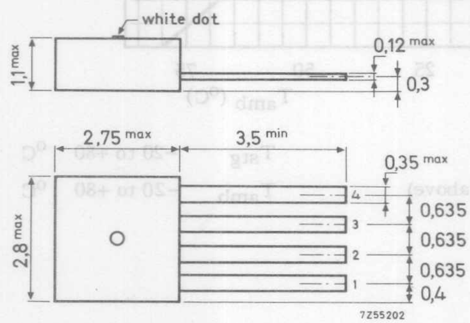
## for use in ear hearing aids

Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

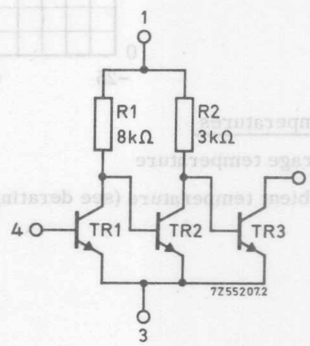
| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| For meaning of symbols see test circuit | | | | |
| Supply voltage | $V_{1-3}$ | max. | 5 | V |
| Supply current | $I_2$ | max. | 5 | mA |
| Total power dissipation up to $T_{amb}$ = 25 °C | $P_{tot}$ | max. | 25 | mW |
| The following data are measured in test circuit | | | | |
| Total supply current | $I_{tot}$ | typ. | 1 | mA |
| Transducer gain | $G_{tr}$ | > | 77 | dB |
| | | typ. | 85 | dB |
| Output power at $d_{tot}$ = 10% | $P_o$ | > | 0, 2 | mW |
| Cut-off frequency (−3 dB) | $f_c$ | > | 20 | kHz |

**PACKAGE OUTLINE** (Dimensions in mm)

SOT-20




**CIRCUIT DIAGRAM**




The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

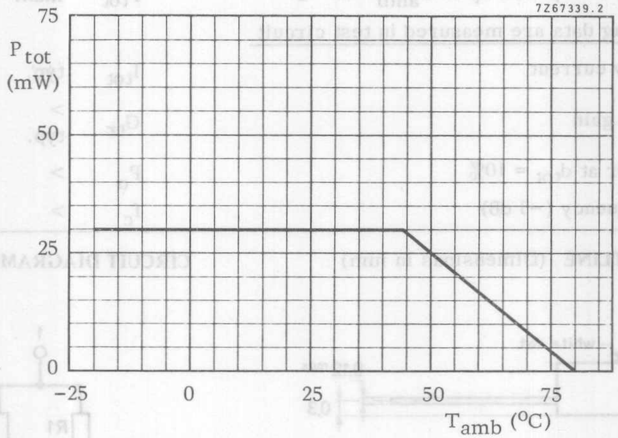
| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-3}$ | max. | 5 | V |
| Output voltage | $V_{2-3}$ | max. | 5 | V [1] |
| Input voltage | $-V_{4-3}$ | max. | 5 | V |

Currents

| | | | | |
|---|---|---|---|---|
| Output current | $I_2$ | max. | 5 | mA |
| Input current | $I_4$ | max. | 5 | mA |

Power dissipation

Power derating curve




Temperatures

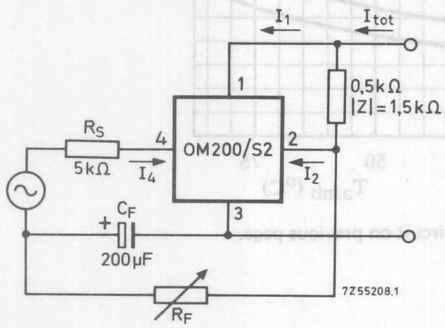
| | | |
|---|---|---|
| Storage temperature | $T_{stg}$ | −20 to +80 $^oC$ |
| Ambient temperature (see derating curve above) | $T_{amb}$ | −20 to +80 $^oC$ |

1) This value may be exceeded during inductive switch-off for transient energies < 10 μWs.

**CHARACTERISTICS** at $V_{1-3} = 1,3$ V; $I_2 = 0,7$ mA and $T_{amb} = 25\ ^oC$ unless otherwise specified

| | | | | | |
|---|---|---|---|---|---|
| Supply currents (no signal) | $I_{tot}$ | < | 1,1 | mA | |
| | $I_1$ | typ. | 0,30 | mA | |
| Transducer gain at f = 1 kHz | $G_{tr}$ | > | 77 | dB | 1) |
| | | typ. | 85 | dB | |
| Total distortion at f = 1 kHz | | | | | |
| $P_o = 100\ \mu W$ | $d_{tot}$ | typ. | 4 | % | |
| | | < | 6 | % | |
| $P_o = 200\ \mu W$ | $d_{tot}$ | < | 10 | % | |
| Noise figure at $R_S = 5\ k\Omega$ | | | | | |
| B = 400 to 3200 Hz | F | typ. | 2,5 | dB | |
| | | < | 6 | dB | 2) |
| Cut-off frequency (−3 dB) | $f_c$ | > | 20 | kHz | |
| Value of $R_F$ to adjust $I_2$ at 0,7 mA | $R_F$ | | 170 to 1000 | kΩ | |
| | | typ. | 400 | kΩ | |

Test circuit




Note

$I_2 = 0,7$ mA; adjusted by means of $R_F$
$V_{1-3} = 1,3$ V; $T_{amb} = 25\ ^oC$

---

1) The transducer gain is defined as the ratio of the output power in the load $|Z| = 1,5\ k\Omega$ and the available input power of the source with $R_S = 5\ k\Omega$.

$$G_{tr} = \frac{P_o}{V_i^2/4\,R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

## SOLDERING RECOMMENDATIONS

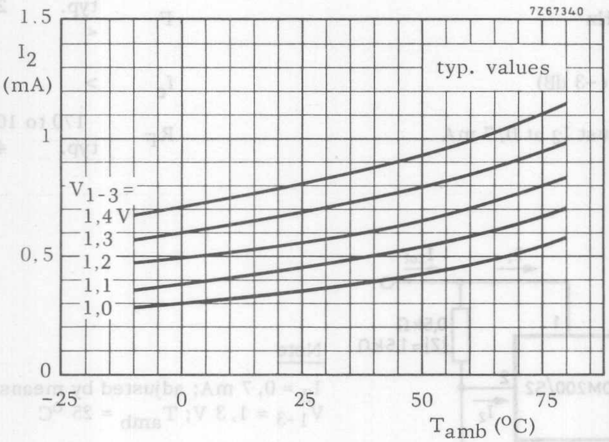
1. Iron soldering

   At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

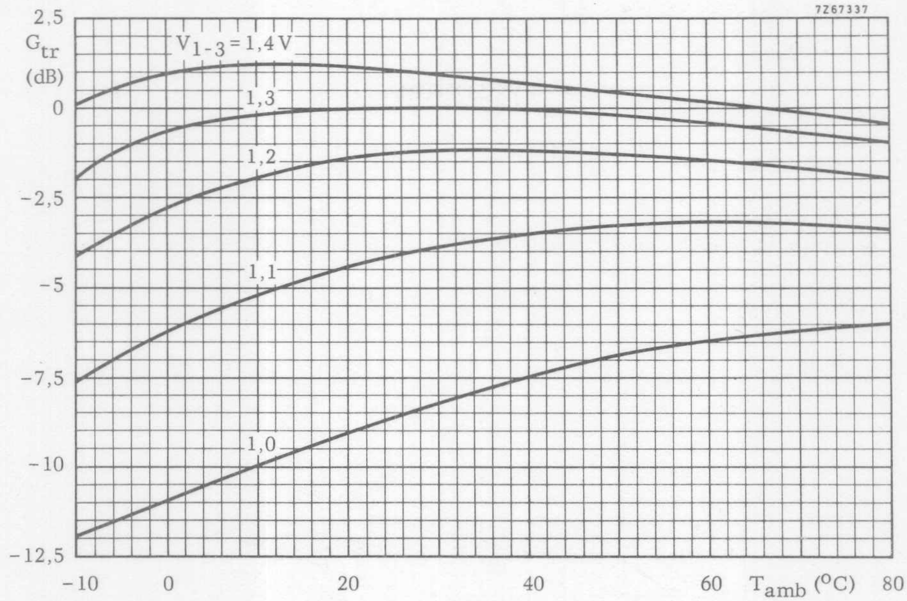
2. Dipsoldering

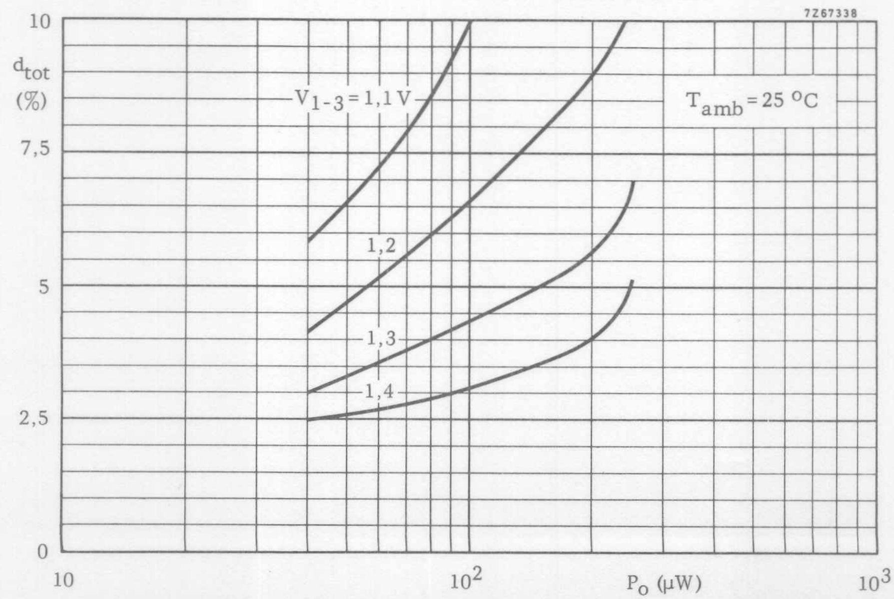
   At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

## CHARACTERISTICS




The graph applies to test circuit on previous page.


7Z67337
2,5
$G_{tr}$
(dB)
0
−2,5
−5
−7,5
−10
−12,5
$V_{1-3}$ = 1,4 V
1,3
1,2
1,1
1,0
−10
0
20
40
60
$T_{amb}$ (°C)
80


7Z67338
10
$d_{tot}$
(%)
7,5
5
2,5
0
$V_{1-3}$ = 1,1 V
1,2
1,3
1,4
$T_{amb}$ = 25 °C
10
$10^2$
$P_o$ (μW)
$10^3$

# LOW COST SPEECH DEMONSTRATION BOARD

## GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

## FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single + 5 V supply
- Low cost

## APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

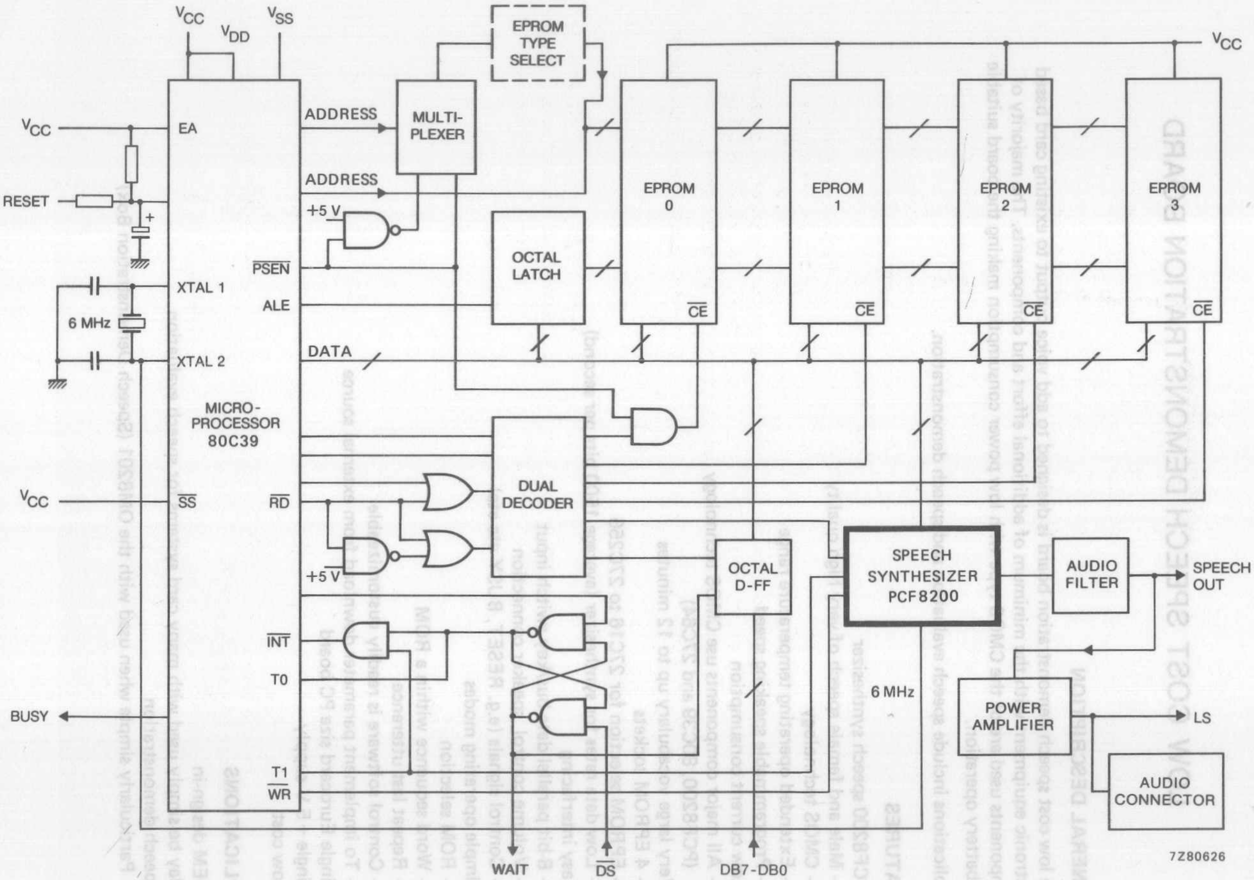



Fig. 1 Block diagram.

## OPERATION

### HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing.

The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.



### SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

– Male speech in several languages
– Female speech in several languages
– Programmable speaking speed

## ORDERING INFORMATION

**Product name:** Low Cost Speech Demonstration Board

**Type number:** OM8200

**Ordering code:** 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

# SPEECH DEMONSTRATION BOX

## GENERAL DESCRIPTION

Speech demonstration box OM8201 is designed to be used in conjunction with the low cost speech demonstration board OM8200. The box contains all the necessary components to drive the board. The combination of these two components make an extremely attractive demonstration unit.

## FEATURES

- Low cost
- Can use unmodified OM8200 board which allows access to all features of the OM8200
- Single + 9 V supply
  - Low power consumption therefore permits battery operation
  - External power supplies may also be used
  - Voltage is regulated and dropped to a standard + 5 V for the OM8200 board
- Simple mechanical construction
  - Allows easy access to the OM8200 for changing EPROMS
- Contains all peripherals needed to drive the OM8200

## HARDWARE DESCRIPTION

The box contains a set of eight keypad switches which are connected to the data bus. Four switches can select which EPROM your speech data is derived from. Repeated pressing of an EPROM switch increments the expression number which will be uttered. To repeat the last expression, a separate switch must be activated.

It is possible in the PCF8200 to change the rate of speaking to 73%, 123% or 145% of the normal speed. A switch has been included on the box which will sequence through the speed options making the same utterance every time.

One of the two remaining switches is the master reset for the program and the other is for future enhancements of the box.

Included in the box are, the volume control for the amplifier, the loudspeaker, and a high impedance audio output.

The final piece of electronics is the power supply. This can be supplied from a + 9 V internal battery or from a + 9 V external supply. The + 9 V is regulated to a + 5 V supply which is then fed to other parts of the box and to the OM8200.

The box is of simple construction and allows easy access to the OM8200 for changing of EPROMS.

## SOFTWARE DESCRIPTION

There is no software in the OM8201. The software of the OM8200 may be used in an unmodified form without any problems. However, if changes have been made to the control program of the OM8200 then different functions for the switches of the box can be achieved.

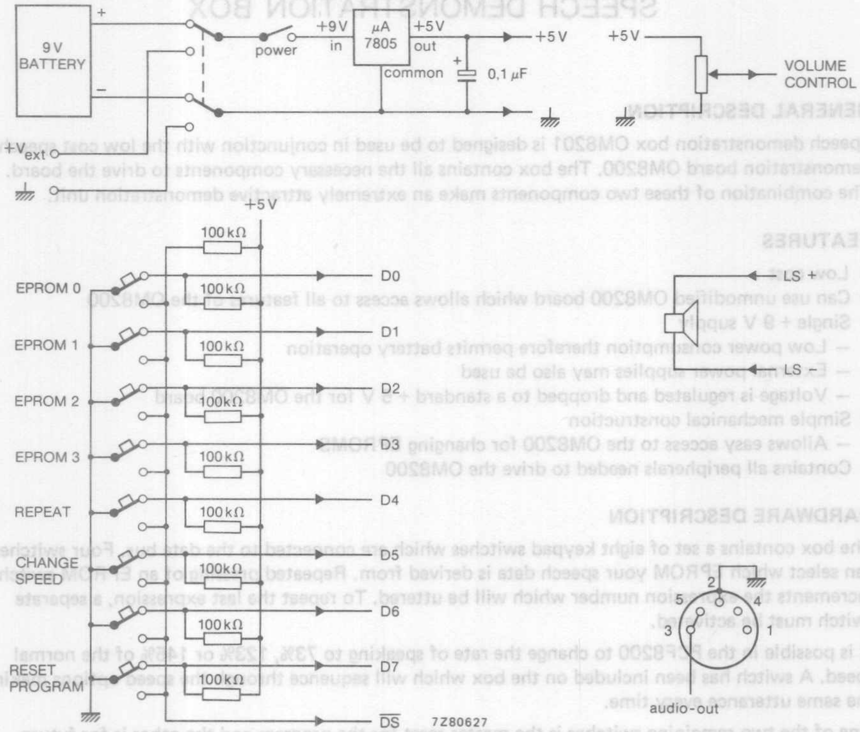



Fig. 1 Schematic diagram.

## ORDERING INFORMATION

**Product name:** Speech Demonstration Box

**Type number:** OM8201

**Ordering code:** 9337 541 40000

N.B. OM8200 must be ordered as well if this box is to be used in demonstration mode.
The order number for the OM8200 is 9337 541 30000.

Orders should be placed with your local Philips/Signetics agent.

# SPEECH ANALYSIS/EDITING SYSTEM

## GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses the HP9816S personal computer.

The OM8210 and the HP9816S function together to produce speech coding for the PCF8200.

The system has many commands available, mostly single key operations, which gives it flexability.

## FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

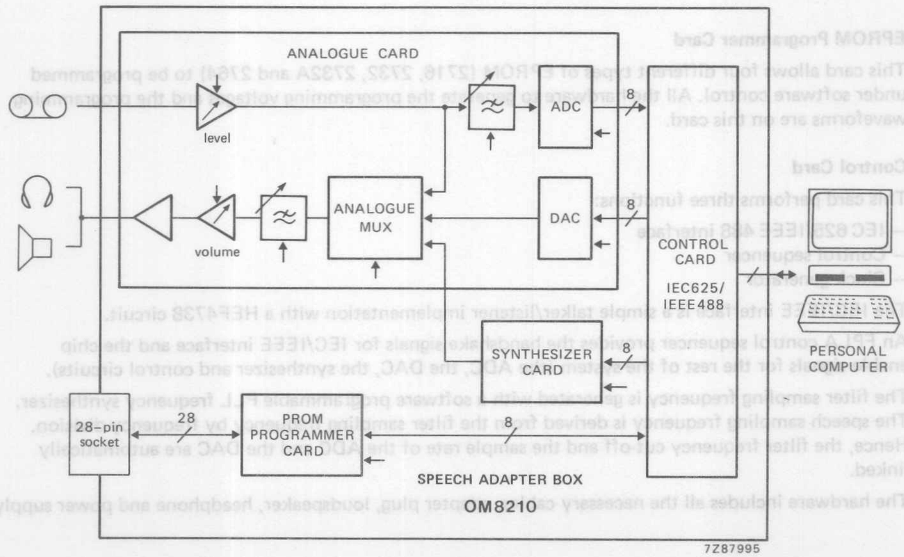



Fig. 1 Block diagram.

## HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

### Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

### Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

### EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

### Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

## SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

| | |
|---|---|
| Sample Mode | Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible. |
| Analysis Mode | Generates speech parameters from samples. The analysis selects the voiced/ unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters. |
| Parameter Edit Mode | Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration. |
| Code Mode | Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM. |
| EPROM Mode | Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands. |
| File Mode | Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library. |
| Media Mode | For diskette initialization and making back-up copies. |
| Option Mode | Allows the system configuration to be read or changed. |



The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

### Computer System

The following equipment is required to make a complete editing system:

- HP9816S-630 (optimum computer type)
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 k bytes total required)

## ORDERING INFORMATION

| | |
|---|---|
| **Product name:** | Speech Analysis/Editing System |
| **Type number:** | OM8210 |
| **Ordering code:** | 9337 561 50000 |

The Hewlett Packard computer should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# 128 x 8-BIT STATIC RAM

## GENERAL DESCRIPTION

The PCD8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus ($I^2C$). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

### Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 $\mu$A
- Power saving mode typ. 50 nA
- Serial input/output bus ($I^2C$)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

### Applications

- Telephony: RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications)
- Radio and television: channel presets
- Video cassette recorder
- General purpose: RAM expansion for the microcomputer families MAB8400 and PCF84C00

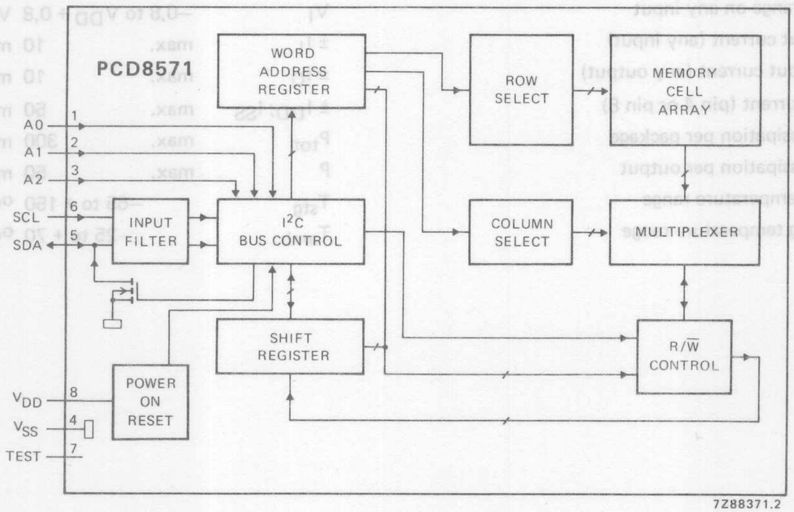



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCD8571P : 8-lead DIL; plastic (SOT-97A).
PCD8571D: 8-lead DIL; ceramic (cerdip) (SOT-151A).
PCD8571T: 8-lead mini-pack (SO-8L; SOT-176).

## PINNING

| | | |
|---|---|---|
| 1 to 3 | A0 to A2 | address inputs |
| 4 | $V_{SS}$ | negative supply |
| 5 | SDA | serial data line } $I^2C$ bus |
| 6 | SCL | serial clock line } $I^2C$ bus |
| 7 | TEST | test input for test speed-up; must be connected to $V_{SS}$ when not in use (power saving mode, see Fig. 14 and 15) |
| 8 | $V_{DD}$ | positive supply |

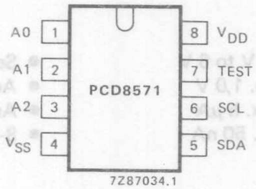



Fig. 2 Pinning diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage range (pin 8) | $V_{DD}$ | | –0,8 to + 8,0 V |
| Voltage range on any input | $V_I$ | | –0,8 to $V_{DD}$ + 0,8 V |
| D.C. input current (any input) | $\pm I_I$ | max. | 10 mA |
| D.C. output current (any output) | $\pm I_O$ | max. | 10 mA |
| Supply current (pin 4 or pin 8) | $\pm I_{DD}; I_{SS}$ | max. | 50 mA |
| Power dissipation per package | $P_{tot}$ | max. | 300 mW |
| Power dissipation per output | P | max. | 50 mW |
| Storage temperature range | $T_{stg}$ | | –65 to + 150 °C |
| Operating temperature range | $T_{amb}$ | | –25 to + 70 °C |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# LCD DUPLEX DRIVER

## GENERAL DESCRIPTION

The PCF2100 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

### Features

- 40 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

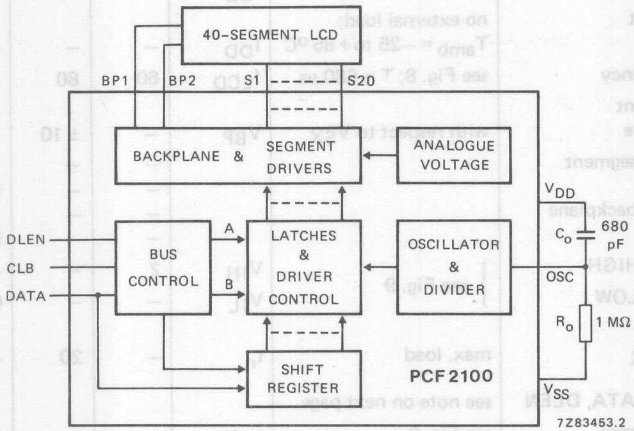



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT-117D).
PCF2100T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | −0,3 to 8 V |
| Voltage on any pin | $V_n$ | $V_{SS}$ −0,3 to $V_{DD}$ + 0,3 V |
| Operating ambient temperature range | $T_{amb}$ | −40 to + 85 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

## CHARACTERISTICS

$V_{DD}$ = 2,25 to 6,5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 to + 85 °C; $R_o$ = 1 MΩ; $C_o$ = 680 pF; unless otherwise specified

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply current | no external load | $I_{DD}$ | − | 10 | 50 | μA |
| Supply current | no external load; $T_{amb}$ = −25 to +85 °C | $I_{DD}$ | − | − | 30 | μA |
| Display frequency | see Fig. 8; τ = 680 μs | $f_{LCD}$ | 60 | 80 | 100 | Hz |
| D.C. component of LCD drive | with respect to $V_{SX}$ | $V_{BP}$ | − | ± 10 | − | mV |
| Load on each segment driver | | | − | − | 10 | MΩ |
| | | | − | − | 500 | pF |
| Load on each backplane driver | | | − | − | 1 | MΩ |
| | | | − | − | 5 | nF |
| Input voltage HIGH | see Fig. 9 | $V_{IH}$ | 2 | − | − | V |
| Input voltage LOW | see Fig. 9 | $V_{IL}$ | − | − | 0,6 | V |
| Rise time $V_{BP}$ to $V_{SX}$ | max. load | $t_r$ | − | 20 | − | μs |
| **Inputs CLB, DATA, DLEN** | see note on next page | | | | | |
| Rise and fall times | see Fig. 2 | $t_r$, $t_f$ | − | − | 10 | μs |
| CLB pulse width HIGH | see Fig. 2 | $t_{WH}$ | 1 | − | − | μs |
| CLB pulse width LOW | see Fig. 2 | $t_{WL}$ | 9 | − | − | μs |

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# LCD DUPLEX DRIVER

## GENERAL DESCRIPTION

The PCF2110 is a single chip, silicon gate CMOS circuit designed to drive 2 LEDs (Light Emitting Diodes) and an LCD (Liquid Crystal Display) with up to 60 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

### Features

- 60 LCD-segment drive capability
- Two LED-driver outputs
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

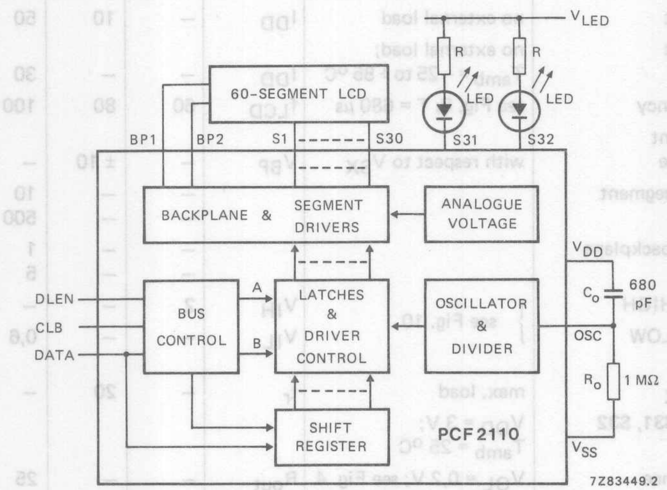



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF2110P: 40-lead DIL; plastic (SOT-129).
PCF2110T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | −0,3 to 8 V |
| Voltage on any pin | $V_n$ | $V_{SS}$ −0,3 to $V_{DD}$ + 0,3 V |
| Operating ambient temperature range | $T_{amb}$ | −40 to + 85 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

## CHARACTERISTICS

$V_{DD}$ = 2,25 to 6,5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 to + 85 °C; $R_o$ = 1 MΩ; $C_o$ = 680 pF; unless otherwise specified

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply current | no external load | $I_{DD}$ | – | 10 | 50 | μA |
| Supply current | no external load;<br>$T_{amb}$ = −25 to + 85 °C | $I_{DD}$ | – | – | 30 | μA |
| Display frequency | see Fig. 9; T = 680 μs | $f_{LCD}$ | 60 | 80 | 100 | Hz |
| D.C. component of LCD drive | with respect to $V_{SX}$ | $V_{BP}$ | – | ± 10 | – | mV |
| Load on each segment driver | | | – | – | 10 | MΩ |
| | | | – | – | 500 | pF |
| Load on each backplane driver | | | – | – | 1 | MΩ |
| | | | – | – | 5 | nF |
| Input voltage HIGH | see Fig. 10 | $V_{IH}$ | 2 | – | – | V |
| Input voltage LOW | see Fig. 10 | $V_{IL}$ | – | – | 0,6 | V |
| Rise time $V_{BP}$ to $V_{SX}$ | max. load | $t_r$ | – | 20 | – | μs |
| **LED outputs S31, S32** | $V_{DD}$ = 3 V;<br>$T_{amb}$ = 25 °C | | | | | |
| Output resistance | $V_{OL}$ = 0,2 V; see Fig. 4 | $R_{out}$ | – | – | 25 | Ω |
| Drain voltage | N-channel OFF | $V_{LED}$ | – | – | 8 | V |
| Drain current | maximum value | $I_{LEDmax}$ | – | – | 50 | mA |
| Total power dissipation | | $P_{tot}$ | – | – | 400 | mW |
| **Inputs CLB, DATA, DLEN** | see note on next page | | | | | |
| Input capacitance | for SOT-129 package | $C_{IN}$ | – | – | 10 | pF |
| | for SOT-158A package | $C_{IN}$ | – | – | 5 | pF |
| Rise and fall times | see Fig. 2 | $t_r$, $t_f$ | – | – | 10 | μs |
| CLB pulse width HIGH | see Fig. 2 | $t_{WH}$ | 1 | – | – | μs |
| CLB pulse width LOW | see Fig. 2 | $t_{WL}$ | 9 | – | – | μs |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# LCD DUPLEX DRIVER

## GENERAL DESCRIPTION

The PCF2111 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

### Features

- 64 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possiblity

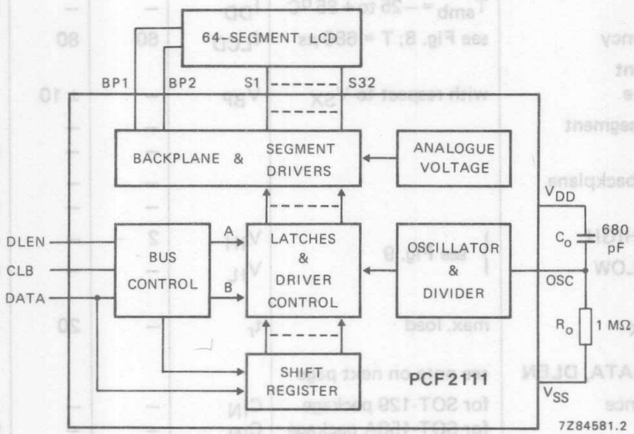



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | $-0,3$ to 8 | V |
| Voltage on any pin | $V_n$ | $V_{SS}$ $-0,3$ to $V_{DD}$ $+ 0,3$ | V |
| Operating ambient temperature range | $T_{amb}$ | $-40$ to $+ 85$ | $^{o}C$ |
| Storage temperature range | $T_{stg}$ | $-55$ to $+ 125$ | $^{o}C$ |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

## CHARACTERISTICS

$V_{DD} = 2,25$ to $6,5$ V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+ 85$ $^{o}C$; $R_o = 1$ MΩ; $C_o = 680$ pF; unless otherwise specified

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply current | no external load | $I_{DD}$ | – | 10 | 50 | µA |
| Supply current | no external load; $T_{amb} = -25$ to $+85$ $^{o}C$ | $I_{DD}$ | – | – | 30 | µA |
| Display frequency | see Fig. 8; T = 680 µs | $f_{LCD}$ | 60 | 80 | 100 | Hz |
| D.C. component of LCD drive | with respect to $V_{SX}$ | $V_{BP}$ | – | ± 10 | – | mV |
| Load on each segment driver | | | – | – | 10 | MΩ |
| | | | – | – | 500 | pF |
| Load on each backplane driver | | | – | – | 1 | MΩ |
| | | | – | – | 5 | nF |
| Input voltage HIGH | see Fig. 9 | $V_{IH}$ | 2 | – | – | V |
| Input voltage LOW | see Fig. 9 | $V_{IL}$ | – | – | 0,6 | V |
| Rise time $V_{BP}$ to $V_{SX}$ | max. load | $t_r$ | – | 20 | – | µs |
| **Inputs CLB, DATA, DLEN** | see note on next page | | | | | |
| Input capacitance | for SOT-129 package | $C_{IN}$ | – | – | 10 | pF |
| | for SOT-158A package | $C_{IN}$ | – | – | 5 | pF |
| Rise and fall times | see Fig. 2 | $t_r$, $t_f$ | – | – | 10 | µs |
| CLB pulse width HIGH | see Fig. 2 | $t_{WH}$ | 1 | – | – | µs |
| CLB pulse width LOW | see Fig. 2 | $t_{WL}$ | 9 | – | – | µs |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# LCD DRIVER

## GENERAL DESCRIPTION

The PCF2112 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 32 segments in direct drive; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

### Features

- 32 LCD-segment drive capability.
- Supply voltage 2,25 to 6,5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.

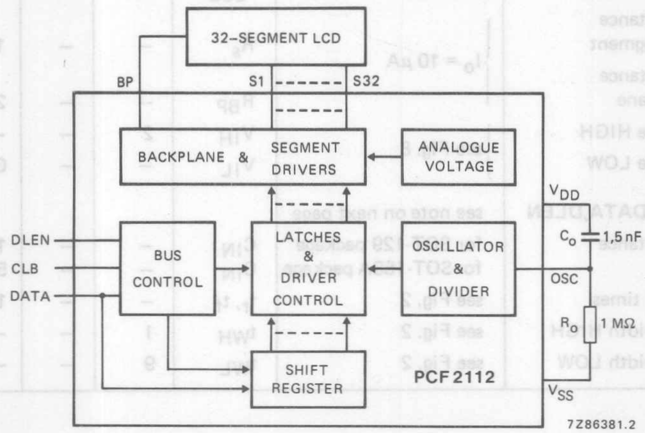



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF2112P : 40-lead DIL; plastic (SOT-129).
PCF2112T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage with respect to $V_{SS}$ | $V_{DD}$ | −0,3 to 8 V |
| Voltage on any pin | $V_n$ | $V_{SS}$−0,3 to $V_{DD}$ + 0,3 V |
| Operating ambient temperature range | $T_{amb}$ | −40 to +85 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

## CHARACTERISTICS

$V_{DD}$ = 2,25 to 6,5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 to + 85 °C; $R_o$ = 1 MΩ; $C_o$ = 1,5 nF; unless otherwise specified.

| parameter | condition | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply current | no external load | $I_{DD}$ | – | 10 | 50 | μA |
| Supply current | no external load; $T_{amb}$ = −25 to +85 °C | $I_{DD}$ | – | – | 30 | μA |
| Display frequency | T = 1,5 ms | $f_{LCD}$ | 30 | 40 | 50 | Hz |
| Output resistance of each segment | $I_o$ = 10 μA | $R_s$ | – | – | 10 | kΩ |
| Output resistance of backplane | $I_o$ = 10 μA | $R_{BP}$ | – | – | 2 | kΩ |
| Input voltage HIGH | see Fig. 8 | $V_{IH}$ | 2 | – | – | V |
| Input voltage LOW | see Fig. 8 | $V_{IL}$ | – | – | 0,6 | V |
| **Inputs CLB,DATA,DLEN** | see note on next page | | | | | |
| Input capacitance | for SOT-129 package | $C_{IN}$ | – | – | 10 | pF |
| | for SOT-158A package | $C_{IN}$ | – | – | 5 | pF |
| Rise and fall times | see Fig. 2 | $t_r$, $t_f$ | – | – | 10 | μs |
| CLB pulse width HIGH | see Fig. 2 | $t_{WH}$ | 1 | – | – | μs |
| CLB pulse width LOW | see Fig. 2 | $t_{WL}$ | 9 | – | – | μs |

# VOICE SYNTHESIZER

## GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

### Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I²C bus
- Software readable status word (parallel bus or I²C bus)
- BUSY-signal and REQN-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

## QUICK REFERENCE DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | – | 5 | – | V |
| Supply current | $I_{DD}$ | – | 10 | t.b.f. | mA |
| Supply current (stand-by) | $I_{DD(SB)}$ | – | 200 | – | μA |
| **Inputs** | | | | | |
| Input voltage | $V_{IH}$ | 2,0 | – | $V_{DD}$ | V |
| Input voltage | $V_{IL}$ | 0 | – | 0,8 | V |
| Input capacitance | $C_I$ | – | 7 | – | pF |
| **Outputs** (D5 to D7) | | | | | |
| Output voltage high | $V_{OH}$ | 3,5 | – | $V_{DD}$ | V |
| Output voltage low | $V_{OL}$ | 0 | – | 0,4 | V |
| Load capacitance | $C_L$ | – | – | 80 | pF |
| Operating ambient temperature range | $T_{amb}$ | −40 | – | + 85 | °C |

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

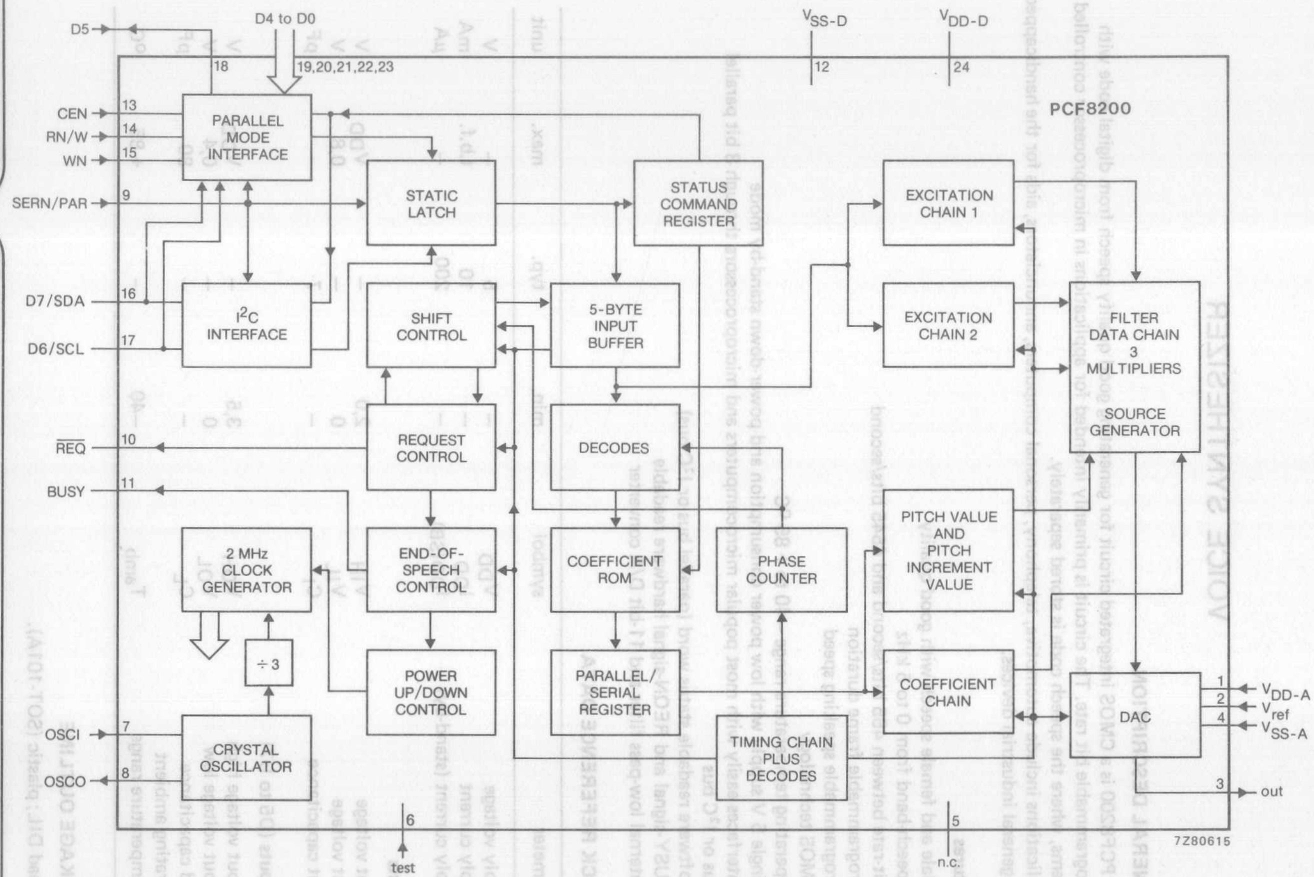



Fig. 1 Block diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{DD-A}$ | supply |
| 2 | $V_{REF}$ | supply |
| 3 | OUT | output |
| 4 | $V_{SS-A}$ | supply |
| 5 | NC | not connected |
| 6 | TEST | input |
| 7 | OSCI | input |
| 8 | OSCO | output |
| 9 | SERN/PAR | input |
| 10 | REQN | output |
| 11 | BUSY | output |
| 12 | $V_{SS-D}$ | supply |
| 13 | CEN | input |
| 14 | RN/W | input |
| 15 | WN | input |
| 16 | SDA/D7 | input/output |
| 17 | SCL/D6 | input/output |
| 18 | D5 | input/output |
| 19 | D4 | input |
| 20 | D3 | input |
| 21 | D2 | input |
| 22 | D1 | input |
| 23 | D0 | input |
| 24 | $V_{DD-D}$ | supply |

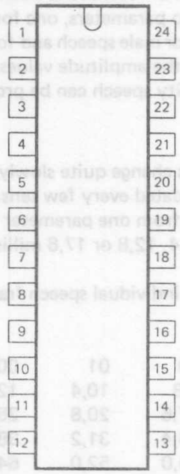



Fig. 2 Pinning diagram.

DEVELOPMENT DATA

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply voltage* | $V_{DD}$ | min. | −0,3 | max. | 7,5 | V |
| Input voltage* | $V_I$ | min. | −0,3 | max. | 7,5 | V |
| Output voltage* | $V_O$ | min. | −0,3 | max. | 7,5 | V |
| Operating ambient temperature range | $T_{amb}$ | | | | −40 to + 85 | °C |
| Storage temperature range | $T_{stg}$ | | | | −55 to + 125 | °C |

* Any pin with respect to $V_{SS}$.

## FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

## OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

| FD1, FD0 | 10 | 01 | 00 | 11 | FS1, FS0 |
|---|---|---|---|---|---|
| 00 | 8,8 | 10,4 | 12,8 | 17,6 | ms |
| 01 | 17,6 | 20,8 | 25,6 | 35,2 | ms |
| 10 | 26,4 | 31,2 | 38,4 | 52,8 | ms |
| 11 | 44,0 | 52,0 | 64,0 | 88,0 | ms |

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation. A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

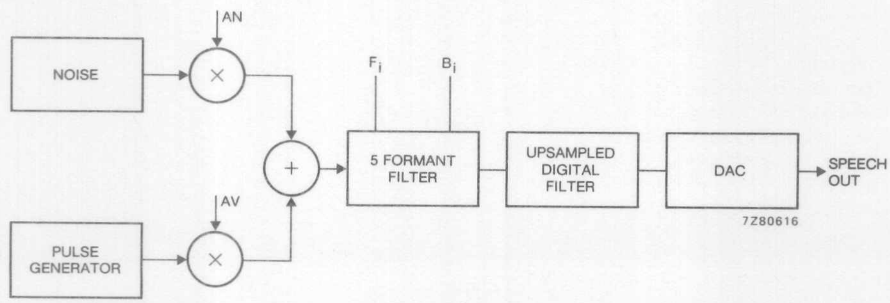



Fig. 3 Block diagram of formant synthesizer.

## DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

### DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or $V_{DD}$ on. Table 2 indicates the amplitude factor.

| byte | factor | dB |
|---|---|---|
| 01110000 | 3,5 | 10,88 |
| 10110000 | 3,25 | 10,24 |
| 00110000 | 3,0 | 9,54 |
| 11010000 | 2,75 | 8,97 |
| 01010000 | 2,5 | 7,96 |
| 10010000 | 2,25 | 7,04 |
| 00010000 | 2,0 | 6,02 |
| 11100000 | 1,75 | 4,86 |
| 01100000 | 1,5 | 3,52 |
| 10100000 | 1,25 | 1,94 |
| 00100000 | 1,0 | 0,00 |
| 11000000 | 0,75 | −2,50 |
| 01000000 | 0,5 | −6,02 |
| 10000000 | 0,25 | −12,04 |
| 00000000 | 0,0 | |
| 11110000 | HEX code F0 and is not allowed as a DAC amplitude | |

Table 2 DAC amplitude factor.

### Start pitch

The second byte after a STOP or BADSTOP, or $V_{DD}$ on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

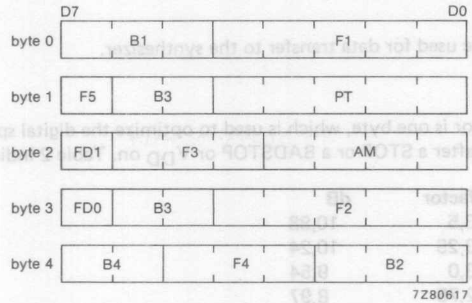
### Frame Data

The frame data is a five byte block which contains the filter and source information:

| | |
|---|---|
| pitch increment/decrement value | 5 bits |
| amplitude | 4 bits |
| frame duration | 2 bits |
| frequency of 1st formant | 5 bits |
| frequency of 2nd formant | 5 bits |
| frequency of 3rd formant | 3 bits |
| frequency of 4th formant | 3 bits |
| frequency of 5th formant | 1 bit |
| bandwidth of 1st formant | 3 bits |
| bandwidth of 2nd formant | 3 bits |
| bandwidth of 3rd formant | 2 bits |
| bandwidth of 4th formant | 2 bits |
| bandwidth of 5th formant | 2 bits |
| | 40 bits = 5 bytes |

The frame-data bits are organized as shown in Fig. 4.

DEVELOPMENT DATA




It is not allowed to set byte 0 to the hexadecimal value E0.

Fig. 4 Format of frame-date.

## CONTROL FORMAT

### Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

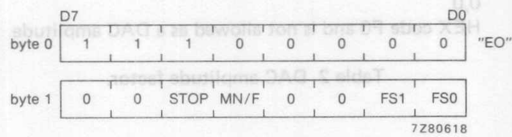



Fig. 5 Control write: first byte fixed, second byte control.

**FS0, FS1 speed option**

| FS1 | FS0 | speech speed | standard-frame duration |
|---|---|---|---|
| 0 | 0 | 100% | 12,8 ms |
| 0 | 1 | 123% | 10,4 ms |
| 1 | 0 | 145% | 8,8 ms |
| 1 | 1 | 73% | 17,6 ms |

**MN/F, male/female option**

MN/F = 0 male quantization table
= 1 female quantization table

**STOP**

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. REQN = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

### Status Read

Three status bits can be read out at any time without a preceding byte (E0).
This is shown in Fig. 6.

| D7 | | | | | | | D0 |
|---|---|---|---|---|---|---|---|
| REQN | BUSY | STOP | x | x | x | x | x |

7Z80619

Fig. 6 Status read.

| | | |
|---|---|---|
| REQN | = 1 | No data required |
| | = 0 | Synthesizer requesting for new data |
| BUSY | = 1 | Busy (an utterance is pronounced) |
| | = 0 | Idle, REQN will set to 1; the synthesizer is in STOP or BADSTOP mode |
| STOP | | The STOP bit is the same as the stop bit written to the synthesizer during a command write. |
| | | STOP = 1, BUSY = 0 stopped by the user. |
| | | STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time. |

DEVELOPMENT DATA

After initial power-up the status/command register is set to the following status:

| | | |
|---|---|---|
| FS0, FS1 | = 0 | Standard-frame duration of 12,8 ms |
| MN/F | = 0 | Male quantization table |
| STOP | = 1 | |
| BUSY | = 0 | Idle |
| REQN | = 1 | No data required |

## INTERFACE PROTOCOL

Data can be written to the synthesizer when REQN = 0 or, when REQN = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The $I^2C$ transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit REQN will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

## $I^2C$ ADDRESS

On chip there is a $I^2C$ slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

## POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

| | |
|---|---|
| PAR-mode: | The input-latches are active so they can receive the first byte |
| SER-mode: | The $I^2C$ transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, CEN, while WN = 0 and RN/W = 1. The synthesizer can be set to permanent power-up by hard-wired control pins (CEN = 0, RN/W = 1, WN = 0). |

## POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial $V_{DD}$ the synthesizer is in power-down mode.

## SERN/PAR

SERN/PAR is hard-wired to $V_{DD}$ or $V_{SS}$.

## HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

DEVELOPMENT DATA

## CHARACTERISTICS

$T_{amb}$ = −45 to + 85 °C; supply voltage ($V_{DD}$ to $V_{SS}$) = 4,5 V to 5,5 V with respect to $V_{SS}$, otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage | $V_{DD}$ | 4,5 | 5,0 | t.b.f. | V |
| Supply current | $I_{DD}$ | − | 10 | − | mA |
| Standby current | $I_{DD(SB)}$ | − | 200 | − | μA |
| **Inputs** | | | | | |
| **CEN, RN/W, WN, OSCI** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | − | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | − | 0,8 | V |
| Input leakage current $V_{in}$ = 0 to 5,5 V | $I_{IR}$ | −10 | − | 10 | μA |
| Rise and fall times (note 2) | $t_{rf}$ | − | − | 50 | ns |
| Input capacitance | $C_I$ | − | − | 7 | pF |
| **PARALLEL MODE** | | | | | |
| **Input Characteristics (D0 to D7)** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | − | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | − | 0,8 | V |
| Input leakage current ($V_{in}$ = 0 to 5,5 V, output off) | $I_{IR}$ | −10 | − | 10 | μA |
| Input capacitance | $C_I$ | − | − | 7 | pF |
| **Output Characteristics (D5 to D7 only)** | | | | | |
| Output voltage HIGH ($I_{OH}$ = −100 μA) | $V_{OH}$ | 3,5 | − | $V_{DD}$ | V |
| Output voltage LOW ($I_{OL}$ = 3,2 mA) | $V_{OL}$ | 0 | − | 0,4 | V |
| Load capacitance | $C_L$ | − | − | 80 | pF |
| Rise and fall times (note 3) | $t_{rf}$ | − | − | 50 | ns |
| **SERIAL MODE** | | | | | |
| **Input Characteristics (SDA and SDL)** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 3,0 | − | $V_{DD}$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | − | 1,5 | V |
| Input leakage current ($V_{in}$ = 0 to 5,5 V, output off) | $I_{IR}$ | −10 | − | 10 | μA |
| Input capacitance | $C_I$ | − | − | 10 | pF |
| **Output Characteristics (SDA only, open drain)** | | | | | |
| Output voltage LOW ($I_{OL}$ = 3 mA) | $V_{OL}$ | 0 | − | 0,4 | V |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Crystal frequency | $f_{XTAL}$ | t.b.f. | 6 | t.b.f. | MHz |
| $V_{REF}$ | | | | | |
| Reference voltage | $V_{REF}$ | 1,9 | – | $\frac{V_{DD}-1,5}{1,25}$ | V |
| Input leakage current | $I_{IR}$ | – | t.b.f. | | |
| **Outputs** | | | | | |
| **REQN, BUSY** | | | | | |
| Output voltage HIGH ($I_{OH}$ = 100 $\mu$A) | $V_{OH}$ | 3,5 | – | $V_{DD}$ | V |
| Output voltage LOW ($I_{OL}$ = 3,2 mA) | $V_{OL}$ | 0 | – | 0,4 | V |
| Load capacitance | $C_L$ | – | – | 80 | pF |
| Rise and fall times (note 3) | $t_{rf}$ | – | – | 50 | ns |
| **OUT** | | | | | |
| Output voltage | $V_{OUT}$ | 0,66 x $V_{REF}$ | | 1,34 x $V_{REF}$ | V |
| Minimum external load | | 600 | – | – | Ω |
| **Timing characteristics** (note 1) (Figs 8 and 9) | | | | | |
| Write enable | $t_{WR}$ | 200 | – | – | ns |
| Data set-up for write | $t_{DS}$ | 150 | – | – | ns |
| Data hold for write | $t_{DH}$ | 30 | – | – | ns |
| Read enable | $t_{RD}$ | 200 | – | – | ns |
| Data delay for read (note 2) | $t_{DD}$ | – | – | 150 | ns |
| Data floating for read (note 2) | $t_{DF}$ | – | – | 150 | ns |
| Control set-up | $t_{CS}$ | 0 | – | – | ns |
| Control hold | $t_{CH}$ | 0 | – | – | ns |
| REQ new (new byte of the same speech frame) | $t_{RN}$ | – | t.b.f. (≈ 3) | | us |
| REQ Valid | $t_{RV}$ | 0 | – | – | ns |
| REQ Hold | $t_{RH}$ | – | 250 | t.b.f. | ns |

**NOTES TO THE CHARACTERISTICS**

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

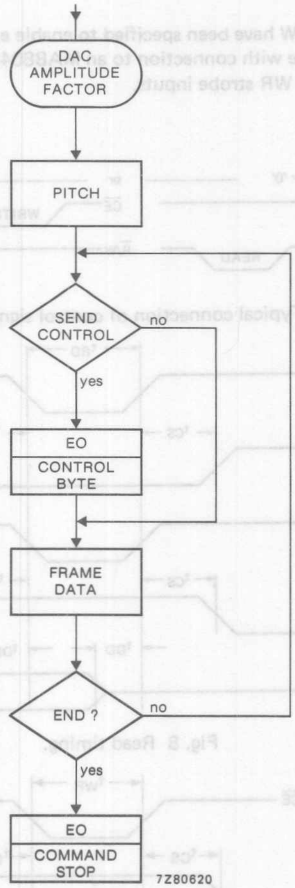
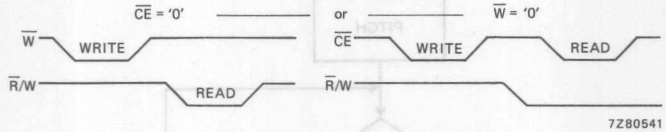



Fig. 7 Interface protocol.

DEVELOPMENT DATA

### Timing diagrams

The control signals CE, R/W and W have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the R/W and W inputs can be used as the RD and WR strobe inputs.




Typical connection of control signals.

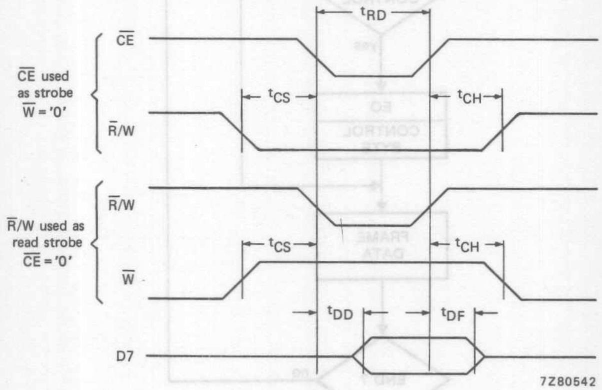



Fig. 8 Read timing.

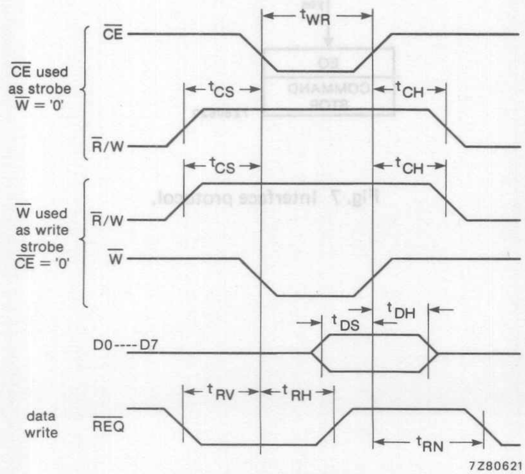



Fig. 9 Write timing.

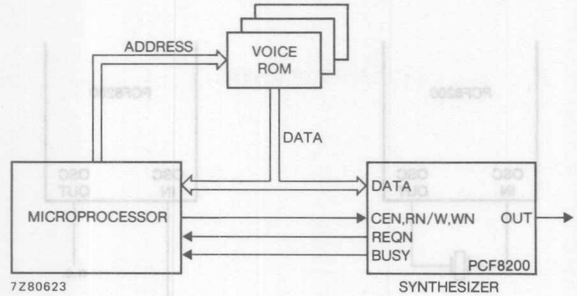



Fig. 10 Typical application configuration with parallel interface.

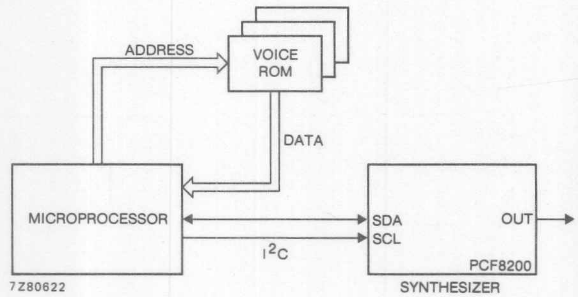



Fig. 11 Typical application configuration with series interface.

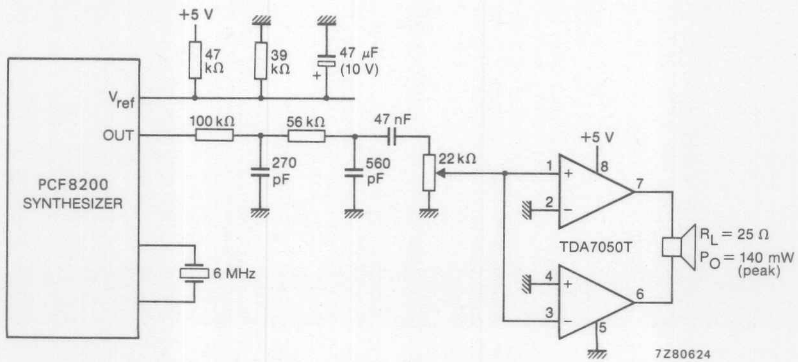



Fig. 12 An example of an output configuration.

DEVELOPMENT DATA

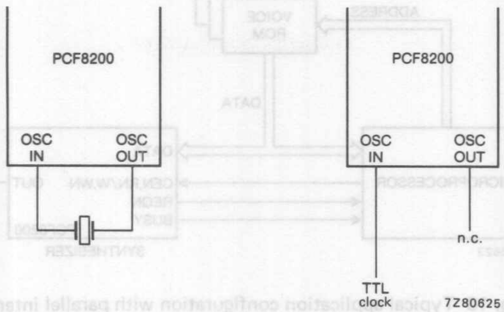



Fig. 13 Oscillator clock configurations.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# 256 x 8-BIT STATIC RAM

## GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus ($I^2C$). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

### Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 $\mu$A
- Power saving mode typ. 50 nA
- Serial input/output bus ($I^2C$)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

### Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcontroller families MAB8400 and PCF84C00

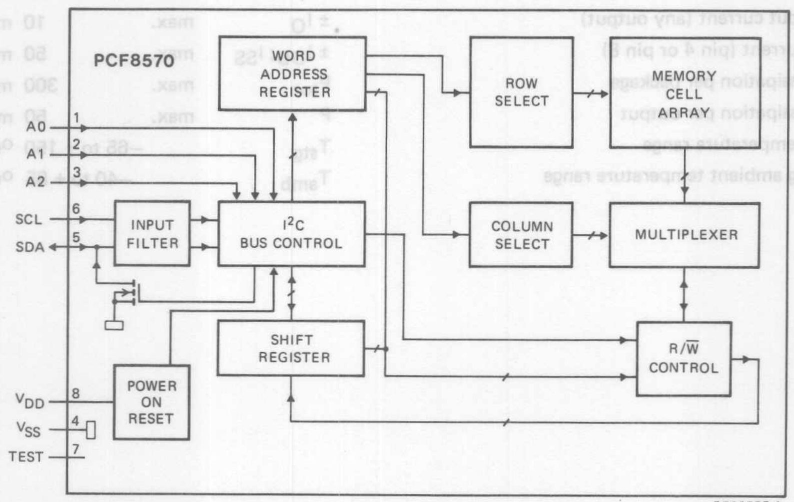



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97A).
PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

## PINNING

| | | |
|---|---|---|
| 1 to 3 | A0 to A2 | address inputs |
| 4 | $V_{SS}$ | negative supply |
| 5 | SDA | serial data line } $I^2C$ bus |
| 6 | SCL | serial clock line } $I^2C$ bus |
| 7 | TEST | test input for test speed-up; must be connected to $V_{SS}$ when not in use (power saving mode, see Figs 14 and 15) |
| 8 | $V_{DD}$ | positive supply |

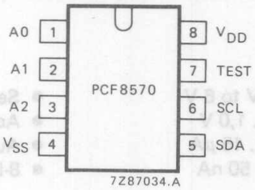



Fig. 2 Pinning diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 8) | $V_{DD}$ | | −0,8 to +8,0 | V |
| Voltage range on any input | $V_I$ | | −0,8 to $V_{DD}$ + 0,8 | V |
| D.C. input current (any input) | $\pm I_I$ | max. | 10 | mA |
| D.C. output current (any output) | $\pm I_O$ | max. | 10 | mA |
| Supply current (pin 4 or pin 8) | $\pm I_{DD}$; $I_{SS}$ | max. | 50 | mA |
| Power dissipation per package | $P_{tot}$ | max. | 300 | mW |
| Power dissipation per output | P | max. | 50 | mW |
| Storage temperature range | $T_{stg}$ | | −65 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −40 to + 85 | °C |

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# CLOCK/CALENDAR WITH SERIAL I/O

## GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC ($I^2C$) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus ($I^2C$). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

### Features

- Serial input/output bus ($I^2C$) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (clock) | $V_{DD}-V_{SS1}$ | | 1,1 to 6,0 | V |
| Supply voltage range ($I^2C$ interface) | $V_{DD}-V_{SS2}$ | | 2,5 to 6,0 | V |
| Crystal oscillator frequency | $f_{osc}$ | typ. | 32,768 | kHz |

## PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

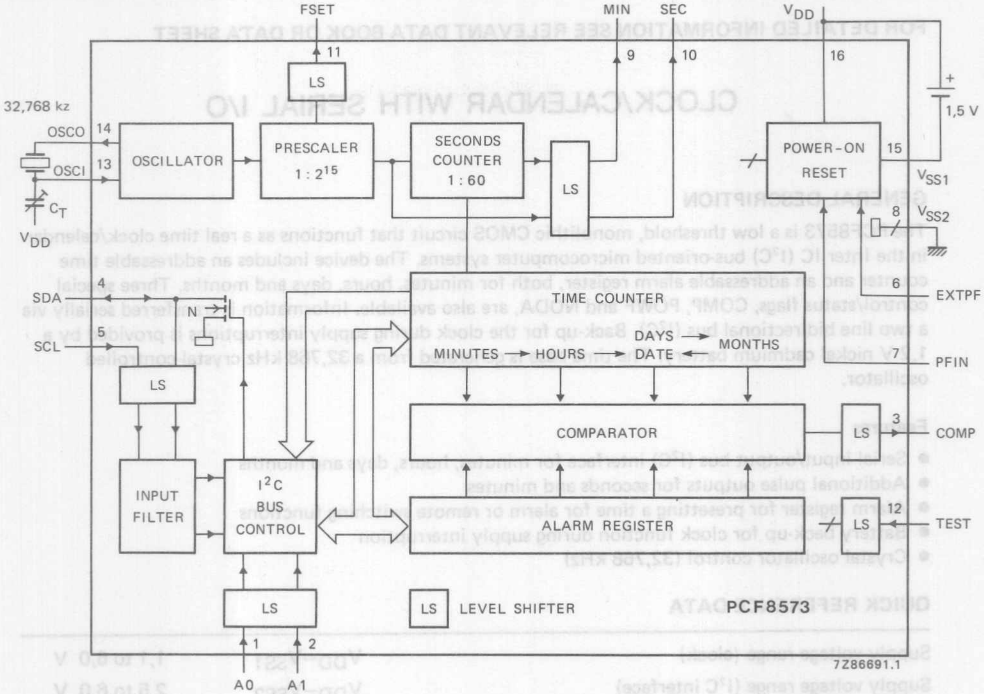



Fig. 1 Block diagram.

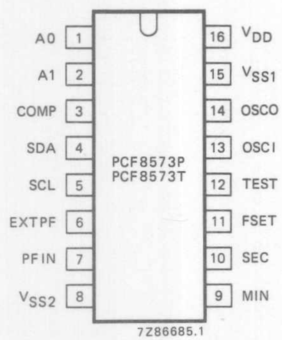



Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | A0 | address input |
| 2 | A1 | address input |
| 3 | COMP | comparator output |
| 4 | SDA | serial data line } I²C bus |
| 5 | SCL | serial clock line } I²C bus |
| 6 | EXTPF | enable power fail flag input |
| 7 | PFIN | power fail flag input |
| 8 | $V_{SS2}$ | negative supply 2 (I²C interface) |
| 9 | MIN | one pulse per minute output |
| 10 | SEC | one pulse per second output |
| 11 | FSET | oscillator tuning output |
| 12 | TEST | test input; must be connected to $V_{SS2}$ when not in use |
| 13 | OSCI | oscillator input |
| 14 | OSCO | oscillator input/output |
| 15 | $V_{SS1}$ | negative supply 1 (clock) |
| 16 | $V_{DD}$ | common positive supply |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# REMOTE 8-BIT I/O FOR $I^2C$ BUS

## GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus ($I^2C$). It can also interface microcomputers without a serial interface to the $I^2C$ bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an $I^2C$ interface.

The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the $I^2C$ bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the $I^2C$ bus. This means that the PCF8574 can remain a simple slave device.

### Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 $\mu$A
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the $I^2C$ bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

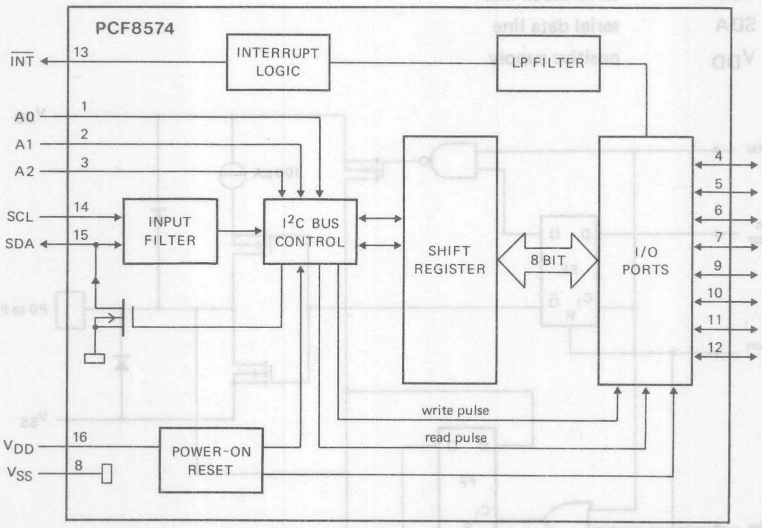



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).

PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

## PINNING

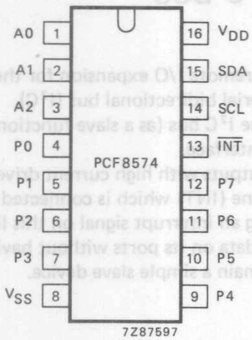



Fig. 2 Pinning diagram.

| | | |
|---|---|---|
| 1 to 3 | A0 to A2 | address inputs |
| 4 to 7 | P0 to P3 | 8-bit quasi-bidirectional I/O port |
| 9 to 12 | P4 to P7 | |
| 8 | $V_{SS}$ | negative supply |
| 13 | $\overline{INT}$ | interrupt output |
| 14 | SCL | serial clock line |
| 15 | SDA | serial data line |
| 16 | $V_{DD}$ | positive supply |

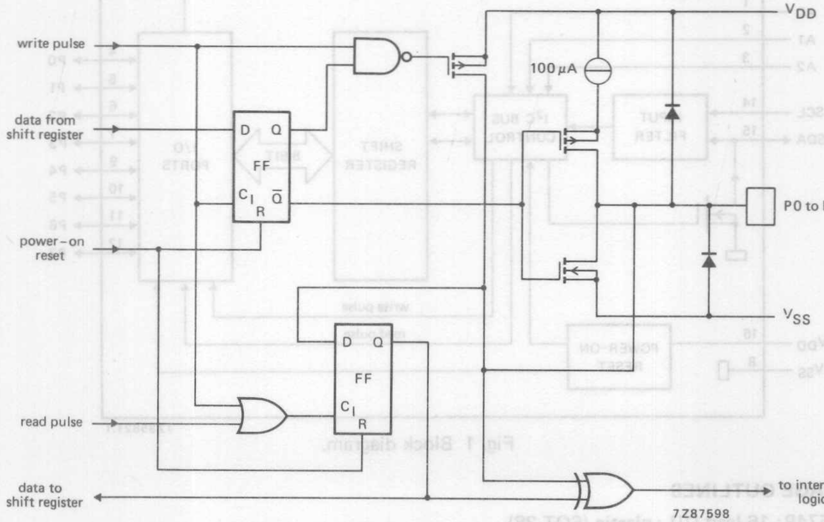



Fig. 3 Simplified schematic diagram of each port.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

## GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus ($I^2C$). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

### Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- $I^2C$ bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with Philips/Videlec chip-on-glass technology
- Manufactured in silicon gate CMOS process

## PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray

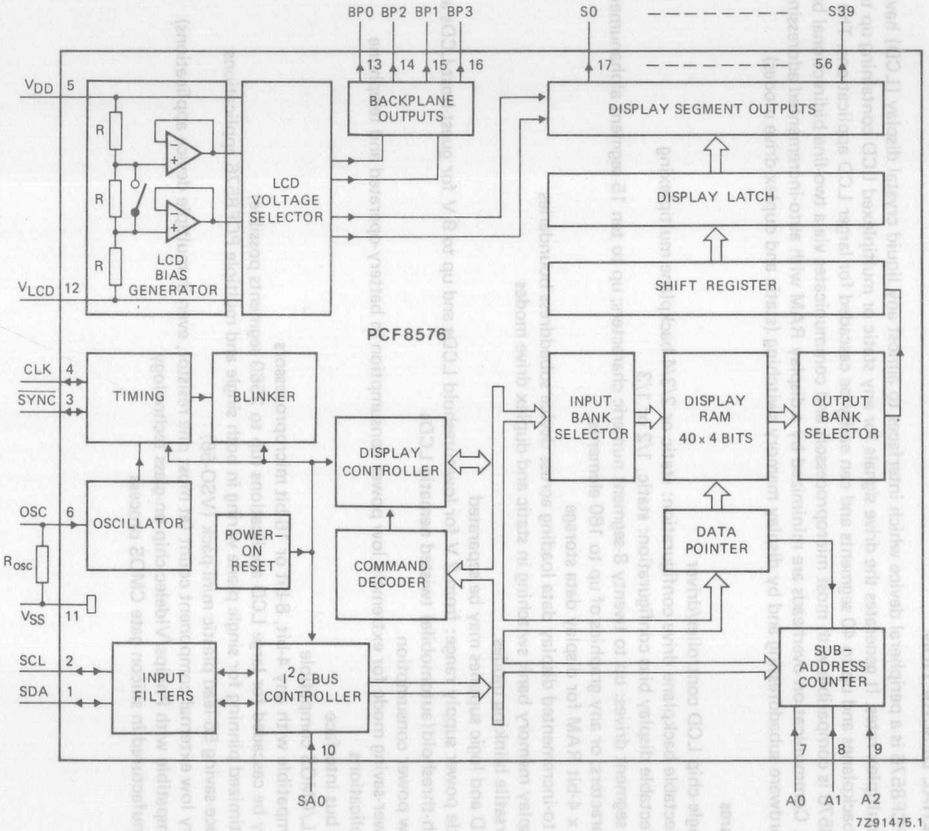



Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

## GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

### Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

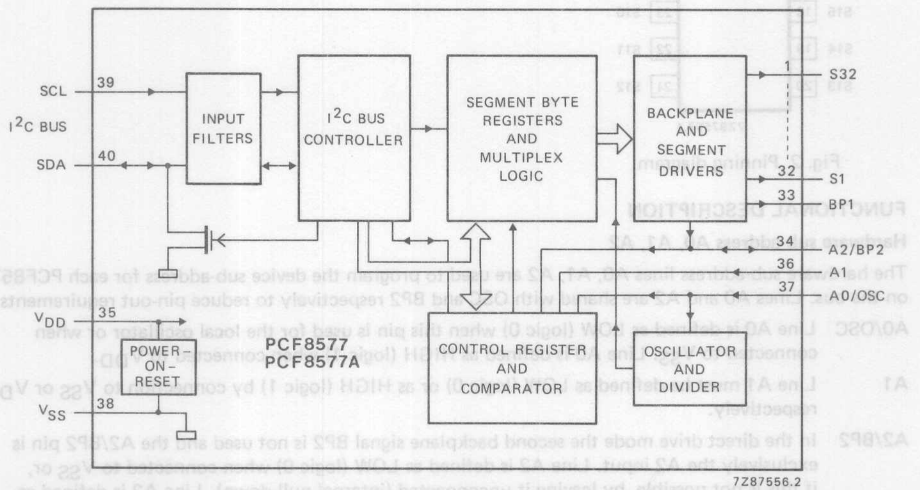



Fig. 1 Block diagram.

## PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

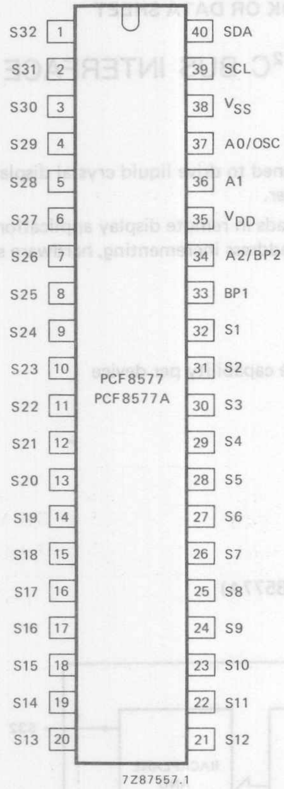



Fig. 2 Pinning diagram.

## PINNING

**Supply**

| | | |
|---|---|---|
| 35 | $V_{DD}$ | positive supply |
| 38 | $V_{SS}$ | negative supply |

**$I^2C$ bus**

| | | |
|---|---|---|
| 40 | SDA | $I^2C$ bus data line |
| 39 | SCL | $I^2C$ bus clock line |

**Inputs**

| | | |
|---|---|---|
| 36 | A1 | hardware address line |
| 37 | A0/OSC | hardware address line/oscillator pin |

**Outputs**

| | | |
|---|---|---|
| 1 – 32 | S1 – S32 | segment outputs |

**Input – Output**

| | | |
|---|---|---|
| 34 | A2/BP2 | harware address line/cascade sync input/backplane output |
| 33 | BP1 | cascade sync input/backplane output |

## FUNCTIONAL DESCRIPTION

### Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to $V_{SS}$. Line A0 is defined as HIGH (logic 1) when connected to $V_{DD}$.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to $V_{SS}$ or $V_{DD}$ respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to $V_{SS}$ or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to $V_{DD}$.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

# PLL FREQUENCY SYNTHESIZER

The integrated circuit SAA1056P together with a suitable prescaler (e.g. SAA1059) and a loop filter forms a complete PLL frequency synthesizer for AM/FM radio tuning systems.

**Features**

- Bus control for the selection of 17-bit words.
- 17-bit latch, for data storage.
- Control lines TTL compatible by means of level shifters.
- Decoupled oscillator frequency output (system clock for other ICs).
- Choice of 4 reference frequencies.

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage ranges | $V_{DD}$ | 8 to 10 | V |
| | $V_{DDI}$ | 4,5 to 5,5 | V |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 80 | °C |
| Maximum input frequency | $f_i$ | 4 | MHz |

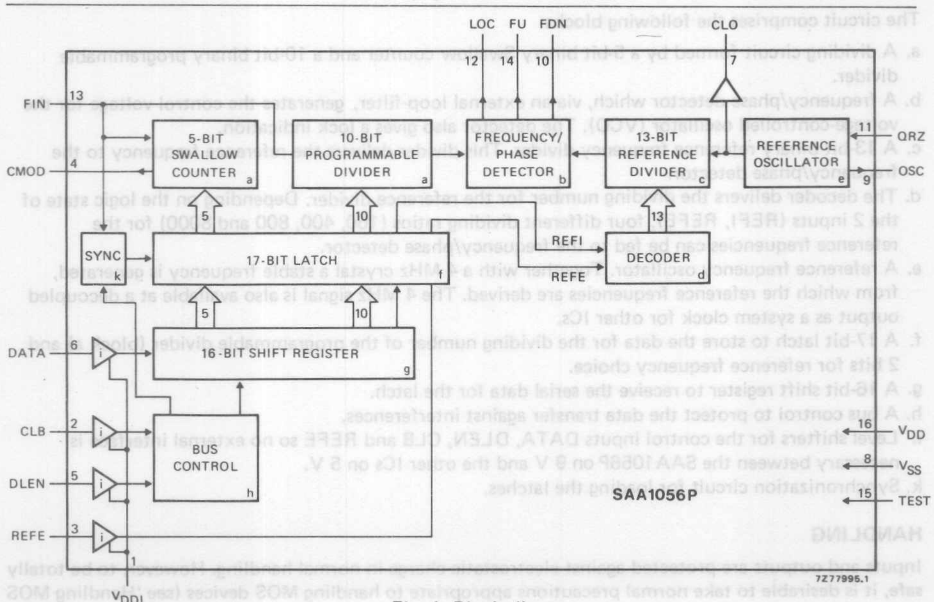



Fig. 1 Block diagram.

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

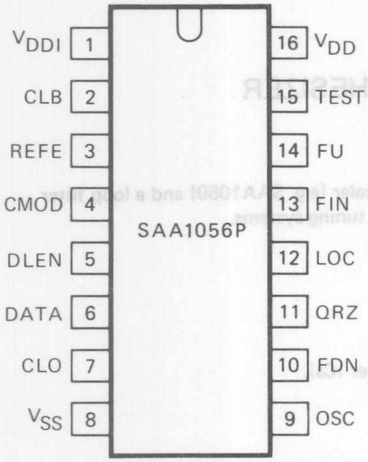



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Fig. 2 Pinning diagram.

**PINNING**

| | | | |
|---|---|---|---|
| 16 | $V_{DD}$ | positive supply | |
| 8 | $V_{SS}$ | ground (0 V) | |
| 1 | $V_{DDI}$ | supply voltage for the level shifters | |

**Inputs**

| | | | |
|---|---|---|---|
| 13 | FIN | input frequency; maximum 4 MHz | |
| 6 | DATA | data input | CBUS |
| 2 | CLB | clock burst | CBUS |
| 5 | DLEN | data line enable | CBUS |
| 3 | REFE | reference frequency selection | |
| 11 | QRZ | quartz crystal input (4 MHz) | |

**Outputs**

| | | |
|---|---|---|
| 4 | CMOD | count mode output for prescaler |
| 12 | LOC | lock detector output |
| 10 | FDN | phase detector output; frequency down |
| 14 | FU | phase detector output; frequency up |
| 7 | CLO | system clock for other ICs (4 MHz) |
| 9 | OSC | quartz crystal oscillator output |

## GENERAL DESCRIPTION

The integrated circuit SAA1056P, together with a suitable prescaler (32/33) and loop-filter, forms a complete synthesizer function for AM/FM radio tuning systems.

The circuit comprises the following blocks:

a. A dividing circuit formed by a 5-bit binary Swallow counter and a 10-bit binary programmable divider.

b. A frequency/phase detector which, via an external loop-filter, generates the control voltage for the voltage-controlled oscillator (VCO). The detector also gives a lock indication.

c. A 13-bit binary reference frequency divider. This divider delivers the reference frequency to the frequency/phase detector.

d. The decoder delivers the dividing number for the reference divider. Depending on the logic state of the 2 inputs (REFI, REFE), four different dividing ratios (160, 400, 800 and 8000) for the reference frequencies can be fed to the frequency/phase detector.

e. A reference frequency oscillator. Together with a 4 MHz crystal a stable frequency is generated, from which the reference frequencies are derived. The 4 MHz signal is also available at a decoupled output as a system clock for other ICs.

f. A 17-bit latch to store the data for the dividing number of the programmable divider (block a) and 2 bits for reference frequency choice.

g. A 16-bit shift register to receive the serial data for the latch.

h. A bus control to protect the data transfer against interferences.

i. Level shifters for the control inputs DATA, DLEN, CLB and REFE so no external interface is necessary between the SAA1056P on 9 V and the other ICs on 5 V.

k. Synchronization circuit for loading the latches.

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage range ($V_{DDI} < V_{DD}$) | $V_{DD}$ | −0,3 to + 15 | V |
| Input voltage range | $V_I$ | −0,3 to + $V_{DD}$ | V |
| Input current (d.c.) | $\pm I_I$ | max. 10 | mA |
| Output current (d.c.) | $\pm I_O$ | max. 10 | mA |
| Current from $V_{DDI}$ to $V_{DD}$ (d.c.) | I | max. 10 | mA |
| Power dissipation per output | $P_O$ | max. 100 | mW |
| Total power dissipation per package | $P_{tot}$ | max. 240 | mW |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 80 | °C |
| Storage temperature range | $T_{stg}$ | −55 to + 150 | °C |

## D.C. CHARACTERISTICS

$V_{SS}$ = 0; $T_{amb}$ = −20 to + 80 °C; unless otherwise specified

| | $V_{DD}$ V | symbol | min. | typ. | max. | | conditions |
|---|---|---|---|---|---|---|---|
| Supply voltages | – | $V_{DD}$ | 8 | 9 | 10 | V | |
| | – | $V_{DDI}$ | 4,5 | 5 | 5,5 | V | |
| Supply current | 10 | $I_{DD}$ | – | – | 100 | μA | $I_O = 0$; $V_I = V_{DD}$ or $V_{DDI}$ or $V_{SS}$ |
| Inputs without level shifters; FIN, QRZ, TEST | | | | | | | |
| input voltage LOW | 8 to 10 | $V_{IL}$ | 0 | – | 0,3 $V_{DD}$ | V | |
| input voltage HIGH | 8 to 10 | $V_{IH}$ | 0,7 $V_{DD}$ | – | $V_{DD}$ | V | |
| input current HIGH | 10 | $I_{IH}$ | – | – | 1 | μA | $V_I$ = 10 V |
| input current LOW | 10 | $-I_{IL}$ | – | – | 1 | μA | $V_I$ = 0 |
| Inputs with level shifters DATA, CLB, DLEN, REFE at $V_{DDI}$ = 4,5 to 5,5 V | | | | | | | |
| input voltage LOW | 8 to 10 | $V_{IL}$ | 0 | – | 0,2 $V_{DDI}$ | V | |
| input voltage HIGH | 8 to 10 | $V_{IH}$ | 0,8 $V_{DDI}$ | – | $V_{DDI}$ | V | |
| input current HIGH | 10 | $I_{IH}$ | – | – | 1 | μA | $V_I = V_{DDI}$ |
| input current LOW | 10 | $-I_{IL}$ | – | – | 1 | μA | $V_I$ = 0 |
| Output CMOD open-drain, n-channel | | | | | | | |
| output voltage LOW | 8 to 10 | $V_{OL}$ | – | – | 0,5 | V | $I_{OL}$ = 5,5 mA |
| output leakage current | 10 | $I_{OR}$ | – | – | 20 | μA | $V_O$ = 10 V |
| Outputs LOC, FU, FDN | | | | | | | |
| output voltage HIGH | 8 to 10 | $V_{OH}$ | $V_{DD}$−0,5 | – | – | V | $-I_O$ = 2,5 mA |
| output voltage LOW | 8 to 10 | $V_{OL}$ | – | – | 0,5 | V | $I_O$ = 5,5 mA |
| Output OSC | | | | | | | |
| output voltage HIGH | 8 to 10 | $V_{OH}$ | $V_{DD}$−1 | – | – | V | $-I_O$ = 1,2 mA; QRZ at $V_{SS}$ |
| output voltage LOW | 8 to 10 | $V_{OL}$ | – | – | 1 | V | $I_O$ = 2 mA; QRZ at $V_{DD}$ |
| Output CLO | | | | | | | |
| output voltage HIGH | 8 to 10 | $V_{OH}$ | $V_{DD}$−1 | – | – | V | $-I_O$ = 1,2 mA |
| output voltage LOW | 8 to 10 | $V_{OL}$ | – | – | 1 | V | $I_O$ = 4 mA |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = −20 to + 80 °C; unless otherwise specified

| | $V_{DD}$ V | symbol | min. | typ. | max. | conditions |
|---|---|---|---|---|---|---|
| Inputs without level shifters; FIN, QRZ | | | | | | |
| input frequency | 8 to 10 | $f_i$ | 4 | – | – MHz | |
| duty factor | 8 to 10 | $\delta$ | 45 | – | 55 % | |
| rise/fall time | 8 to 10 | $t_r$, $t_f$ | – | – | 50 ns | |
| Inputs with level shifter DATA, CLB, DLEN, REFE | | | | | | |
| rise/fall time | 8 to 10 | $t_r$, $t_f$ | – | – | 1 μs | |
| pulse width | – | $t_{WH}$, $t_{WL}$ | 500 | – | – ns | at 0,8 x $V_{DD}$ resp. 0,2 x $V_{DD}$ levels |
| Output CMOD open-drain, n-channel | | | | | | |
| fall time | 8 to 10 | $t_f$ | – | – | 20 ns | $C_L$ = 25 pF; $R_L$ = 1,2 kΩ ± 20% |
| Output CLO | | | | | | |
| pulse period | 8 to 10 | T | 250 | – | – ns | see Figs 3 and 4 |
| pulse width HIGH | – | $t_{WH}$ | 90 | – | – ns | see Figs 3 and 4 |
| pulse width LOW | – | $t_{WL}$ | 90 | – | – ns | see Figs 3 and 4 |
| Output LOC, FU, FDN | | | | | | |
| rise/fall time | 8 to 10 | $t_r$, $t_f$ | – | – | 20 ns | $C_L$ = 25 pF; $R_L$ = 10 kΩ ± 10% |

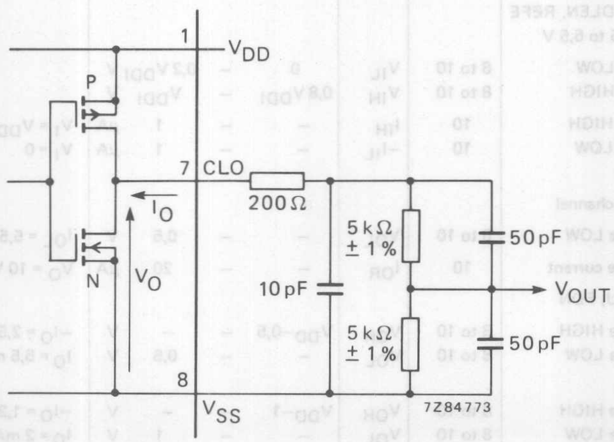



Fig. 3 Output CLO test circuit.

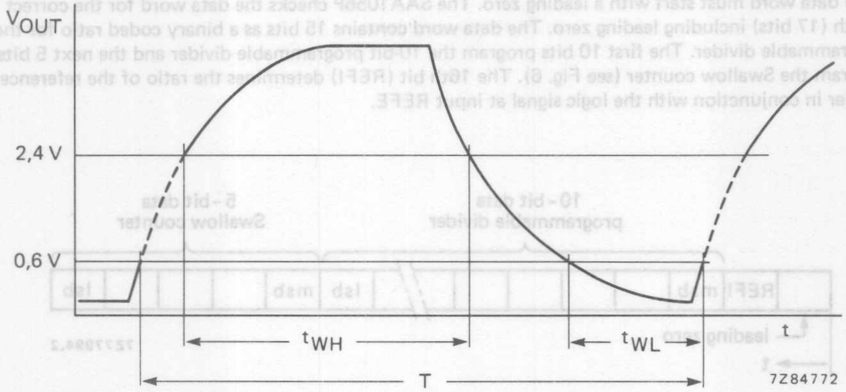



Fig. 4 Output voltage ($V_{OUT}$) of Fig. 3 as a function of time.

## OPERATION DESCRIPTION

### Data inputs (DLEN and DATA)

The SAA1056P accepts the serial 17-bit data word synchronized with the clock burst (CLB), are offered at the data input DATA. However, a command is accepted only when the data line enable input DLEN is HIGH at the same time.

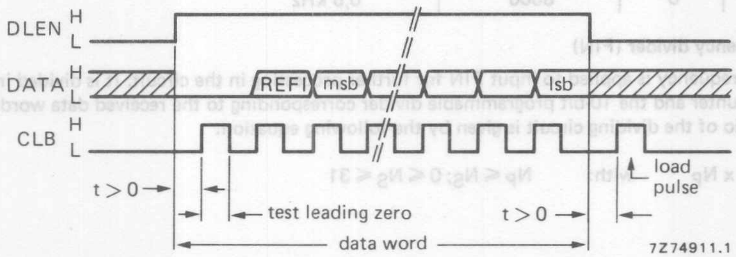



Fig. 5 Pulse diagram of the 17-bit data word.

OPERATION DESCRIPTION (continued)

Each data word must start with a leading zero. The SAA1056P checks the data word for the correct length (17 bits) including leading zero. The data word contains 15 bits as a binary coded ratio for the programmable divider. The first 10 bits program the 10-bit programmable divider and the next 5 bits program the Swallow counter (see Fig. 6). The 16th bit (REFI) determines the ratio of the reference divider in conjunction with the logic signal at input REFE.

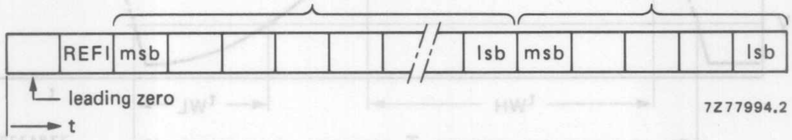



Fig. 6 Organization of a data word.

**Setting the reference divider** (input REFE and control-bit REFI)

The reference divider can be set to four different ratios, using the two signals REFE and REFI.

| control bit REFI | input REFE | dividing ratio $N_{ref}$ | reference frequency at $f_{osc}$ = 4 MHz; $f_{ref}$ |
|---|---|---|---|
| 1 | 1 | 160 | 25 kHz |
| 1 | 0 | 400 | 10 kHz |
| 0 | 1 | 800 | 5 kHz |
| 0 | 0 | 8000 | 0,5 kHz |

**Input frequency divider** (FIN)

The input frequency is applied to input FIN for further processing in the circuit. It is divided in the Swallow counter and the 10-bit programmable divider corresponding to the received data word. The division ratio of the dividing circuit is given by the following equation:

$N = N_S + P \times N_P$ with: $N_P \leqslant N_S$; $0 \leqslant N_S \leqslant 31$

in which:

N = division ratio of total divider
$N_S$ = value for the Swallow counter
P = lowest division ratio of prescaler
$N_P$ = division ratio of the 10-bit programmable divider.

In combination with the 32/33 divider (SAA1059), the minimum and maximum dividing number can be calculated:

$$N_{min} = 0 + 32 \times 31 = 992$$
$$N_{max} = 31 + 32 \times 1023 = 32\,767$$

**Count mode output for prescaler** (CMOD)

Depending on the received data word, the 5-bit Swallow counter generates a signal for setting the prescaler.

0 = divide by low dividing number
1 = divide by high dividing number.

The signal appears about 150 ns after the input pulse FIN (see Fig. 7).

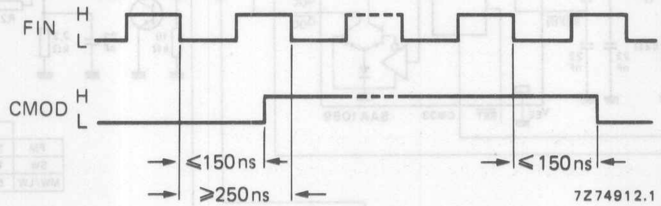



Fig. 7 Timing of the CMOD signal.

**Phase detector (frequency up/down) and lock detector outputs** (FDN, FU, LOC)

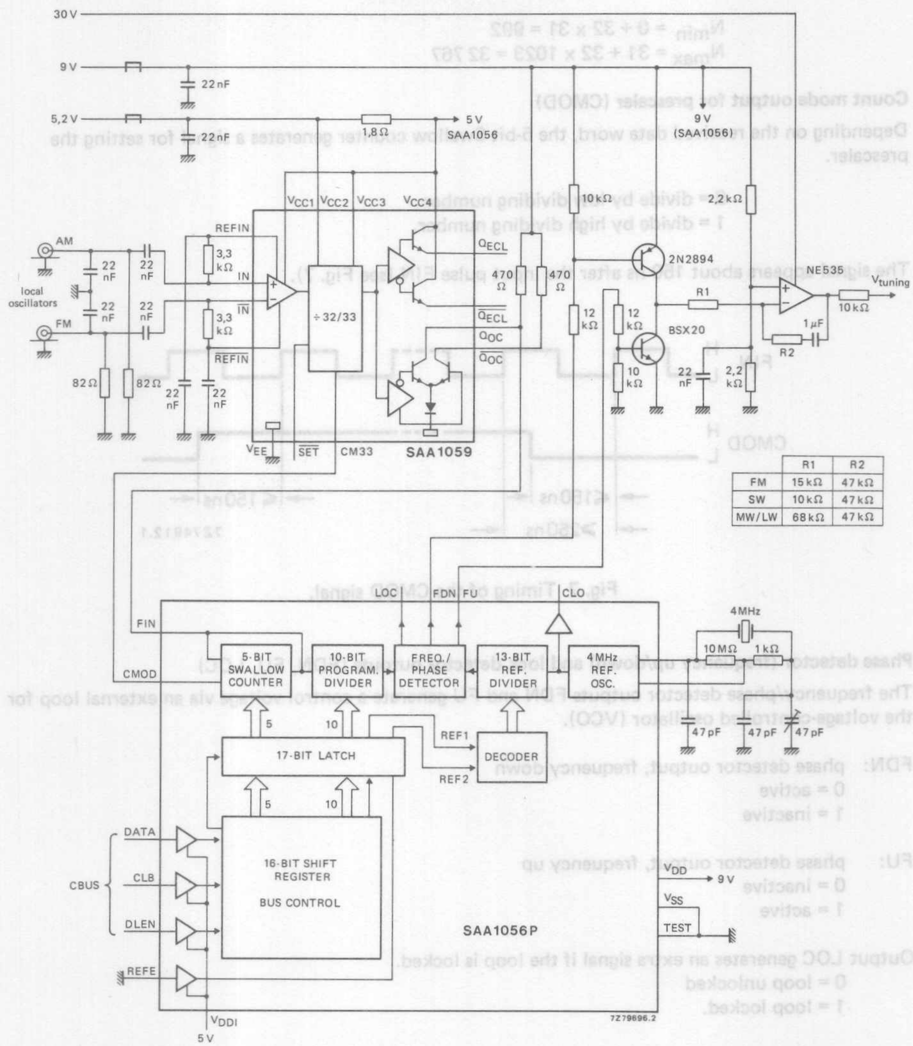
The frequency/phase detector outputs FDN and FU generate a control voltage via an external loop for the voltage-controlled oscillator (VCO).

FDN: phase detector output, frequency down
0 = active
1 = inactive

FU: phase detector output, frequency up
0 = inactive
1 = active

Output LOC generates an extra signal if the loop is locked.
0 = loop unlocked
1 = loop locked.

## APPLICATION INFORMATION




| | R1 | R2 |
|---|---|---|
| FM | 15 kΩ | 47 kΩ |
| SW | 10 kΩ | 47 kΩ |
| MW/LW | 68 kΩ | 47 kΩ |

Fig. 8 A practical digital frequency synthesizer for a radio receiver.

# RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in $I^2L$ technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

**Features**

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

**QUICK REFERENCE DATA**

| | | | |
|---|---|---|---|
| Supply voltage ranges | $V_{CC1}$ | | 3,6 to 12 V |
| | $V_{CC2}$ | | 3,6 to 12 V |
| | $V_{CC3}$ | | $V_{CC2}$ to 31 V |
| Supply currents | $I_{CC1} + I_{CC2}$ | typ. | 18 mA |
| | $I_{CC3}$ | typ. | 0,8 mA |
| Input frequency ranges | | | |
| at pin FAM | $f_{FAM}$ | | 512 kHz to 32 MHz |
| at pin FFM | $f_{FFM}$ | | 70 to 120 MHz |
| Maximum crystal input frequency | $f_{XTAL}$ | > | 4 MHz |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 80 °C |

**PACKAGE OUTLINE**

18-lead DIL; plastic (SOT-102HE).

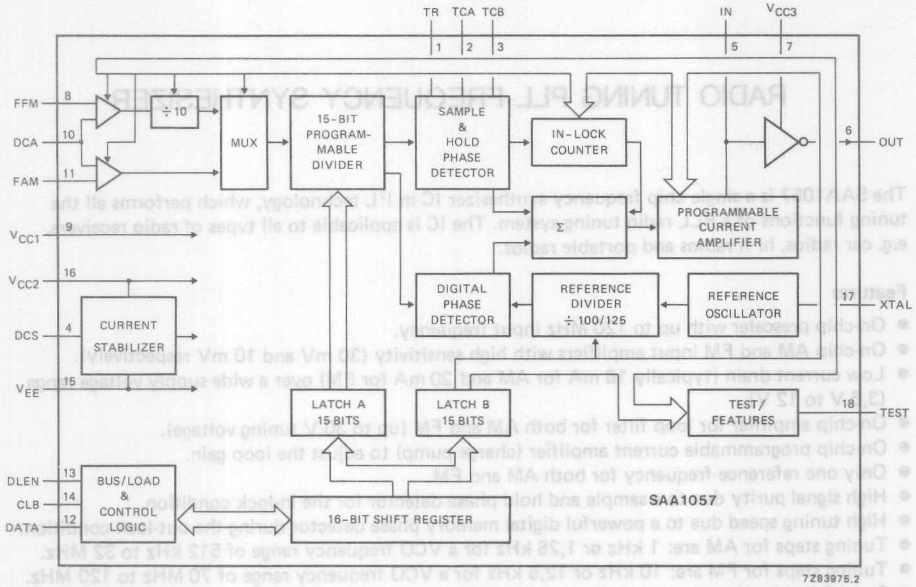



Fig. 1 Block diagram.

## GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

## OPERATION DESCRIPTION

### Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

| | |
|---|---|
| FM | FM/AM selection; '1' = FM, '0' = AM |
| REFH | reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector) |
| CP3<br>CP2<br>CP1<br>CP0 | control bits for the programmable current amplifier (see section Characteristics) |
| SB2 | enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically |
| SLA | load mode of latch A; '1' = synchronous, '0' = asynchronous |
| PDM1<br>PDM0 | phase detector mode |

| PDM1 | PDM0 | digital phase detector |
|---|---|---|
| 0 | X | automatic on/off |
| 1 | 0 | on |
| 1 | 1 | off |

| | |
|---|---|
| BRM | bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on |
| T3 | test bit; must be programmed always '0' |
| T2 | test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin |
| T1 | test bit; must be programmed always '0' |
| T0 | test bit; selects the output of the programmable counter to the TEST pin |

| T3 | T2 | T1 | T0 | TEST (pin 18) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | reference frequency |
| 0 | 0 | 0 | 1 | output programmable counter |
| 0 | 1 | 0 | 1 | output in-lock counter<br>'0' = out-lock<br>'1' = in-lock |

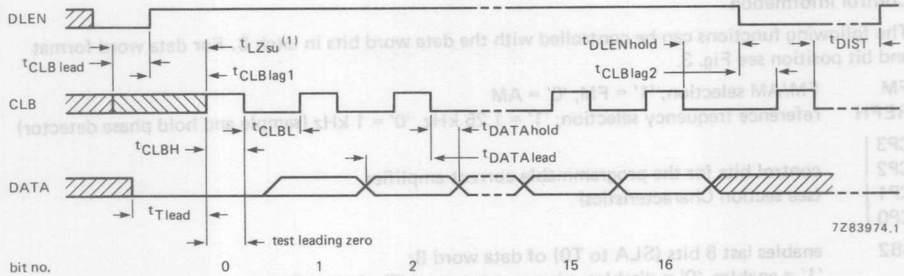



Fig. 2 BUS format.

(1) During the zero set-up time ($t_{LZsu}$) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines.

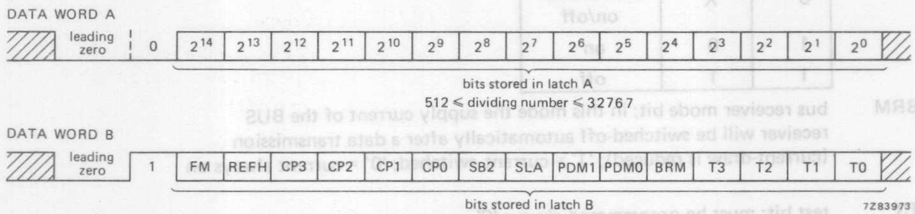



Fig. 3 Bit organization of data words A and B.

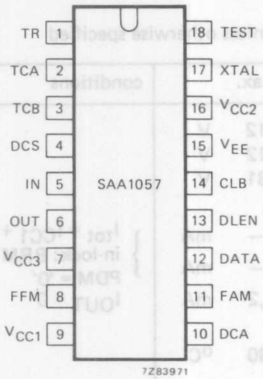



Fig. 4 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | TR | resistor/capacitors for sample and hold circuit |
| 2 | TCA | |
| 3 | TCB | |
| 4 | DCS | decoupling of supply |
| 5 | IN | input of output amplifier |
| 6 | OUT | output of output amplifier |
| 7 | $V_{CC3}$ | positive supply voltage of output amplifier |
| 8 | FFM | FM signal input |
| 9 | $V_{CC1}$ | positive supply voltage of high frequency logic part |
| 10 | DCA | decoupling of input amplifiers |
| 11 | FAM | AM signal input |
| 12 | DATA | BUS |
| 13 | DLEN | |
| 14 | CLB | |
| 15 | $V_{EE}$ | ground |
| 16 | $V_{CC2}$ | positive supply voltage of low frequency logic part and analogue part |
| 17 | XTAL | reference oscillator input |
| 18 | TEST | test output |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage; logic and analogue part | $V_{CC1}$; $V_{CC2}$ | −0,3 to 13,2 V |
| Supply voltage; output amplifier | $V_{CC3}$ | $V_{CC2}$ to + 32 V |
| Total power dissipation | $P_{tot}$ | max. 800 mW |
| Operating ambient temperature range | $T_{amb}$ | −30 to + 85 °C |
| Storage temperature range | $T_{stg}$ | −65 to + 150 °C |

## CHARACTERISTICS

$V_{EE}$ = 0 V; $V_{CC1}$ = $V_{CC2}$ = 5 V; $V_{CC3}$ = 30 V; $T_{amb}$ = 25 $^oC$; unless otherwise specified

| | symbol | min. | typ. | max. | | conditions |
|---|---|---|---|---|---|---|
| Supply voltages | $V_{CC1}$ | 3,6 | 5 | 12 | V | |
| | $V_{CC2}$ | 3,6 | 5 | 12 | V | |
| | $V_{CC3}$ | $V_{CC2}$ | – | 31 | V | |
| Supply currents* | | | | | | |
| AM mode | $I_{tot}$ | – | 16 | – | mA | $I_{tot} = I_{CC1} + I_{CC2}$ |
| FM mode | $I_{tot}$ | – | 20 | – | mA | in-lock: BRM = '1'; PDM = '0' |
| | $I_{CC3}$ | 0,3 | 0,8 | 1,2 | mA | $I_{OUT}$ = 0 |
| Operating ambient temperature | $T_{amb}$ | –25 | – | + 80 | $^oC$ | |
| **RF inputs** (FAM, FFM) | | | | | | |
| AM input frequency | $f_{FAM}$ | 512 kHz | – | 32 | MHz | |
| FM input frequency | $f_{FFM}$ | 70 | – | 120 | MHz | |
| Input voltage at FAM | $V_{i\ (rms)}$ | 30 | – | 500 | mV | |
| Input voltage at FFM | $V_{i\ (rms)}$ | 10 | – | 500 | mV | |
| Input resistance at FAM | $R_i$ | – | 2 | – | kΩ | |
| Input resistance at FFM | $R_i$ | – | 135 | – | Ω | |
| Input capacitance at FAM | $C_i$ | – | 3,5 | – | pF | |
| Input capacitance at FFM | $C_i$ | – | 3 | – | pF | |
| Voltage ratio allowed between selected and non-selected input | $V_s/V_{ns}$ | – | –30 | – | dB | |
| **Crystal oscillator** (XTAL) | | | | | | see note 1 |
| Maximum input frequency | $f_{XTAL}$ | 4 | – | – | MHz | |
| Crystal series resistance | $R_s$ | – | – | 150 | Ω | |
| **BUS inputs** (DLEN, CLB, DATA) | | | | | | |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V | |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | $V_{CC1}$ | V | |
| Input current LOW | $-I_{IL}$ | – | – | 10 | μA | $V_{IL}$ = 0,8 V |
| Input current HIGH | $I_{IH}$ | – | – | 10 | μA | $V_{IH}$ = 2,4 V |

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

## CHARACTERISTICS (continued)

$V_{EE}$ = 0 V; $V_{CC1}$ = $V_{CC2}$ = 5 V; $V_{CC3}$ = 30 V; $T_{amb}$ = 25 °C; unless otherwise specified

| | symbol | min. | typ. | max. | | conditions |
|---|---|---|---|---|---|---|
| **BUS inputs timing** (DLEN, CLB, DATA) | | | | | | see also Fig. 2 and note 2 |
| Lead time for CLB to DLEN | $t_{CLBlead}$ | 1 | – | – | μs | |
| Lead time for DATA to the first CLB pulse | $t_{Tlead}$ | 0,5 | – | – | μs | |
| Set-up time for DLEN to CLB | $t_{CLBlag1}$ | 5 | – | – | μs | |
| CLB pulse width HIGH | $t_{CLBH}$ | 5 | – | – | μs | |
| CLB pulse width LOW | $t_{CLBL}$ | 5 | – | – | μs | |
| Set-up time for DATA to CLB | $t_{DATAlead}$ | 2 | – | – | μs | |
| Hold time for DATA to CLB | $t_{DATAhold}$ | 0 | – | – | μs | |
| Hold time for DLEN to CLB | $t_{DLENhold}$ | 2 | – | – | μs | |
| Set-up time for DLEN to CLB load pulse | $t_{CLBlag2}$ | 2 | – | – | μs | |
| Busy time from load pulse to next start of transmission | $t_{DIST}$ | 5 | – | – | μs | next transmission after word 'B' to other device or |
| Busy time asynchronous mode | $t_{DIST}$ | 0,3 | – | – | ms | next transmission to SAA1057 after word 'A' (see also note 5) |
| synchronous mode | $t_{DIST}$ | 1,3 | – | – | ms | |
| **Sample and hold circuit** (TR, TCA, TCB) | | | | | | see also notes 3; 4 |
| Minimum output voltage | $V_{TCA}$, $V_{TCB}$ | – | 1,3 | – | V | |
| Maximum output voltage | $V_{TCA}$, $V_{TCB}$ | – | – | $V_{CC2}$–0,7 | V | |
| Capacitance at TCA (external) | $C_{TCA}$ | – | – | 2,2 | nF | REFH = '1' |
| | $C_{TCA}$ | – | – | 2,7 | nF | REFH = '0' |
| Discharge time at TCA | $t_{dis}$ | – | – | 5 | μs | REFH = '1' |
| | $t_{dis}$ | – | – | 6,25 | μs | REFH = '0' |
| Resistance at TR | $R_{TR}$ | 100 | – | – | Ω | external |
| Voltage at TR during discharge | $V_{TR}$ | – | 0,7 | – | V | |
| Capacitance at TCB | $C_{TCB}$ | – | – | 10 | nF | external |
| Bias current into TCA, TCB | $I_{bias}$ | – | – | 10 | nA | in-lock |

**CHARACTERISTICS** (continued)

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | symbol | min. | typ. | max. | | conditions |
|---|---|---|---|---|---|---|
| **Programmable current amplifier** (PCA) | | | | | | |
| Output current of the dig. phase detector | $\pm I_{dig}$ | – | 0,4 | – | mA | |
| Current gain of PCA | | | | | | |
| CP3 CP2 CP1 CP0 | | | | | | |
| P1 0 0 0 0 | $G_{P1}$ | – | 0,023 | – | | $V_{CC2} \geqslant 5$ V (only for P1) |
| P2 0 0 0 1 | $G_{P2}$ | – | 0,07 | – | | |
| P3 0 0 1 0 | $G_{P3}$ | – | 0,23 | – | | |
| P4 0 1 1 0 | $G_{P4}$ | – | 0,7 | – | | |
| P5 1 1 1 0 | $G_{P5}$ | – | 2,3 | – | | |
| Ratio between the output current of S/H into PCA and the voltage on $C_{TCB}$ | $S_{TCB}$ | – | 1,0 | – | μA/V | |
| Offset voltage on TCB | $\Delta V_{TCB}$ | – | – | 1 | V | in-lock |
| **Output amplifier** (IN,OUT) | | | | | | |
| Input voltage | $V_{IN}$ | – | 1,3 | – | V | in-lock; equal to internal reference voltage |
| Output voltages | | | | | | |
| minimum | $V_{OUT}$ | – | – | 0,5 | V | $-I_{OUT} = 1$ mA |
| maximum | $V_{OUT}$ | $V_{CC3}-2$ | – | – | V | $I_{OUT} = 1$ mA |
| maximum | $V_{OUT}$ | $V_{CC3}-1$ | – | – | V | $I_{OUT} = 0{,}1$ mA |
| Maximum output current | $\pm I_{OUT}$ | 5 | – | – | mA | $V_{OUT} = ½ V_{CC3}$ |
| **Test output** (TEST)* | | | | | | |
| Output voltage LOW | $V_{TL}$ | – | – | 0,5 | V | |
| Output voltage HIGH | $V_{TH}$ | – | – | 12 | V | |
| Output current OFF | $I_{Toff}$ | – | – | 10 | μA | $V_{TH}$ |
| Output current ON | $I_{Ton}$ | 150 | – | – | μA | $V_{TL}$ |
| **Ripple rejection**** | | | | | | |
| at $f_{ripple} = 100$ Hz | | | | | | |
| $\Delta V_{CC1}/\Delta V_{OUT}$ | | – | 77 | – | dB | |
| $\Delta V_{CC2}/\Delta V_{OUT}$ | | – | 70 | – | dB | |
| $\Delta V_{CC3}/\Delta V_{OUT}$ | | – | 60 | – | dB | $V_{OUT} \leqslant V_{CC3}-3$ V |

* Open collector output.

** Measured in Fig. 6.

## NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

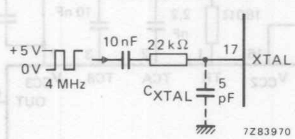



Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ $V_{CC2}$+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ $V_{CC2}$+0,3 V.
4. Crystal oscillator frequency $f_{XTAL}$ = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

## APPLICATION INFORMATION

### Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

### Synchronous/asynchronous operation

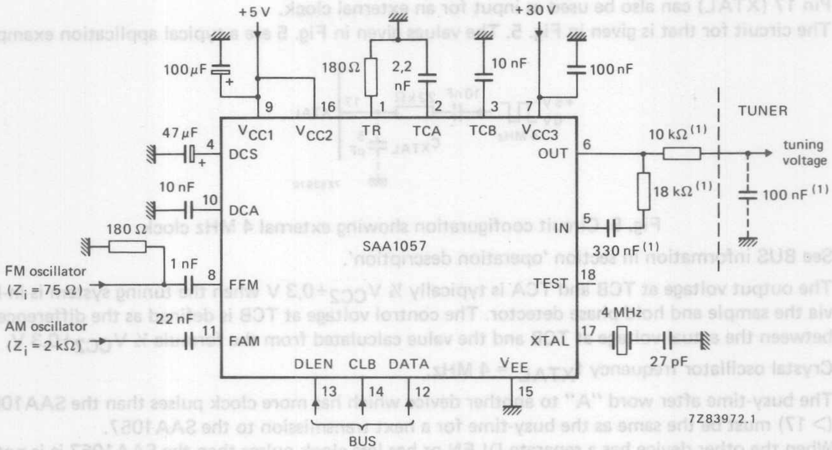
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

### Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage $V_{CC2}$ is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

### Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.




(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

# LED DISPLAY/INTERFACE CIRCUIT

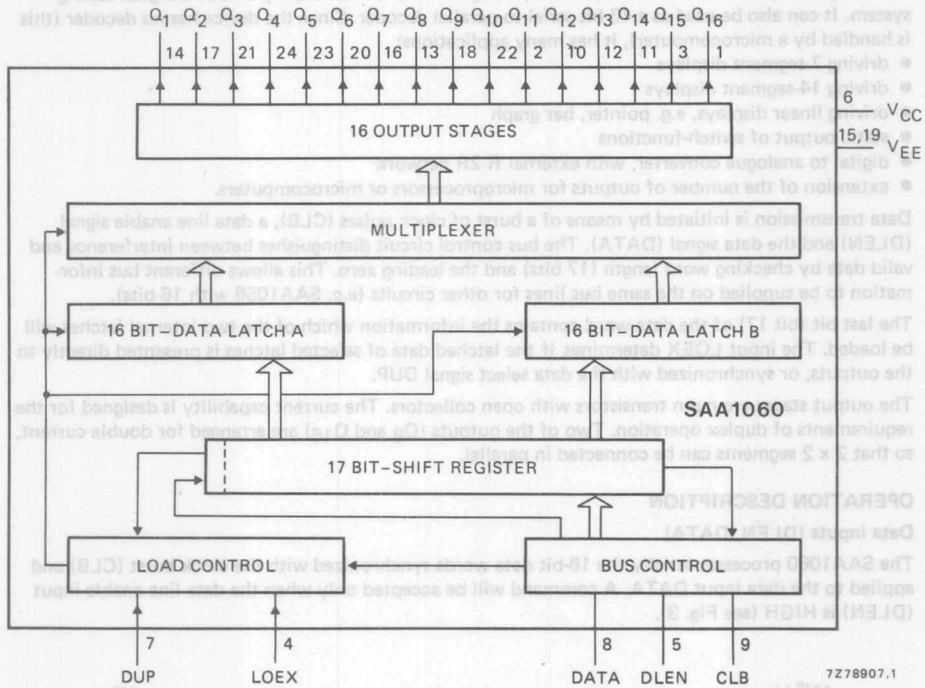



Fig.1 Block diagram.

**Features**

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 4 to 6 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 80 | °C |
| Maximum input frequency | $f_I$ | typ. | 50 | kHz |
| Supply current | $I_{CC}$ | typ. | 60 | mA |
| Output current | $I_Q$ | < | 40 | mA |
| Output current ($Q_8$ and $Q_{16}$ only) | $I_Q$ | < | 80 | mA |

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

## GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs ($Q_8$ and $Q_{16}$) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

## OPERATION DESCRIPTION

### Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

16th bit … 1st bit

| load bit | P $Q_{16}$ | O $Q_{15}$ | N $Q_{14}$ | M $Q_{13}$ | L $Q_{12}$ | K $Q_{11}$ | J $Q_{10}$ | I $Q_9$ | H $Q_8$ | G $Q_7$ | F $Q_6$ | E $Q_5$ | D $Q_4$ | C $Q_3$ | B $Q_2$ | A $Q_1$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

leading zero

7Z78909

Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# LCD DISPLAY/INTERFACE CIRCUIT

## GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

### Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 4,2 to 5,5 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |
| Maximum input frequency | $f_i$ | typ. | 50 | kHz |
| Supply current | $I_{CC}$ | typ. | 3,5 | mA |
| Output current ($Q_1$ to $Q_{20}$) | $I_Q$ | > | 60 | $\mu$A |

## PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

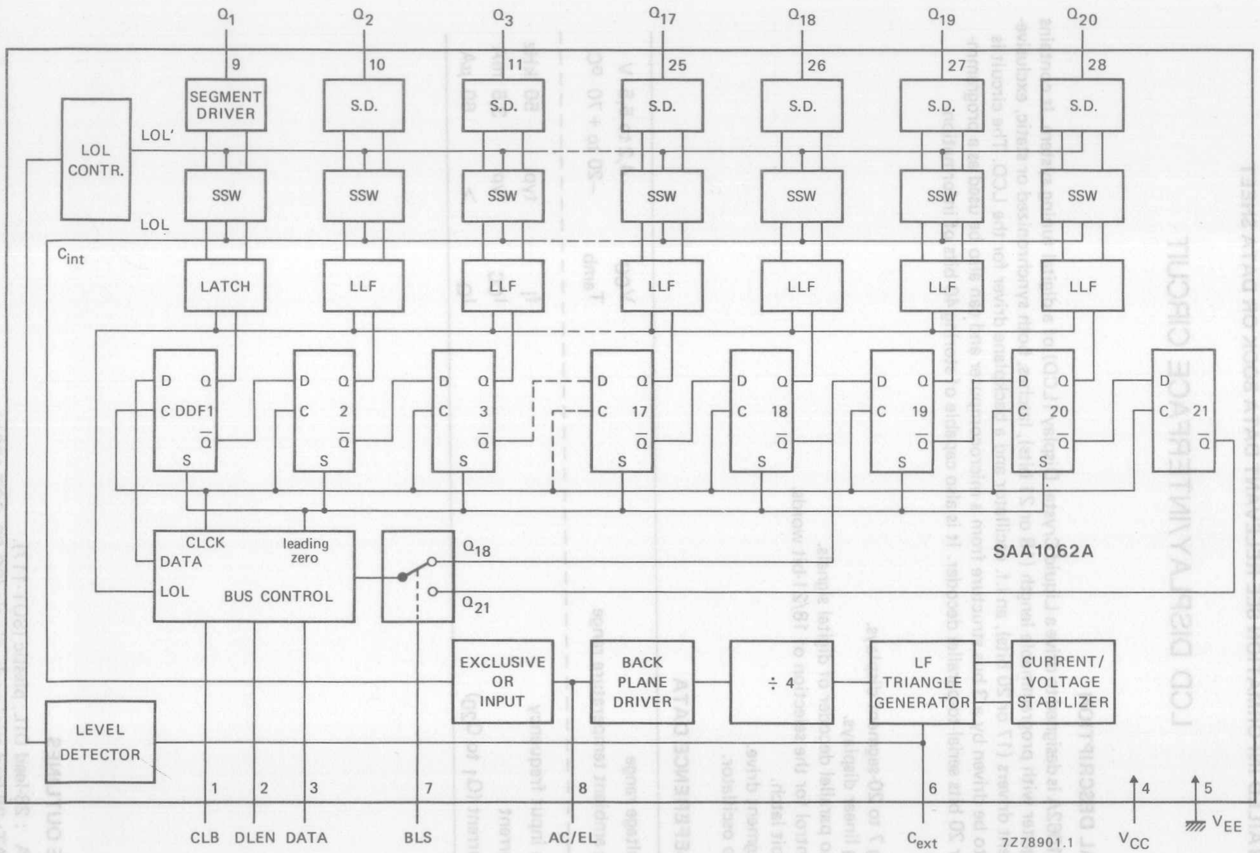



Fig. 1 Block diagram.

# FLUORESCENT DISPLAY/INTERFACE CIRCUIT

## GENERAL DESCRIPTION

The SAA1063 is designed to drive the display unit of a digital tuning system. It contains a 17-bit shift register, latches, display multiplexers and output stages, capable of driving 4½ decades of a 7 segment fluorescent display in duplex mode. The decoding for the display is carried out in the data input (microcomputer).

### Features

- Driving 4½ decades of a seven segment display in duplex mode.
- Microcomputer compatible.
- 17-bit shift register.
- D.C. and duplex operation.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 4 to 5,5 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +80 | °C |
| Maximum input frequency | $f_i$ | min. | 50 | kHz |
| Supply current | $I_{CC}$ | typ. | 20 | mA |
| Output current | $I_Q$ | max. | 1,5 | mA |
| Maximum output voltage swing | $V_{Qmax}$ | min. | 34,5 | V |

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

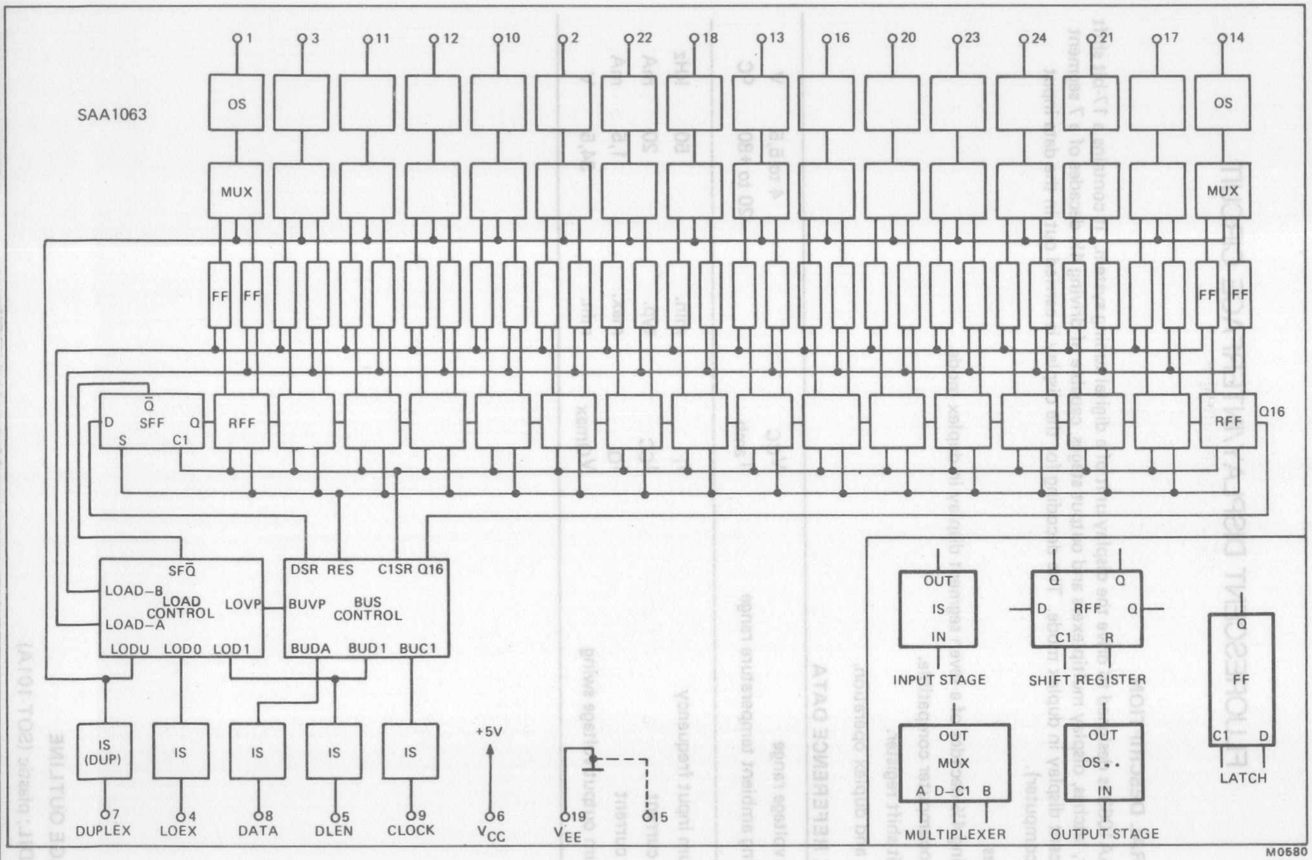



Fig. 1 Block diagram.
Insert indicates structure of logic elements.

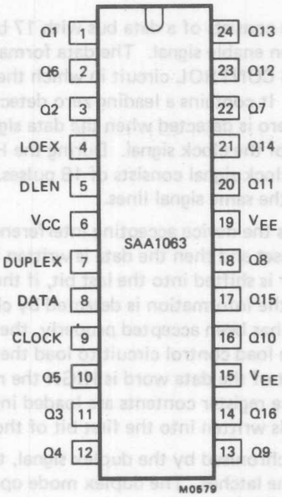



Fig. 2 Pinning diagram.

## PINNING

| | | | | | |
|---|---|---|---|---|---|
| 1. | Q1 | | 13. | Q9 | segment drive outputs |
| 2. | Q6 | segment drive outputs | 14. | Q16 | |
| 3. | Q2 | | 15. | $V_{EE}$ | ground |
| 4. | LOEX | mode selection | 16. | Q10 | |
| 5. | DLEN | bus enable | 17. | Q15 | segment drive outputs |
| 6. | $V_{CC}$ | +5 V power supply | 18. | Q8 | |
| 7. | DUPLEX | duplex input | 19. | $V_{EE}$ | ground |
| 8. | DATA | data input | 20. | Q11 | |
| 9. | CLOCK | bus clock input | 21. | Q14 | |
| 10. | Q5 | | 22. | Q7 | segment drive outputs |
| 11. | Q3 | segment drive outputs | 23. | Q12 | |
| 12. | Q4 | | 24. | Q13 | |

## OPERATION DESCRIPTION

The input information for this device consists of a data bus with 17 bit words, an external clock synchronized with the data bus and an enable signal. The data format of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is taken as to whether these signals are valid for this device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal HIGH, during the first HIGH period of the clock signal. During the HIGH period of the DLEN signal, the length control determines if the clock signal consists of 18 pulses. This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device accepting interference on the signal lines. If leading zero is detected the shift register is reset and then the data is written into this register. The reset position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input is correct. Incorrect length of the information is detected by checking the value of the last bit of the register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOVP). This pulse enables the load control circuit to load the contents of the register into one of the two latches. When the load bit of the data word is HIGH the register contents are loaded into latch A; when this load bit is LOW the register contents are loaded into latch B. When the data information is accepted this load bit is written into the first bit of the shift register.

In duplex mode the load pulse is synchronised by the duplex signal, to avoid current transients in the output stages during the loading of the latches. The duplex mode operates in one of two mode conditions. When LOEX (pin 4) is LOW the duplex mode condition is selected; when LOEX is HIGH the d.c. mode condition is selected. The output stages are switched to the contents of latch A and latch B respectively.

When the duplex input (pin 7) is LOW the contents of latch A can be found on the output, when this input is HIGH the contents of latch B are found on the output.

In the duplex mode condition the output stages are capable of driving 32 duplexed segments of a fluorescent display. However, in the d.c. mode condition the output stages can only drive 16 segments of the display and two SAA1063 devices are required to drive a 4½ decade display unit.

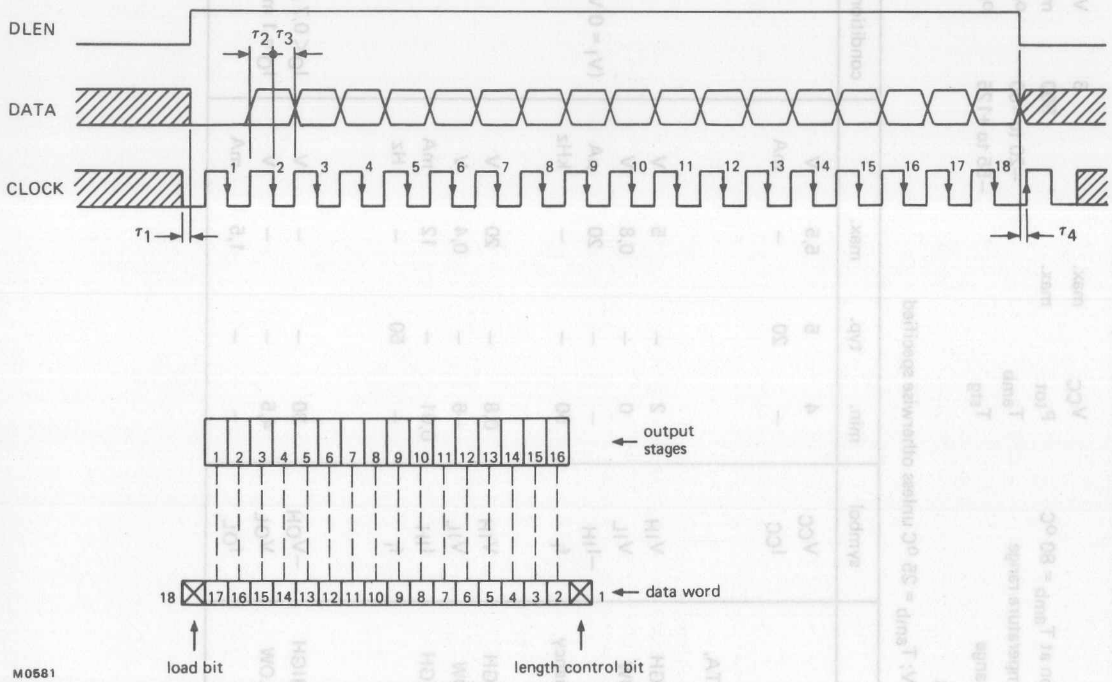



Fig. 3 Organisation of 18-bit data word.

## Notes

1. The display segment is blanked by a HIGH data bit.
2. In duplex mode the period between the two data words must be greater than 21 ms.
3. Shaded timing periods are 'don't care' levels.
4. $\tau_1 > 4\ \mu s$ if a continuous clock is used. $\tau_2$ and $\tau_3 > 4\ \mu s$. $\tau_4 > 2\ \mu s$.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | max. | 6 | V |
| Total power dissipation at $T_{amb}$ = 80 °C | $P_{tot}$ | max. | 900 | mW |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +80 | °C |
| Storage temperature range | $T_{stg}$ | | −55 to +125 | °C |

## CHARACTERISTICS

$V_{EE}$ = 0 V; $V_{CC}$ = 5 V; $T_{amb}$ = 25 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | | conditions |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4 | 5 | 5,5 | V | |
| Supply current | $I_{CC}$ | – | 20 | – | mA | |
| **Inputs** | | | | | | |
| LOEX, DLEN, DATA, CLOCK | | | | | | |
| input voltage HIGH | $V_{IH}$ | 2 | – | 5 | V | |
| input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V | |
| input current | $-I_{IH}$ | – | – | 20 | μA | ($V_I$ = 0 V) |
| max. input frequency | $f_i$ | 50 | – | – | kHz | |
| DUPLEX | | | | | | |
| input voltage HIGH | $V_{IH}$ | 0,8 | – | 20 | V | |
| input voltage LOW | $V_{IL}$ | −6 | – | 0,4 | V | |
| input current HIGH | $I_{IH}$ | 0,01 | – | 12 | mA | |
| input frequency | $f_i$ | – | 50 | – | Hz | |
| **Outputs** | | | | | | |
| Q1 to Q16 | | | | | | |
| output voltage HIGH | $-V_{OH}$ | 30 | – | – | V | $I_O$ < 0,7 μA |
| output voltage LOW | $V_{OL}$ | 4,5 | – | – | V | $I_O$ = 1 mA |
| output current | $I_{OL}$ | – | – | 1,5 | mA | |

# MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

## GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

### Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

### Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 18) | $V_{DD}$ | typ. | 5 | V |
| Supply current (pin 18) | $I_{DD}$ | typ. | 55 | mA |
| Reference current (pin 6) | $I_{ref}$ | typ. | 250 | $\mu$A |
| Total power dissipation | $P_{tot}$ | | 450 | mW |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 | $^{o}$C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

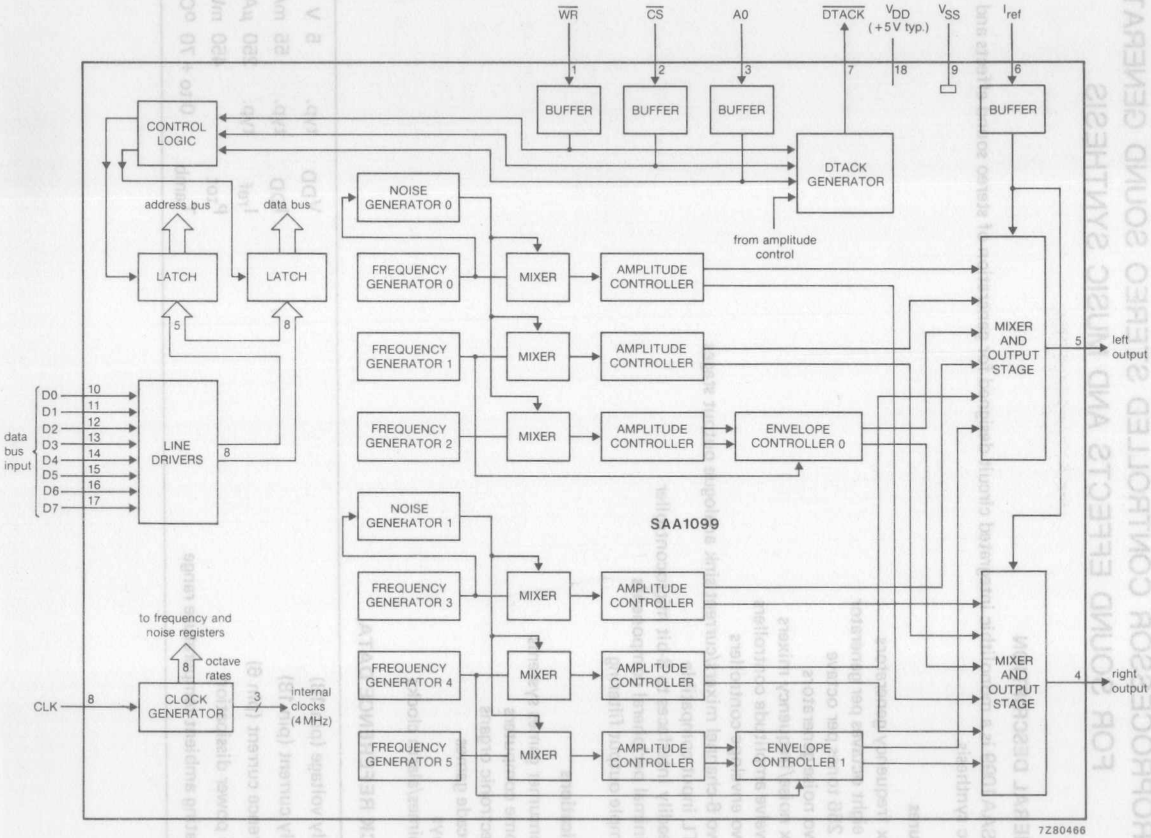



Fig. 1 Block diagram.

## PINNING

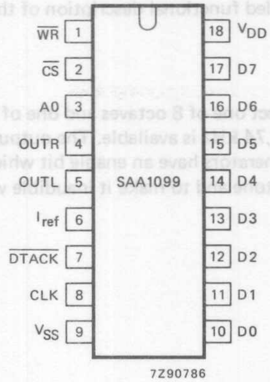



Fig. 2 Pinning diagram.

## PIN DESIGNATION

| | | |
|---|---|---|
| 1 | $\overline{WR}$ | **Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers. |
| 2 | $\overline{CS}$ | **Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers. |
| 3 | A0 | **Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1). |
| 4 | OUTR | **Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor. |
| 5 | OUTL | **Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor. |
| 6 | $I_{ref}$ | **Reference current supply**: used to bias the current sink outputs. |
| 7 | $\overline{DTACK}$ | **Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive. |
| 8 | CLK | **Clock**: input for an externally generated clock at a nominal frequency of 8 MHz. |
| 9 | $V_{SS}$ | **Ground**: 0 V. |
| 10-17 | D0-D7 | **Data**: Data bus input. |
| 18 | $V_{DD}$ | **Power supply**: + 5 V typical. |

DEVELOPMENT DATA

## FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

### Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 30 Hz to 7,74 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone tone and to make it inaudible when required.

The frequency ranges per octave are:

| Octave | Frequency range |
|---|---|
| 0 | 30 Hz to 60 Hz |
| 1 | 60 Hz to 122 Hz |
| 2 | 122 Hz to 244 Hz |
| 3 | 244 Hz to 488 Hz |
| 4 | 489 Hz to 976 Hz |
| 5 | 978 Hz to 1,95 kHz |
| 6 | 1,95 kHz to 3,90 kHz |
| 7 | 3,91 kHz to 7,81 kHz |

### Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.
In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

### Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

### Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.
When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

### Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

### Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

### Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

### Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 18) | $V_{DD}$ | | −0,3 to + 7,5 V |
| Maximum input voltage | $V_I$ | | −0,3 to + 7,5 V |
| at $V_{DD}$ = 4,5 to 5,5 V | $V_I$ | | −0,5 to + 7,5 V |
| Maximum output current | $I_O$ | max. | 10 mA |
| Total power dissipation | $P_{tot}$ | | 450 mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 125 °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 °C |
| Electrostatic handling* | $V_{es}$ | | −1000 to + 1000 V |

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

## D.C. CHARACTERISTICS

$V_{DD}$ = 5 V; $T_{amb}$ = 0 to 70 °C; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage | $V_{DD}$ | 4,5 | 5,0 | 5,5 | V |
| Supply current | $I_{DD}$ | – | 55 | 90 | mA |
| Reference current (note 1) | $I_{ref}$ | 100 | 250 | 400 | μA |
| **INPUTS** | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | 6,0 | V |
| Input voltage LOW | $V_{IL}$ | –0,5 | | 0,8 | V |
| Input leakage current | $\pm I_{LI}$ | – | – | 10 | μA |
| Input capacitance | $C_I$ | – | – | 10 | pF |
| **OUTPUTS** | | | | | |
| *$\overline{DTACK}$* (open drain; note 2) | | | | | |
| Output voltage LOW at $I_{OL}$ = 3,2 mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Voltage on pin 7 (OFF state) | $V_{7\text{-}9}$ | –0,3 | – | 6,0 | V |
| Output capacitance (OFF state) | $C_O$ | – | – | 10 | pF |
| Load capacitance | $C_L$ | – | – | 150 | pF |
| Output leakage current (OFF state) | $-I_{LO}$ | – | – | 10 | μA |
| **Audio outputs** (pins 4 and 5) | | | | | |
| *With fixed $I_{ref}$* (note 3) | | | | | |
| One channel on | $I_{01}/I_{ref}$ | 90 | – | 125 | % |
| Six channels on | $I_{06}/6xI_{ref}$ | 85 | – | 120 | % |
| *With $I_{ref}$ = 250 μA; $R_L$ = 1,1 kΩ* (± 5%) | | | | | |
| One channel on | $I_{01}/I_{ref}$ | 95 | – | 115 | % |
| Six channels on | $I_{06}/6xI_{ref}$ | 90 | – | 110 | % |
| Output current one channel on | $I_{01}$ | 238 | | 288 | μA |
| Output current six channels on | $I_{06}$ | 1,38 | | 1,65 | mA |
| *With resistor supplying $I_{ref}$* (note 4) | | | | | |
| Output current one channel on | $I_{01}$ | 155 | – | 270 | μA |
| Output current six channels on | $I_{06}$ | 0,94 | – | 1,65 | mA |
| Load resistance | $R_L$ | 600 | | | Ω |
| D.C. leakage current all channels off | $-I_{LO}$ | – | – | 10 | μA |
| Maximum current difference between left and right current sinks (note 5) | $\pm I_{Omax}$ | – | – | 15 | % |
| Signal-to-noise ratio (note 6) | S/N | – | tbf | – | dB |

DEVELOPMENT DATA

## A.C. CHARACTERISTICS

$V_{DD}$ = 5 V; $T_{amb}$ = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Bus interface timing** (see Fig. 3) | | | | | |
| A0 set-up time to $\overline{CS}$ fall | $t_{ASC}$ | 0 | – | | ns |
| $\overline{CS}$ LOW to $\overline{WR}$ fall | $t_{CSW}$ | 30 | – | | ns |
| A0 set-up time to $\overline{WR}$ fall | $t_{ASW}$ | 50 | – | – | ns |
| $\overline{WR}$ LOW time | $t_{WL}$ | 100 | – | – | ns |
| Data bus valid to $\overline{WR}$ rise | $t_{BSW}$ | 100 | – | – | ns |
| $\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7) | $t_{DFW}$ | 0 | – | 85 | ns |
| A0 hold time from $\overline{WR}$ HIGH | $t_{AHW}$ | 0 | – | – | ns |
| $\overline{CS}$ hold time from $\overline{WR}$ HIGH | $t_{CHW}$ | 0 | – | – | ns |
| Data bus hold time from $\overline{WR}$ HIGH | $t_{DHW}$ | 0 | – | – | ns |
| $\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH | $t_{DRW}$ | 0 | – | 100 | ns |
| Bus cycle time (note 8) | $t_{CY}$ | 2CP | – | – | |
| Bus cycle time (note 9) | $t_{CY}$ | 8CP | – | – | |
| **Clock input timing** (see Fig. 4) | | | | | |
| Clock period | $t_{CLK}$ | 120 | 125 | 255 | ns |
| Clock LOW time | $t_{HIGH}$ | 55 | – | – | ns |
| Clock HIGH time | $t_{LOW}$ | 55 | – | – | ns |

**Notes to the characteristics**

1. Using an external constant current generator to provide a nominal $I_{ref}$ or external resistor connected to $V_{DD}$.
2. This output is short-circuit protected to $V_{DD}$ and $V_{SS}$.
3. Measured with $I_{ref}$ a constant value between 100 and 400 $\mu$A; load resistance ($R_L$) allowed to match E24 (5%) in all applications via:

$$R_L = \frac{0,27775 \pm 0,03611}{I_{ref}}.$$

4. Measured with $R_{ref}$ = 10 k$\Omega$ (± 5%) connected between $I_{ref}$ and $V_{DD}$; $R_L$ = 820 $\Omega$ (± 5%); OUTR and OUTL short-circuit protected to $V_{SS}$.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of two clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of eight clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

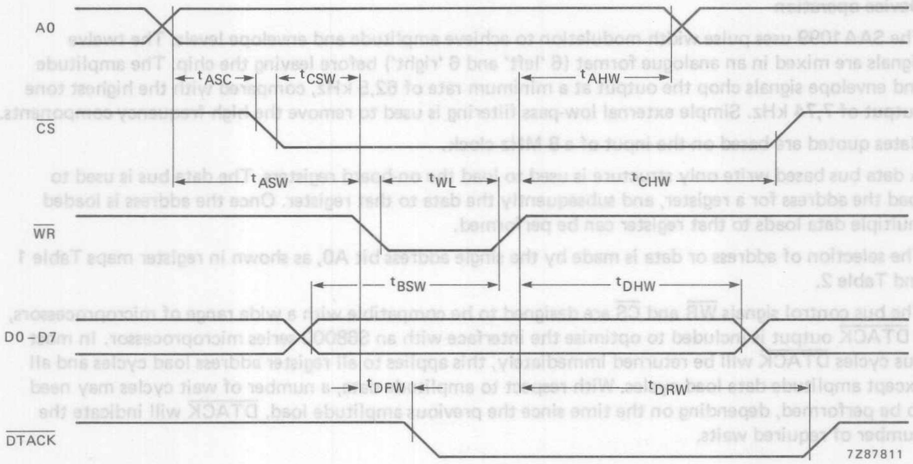



Fig. 3 Bus interface waveforms.

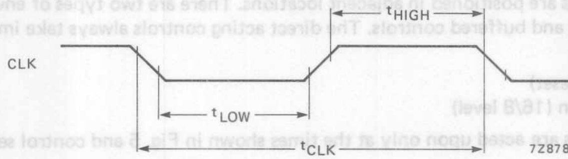



Fig. 4 Clock input waveform.

## APPLICATION INFORMATION

### Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,74 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

**Register description** (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

**Table 1 External memory map**

| select | data bus inputs | | | | | | | | operations |
|---|---|---|---|---|---|---|---|---|---|
| A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | data for internal registers |
| 1 | X | X | X | A4 | A3 | A2 | A1 | A0 | internal register address |

Where X = don't care state.

**Table 2** Internal register map.

| register address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | operations |
|---|---|---|---|---|---|---|---|---|---|
| | data bus inputs | | | | | | | | |
| 00 | AR03 | AR02 | AR01 | AR00 | AL03 | AL02 | AL01 | AL00 | amplitude 0 right channel; left channel |
| 01 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | amplitude 1 right/left |
| 02 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | amplitude 2 right/left |
| 03 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | amplitude 3 right/left |
| 04 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | amplitude 4 right/left |
| 05 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | amplitude 5 right/left |
| 06 | X | X | X | X | X | X | X | X | |
| 07 | X | X | X | X | X | X | X | X | |
| 08 | F07 | F06 | F05 | F04 | F03 | F02 | F01 | F00 | frequency of tone 0 |
| 09 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | frequency of tone 1 |
| 0A | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | frequency of tone 2 |
| 0B | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | frequency of tone 3 |
| 0C | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | frequency of tone 4 |
| 0D | F57 | F56 | F55 | F54 | F53 | F52 | F51 | F50 | frequency of tone 5 |
| 0E | X | X | X | X | X | X | X | X | |
| 0F | X | X | X | X | X | X | X | X | |
| 10 | X | 012 | 011 | 010 | X | 002 | 001 | 000 | octave 1; octave 0 |
| 11 | X | 032 | 031 | 030 | X | 022 | 021 | 020 | octave 3; octave 2 |
| 12 | X | 052 | 051 | 050 | X | 042 | 041 | 040 | octave 5; octave 4 |
| 13 | X | X | X | X | X | X | X | X | |
| 14 | X | X | FE5 | FE4 | FE3 | FE2 | FE1 | FE0 | frequency enable |
| 15 | X | X | NE5 | NE4 | NE3 | NE2 | NE1 | NE0 | noise enable |
| 16 | X | X | N11 | N10 | X | X | N01 | N00 | noise generator 1; noise generator 0 |
| 17 | X | X | X | X | X | X | X | X | |
| 18 | E07 | X | E05 | E04 | E03 | E02 | E01 | E00 | envelope generator 0 |
| 19 | E17 | X | E15 | E14 | E13 | E12 | E11 | E10 | envelope generator 1 |
| 1A | X | X | X | X | X | X | X | X | |
| 1B | X | X | X | X | X | X | X | X | |
| 1C | X | X | X | X | X | X | X | SE | sound enable (all channels) |
| 1D | X | X | X | X | X | X | X | X | |
| 1E | X | X | X | X | X | X | X | X | |
| 1F | X | X | X | X | X | X | X | X | |

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

DEVELOPMENT DATA

## APPLICATION INFORMATION (continued)

**Table 3** Register description

| bit | description |
|---|---|
| ARn3; ARn2;<br>ARn1; ARn0<br>(n = 0,5) | 4 bits for amplitude control<br>of right channel<br>0 0 0 0 minimum amplitude (off)<br>1 1 1 1 maximum amplitude |
| ALn3; ALn2;<br>ALn1; ALn0<br>(n = 0,5) | 4 bits for amplitude control<br>of left channel<br>0 0 0 0 minimum amplitude (off)<br>1 1 1 1 maximum amplitude |
| Fn7 to Fn0<br>(n = 0,5) | 8 bits for frequency control<br>of the six frequency generators<br>0 0 0 0 0 0 0 0 lowest frequency<br>1 1 1 1 1 1 1 1 highest frequency |
| On2; On1; On0<br>(n = 0,5) | 3 bits for octave control<br>0 0 0 lowest octave (30 Hz to 60 Hz)<br>0 0 1 (60 Hz to 122 Hz)<br>0 1 0 (122 Hz to 244 Hz)<br>0 1 1 (244 Hz to 488 Hz)<br>1 0 0 (489 Hz to 976 Hz)<br>1 0 1 (978 Hz to 1,95 kHz)<br>1 1 0 (1,95 kHz to 3,90 kHz)<br>1 1 1 highest octave (3,91 kHz to 7,81 kHz) |
| FEn<br>(n = 0,5) | frequency enable bit (one tone per generator)<br>FEn = 0 indicates that frequency 'n' is off |
| NEn<br>(n = 0,5) | noise enable bit (one tone per generator)<br>NEn = 0 indicates that noise 'n' is off |
| Nn1; Nn0<br>(n = 0,1) | 2 bits for noise generator control.<br>These bits select the noise generator rate (noise 'colour')<br>Nn1 Nn0 clock frequency (kHz)<br>0 0 31,3<br>0 1 15,6<br>1 0 7,6<br>1 1 61 to 15,6 (frequency generator 0/2) |

| bit | description |
|---|---|
| En7;<br>En5 to En0<br>(n = 0,1) | 7 bits for envelope control<br>En0<br>0 left and right component have the same envelope<br>1 right component has inverse of envelope that is applied to left component<br>En3 En2 En1<br>0 0 0 zero amplitude<br>0 0 1 maximum amplitude<br>0 1 0 single decay<br>0 1 1 repetitive decay<br>1 0 0 single triangular<br>1 0 1 repetitive triangular<br>1 1 0 single attack<br>1 1 1 repetitive attack<br>En4<br>0 4 bits for envelope control (maximum frequency = 976 Hz)<br>1 3 bits for envelope control (maximum frequency = 1,95 kHz)<br>En5<br>0 internal envelope clock (frequency generator 1 or 4)<br>1 external envelope clock (address write pulse)<br>En7<br>0 reset (no envelope control)<br>1 envelope control enabled |
| SE | SE sound enable for all channels<br>(reset on power-up to 0)<br>0 all channels disabled<br>1 all channels enabled |

**Note**

All rates given are based on the input of a 8 MHz clock.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

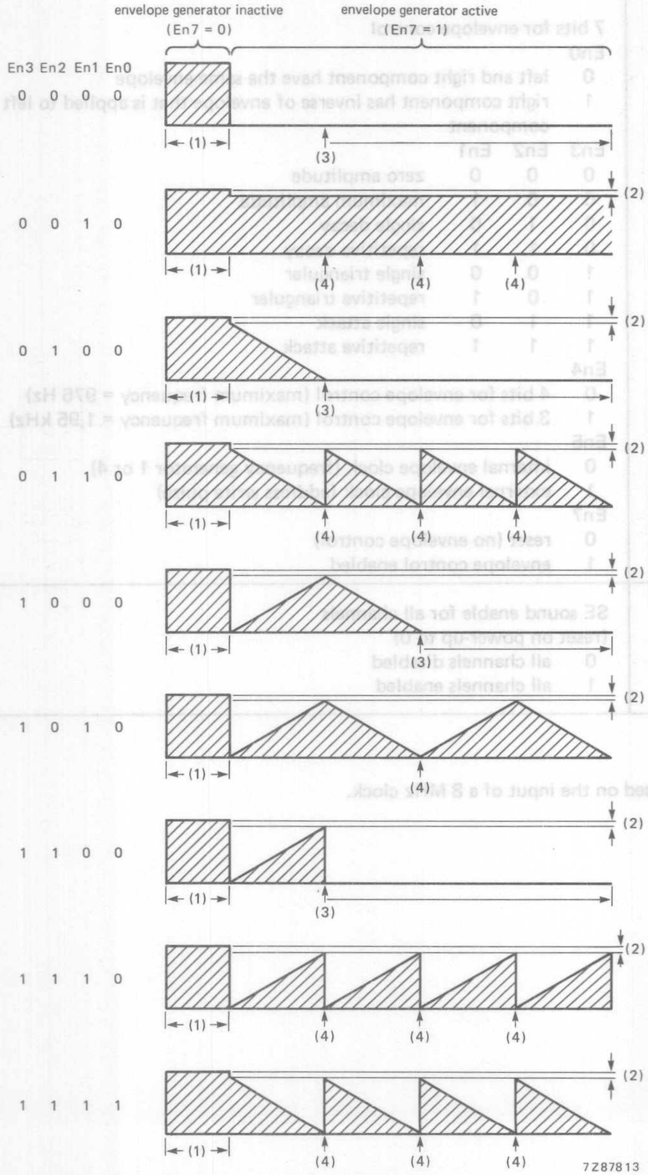



Fig. 5 Envelope waveforms.

**Notes to Fig. 5**

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 15/16ths of the amplitude level, rounded down to the nearest eight. When the generator is inactive (En7 = 0) the level will be 16/16ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).



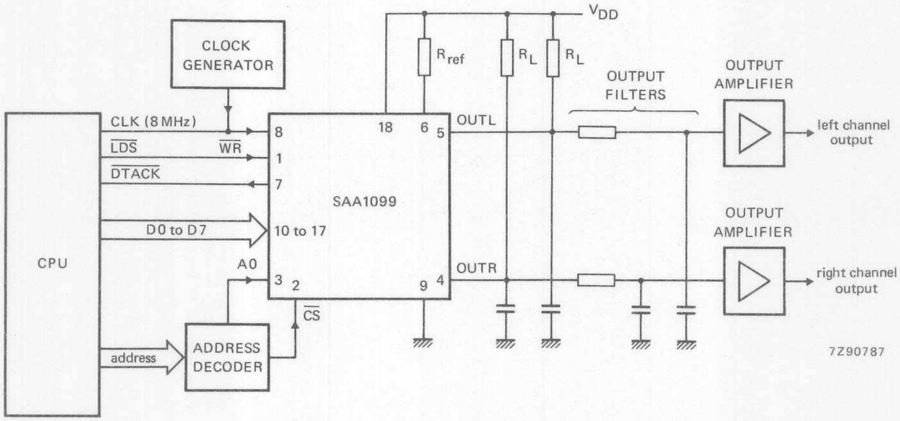



Fig. 6 Typical application circuit diagram.

# TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an $I^2C$ bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to −100 $\mu$A in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the $I^2C$ bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the $I^2C$ bus. A subaddressing system allows the connection of up to three circuits on the same $I^2C$ bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

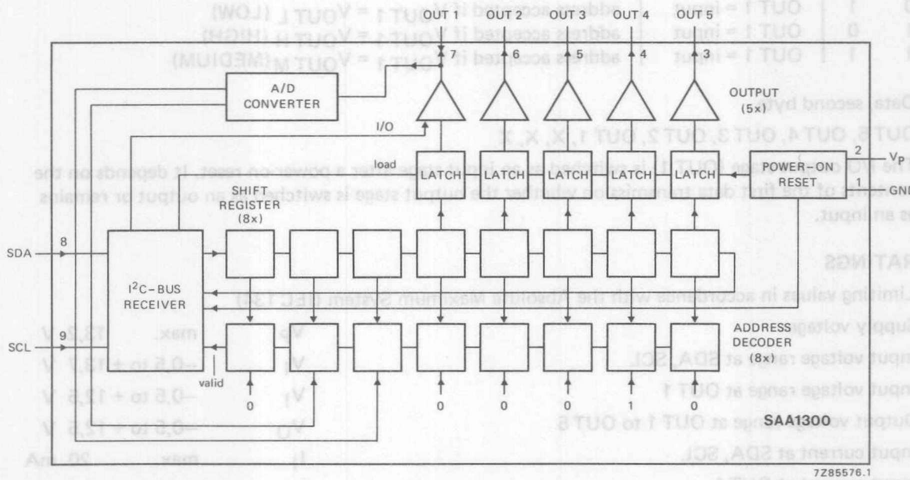



Fig. 1 Block diagram.

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

## PINNING

| pin no. | symbol | function |
|---|---|---|
| 1 | GND | ground |
| 2 | $V_P$ | positive supply |
| 3 | OUT 5 | outputs |
| 4 | OUT 4 | outputs |
| 5 | OUT 3 | outputs |
| 6 | OUT 2 | outputs |
| 7 | OUT 1 | output and subaddressing input |
| 8 | SDA | serial data line } $I^2C$ bus |
| 9 | SCL | serial clock line } $I^2C$ bus |

## $I^2C$ BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

| A | B | function | condition |
|---|---|---|---|
| 0 | 0 | general address | OUT 1 = output |
| 0 | 1 | OUT 1 = input | address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW) |
| 1 | 0 | OUT 1 = input | address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH) |
| 1 | 1 | OUT 1 = input | address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM) |

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | 13,2 | V |
| Input voltage range at SDA, SCL | $V_I$ | | −0,5 to + 13,7 | V |
| Input voltage range at OUT 1 | $V_I$ | | −0,5 to + 12,5 | V |
| Output voltage range at OUT 1 to OUT 5 | $V_O$ | | −0,5 to + 12,5 | V |
| Input current at SDA, SCL | $I_I$ | max. | 20 | mA |
| Input current at OUT 1 | $I_I$ | max. | 20 | mA |
| Total power dissipation | $P_{tot}$ | max. | 650 | mW |
| Storage temperature range | $T_{stg}$ | | −40 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 80 | °C |

## CHARACTERISTICS

$V_P$ = 8 V; $T_{amb}$ = 25 °C; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 2) | | | | | |
| Supply voltage range | $V_P$ | 4 | – | 12 | V |
| Supply current | $I_P$ | – | 10 | – | mA |
| Power-on reset level output stage in "OFF" condition | $V_{PR}$ | – | – | 3,5 | V |
| Maximum power dissipation* | $P_{max}$ | – | 650 | – | mW |
| **Inputs SDA, SCL** (pins 8 and 9) | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,8 | – | $V_P + 0,5$ | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 1,8 | V |
| Input current HIGH | $-I_{IH}$ | – | – | 50 | μA |
| Input current LOW | $I_{IH}$ | – | – | 0,1 | μA |
| Acknowledge sink current | $I_{ACK}$ | 2,5 | – | – | mA |
| Maximum input frequency | $f_{i\,max}$ | 100 | – | – | kHz |
| **Outputs OUT 1 to OUT 5** (pins 3 to 7) | | | | | |
| Maximum output current; source : "ON" | $I_{Oso}$ | + 100 | – | + 150 | mA |
| Maximum output current; source : "ON" $T_{amb}$ = 80 °C | $I_{Oso}$ | 60 | – | – | mA |
| Output voltage HIGH at $I_{Oso}$ | $V_{OH}$ | – | – | $V_P - 2$ | V |
| Output current; sink: "OFF" | $I_{Osi}$ | −100 | −300 | – | μA |
| Output voltage LOW at $I_{Osi}$ | $V_{OL}$ | – | – | 100 | mV |
| Output voltage MEDIUM at $I_O$ = 12,5 mA | $V_{OM}$ | – | – | $V_P - 0,5$ | V |
| **OUT 1 used as subaddressing input** | | | | | |
| Input voltage HIGH (code 1 0) | $V_{OUT\,1H}$ | 0,72 $V_P$ | – | $V_P$ | V |
| Input voltage MEDIUM (code 1 1) | $V_{OUT\,1M}$ | 0,39 $V_P$ | – | 0,61 $V_P$ | V |
| Input voltage LOW (code 0 1) | $V_{OUT\,1L}$ | 0 | – | 0,28 $V_P$ | V |

* Outputs must not be driven simultaneously at maximum source current.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# REMOTE CONTROL TRANSMITTER

## GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at $V_{DD} = 6$ V ($-I_{OH} = 40$ mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current $< 2$ mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

## PACKAGE OUTLINES

20-lead DIL; plastic (SOT-146C1).
20-lead mini-pack; plastic (SO-20; SOT-163AC3).

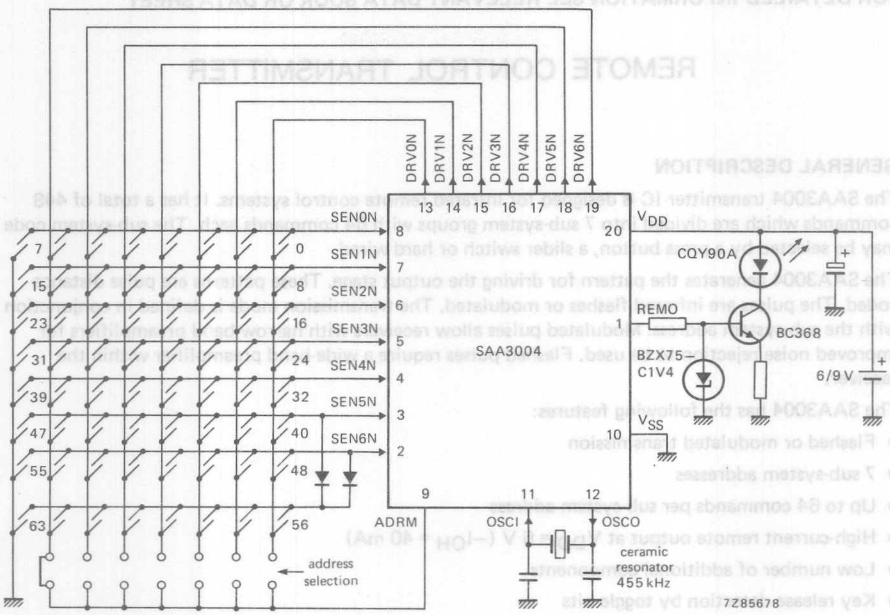



Fig. 1 Transmitter with SAA3004.

## INPUTS AND OUTPUTS

**Key matrix inputs and outputs** (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

**Address mode input** (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# LOW VOLTAGE INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

## GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

### Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{DD}$ | 2 to 7 | V |
| Input voltage range | $V_I$ | 0,5 to ($V_{DD}$ + 0,5) | V* |
| Input current | $\pm I_I$ | max. 10 | mA |
| Output voltage range | $V_O$ | −0,5 to ($V_{DD}$ + 0,5) | V* |
| Output current | $\pm I_O$ | max. 10 | mA |
| Operating ambient temperature range | $T_{amb}$ | −25 to +85 | $^oC$ |

* $V_{DD}$ + 0,5 V not to exceed 9 V.

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

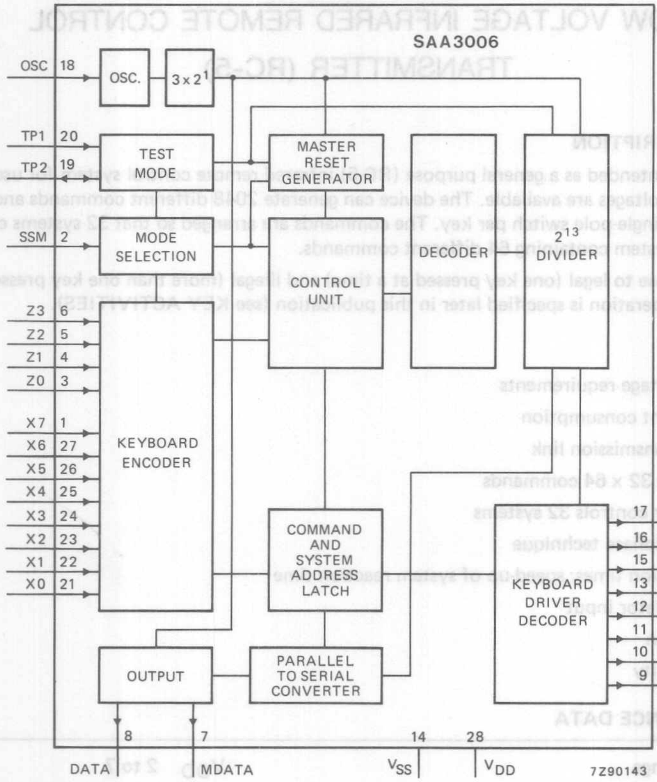



Fig. 1 Block diagram.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

## GENERAL DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

### Features

- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Very low current consumption
- For infrared transmission link
- Transmission by biphase technique
- Short transmission times; speed-up of system reaction time
- LC oscillator; no crystal required
- Input protection
- Test mode facility

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{DD}$ | 4,75 to 12,6 | V |
| Input voltage range | $V_I$ | $-0,5$ to $(V_{DD}+0,5)$ | V* |
| Input current | $\pm I_I$ | max. 10 | mA |
| Output voltage range | $V_O$ | $-0,5$ to $(V_{DD}+0,5)$ | V* |
| Output current | $\pm I_O$ | max. 10 | mA |
| Operating ambient temperature range | $T_{amb}$ | $-25$ to $+85$ | $^oC$ |

* $V_{DD}$ + 0,5 V not to exceed 15 V.

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

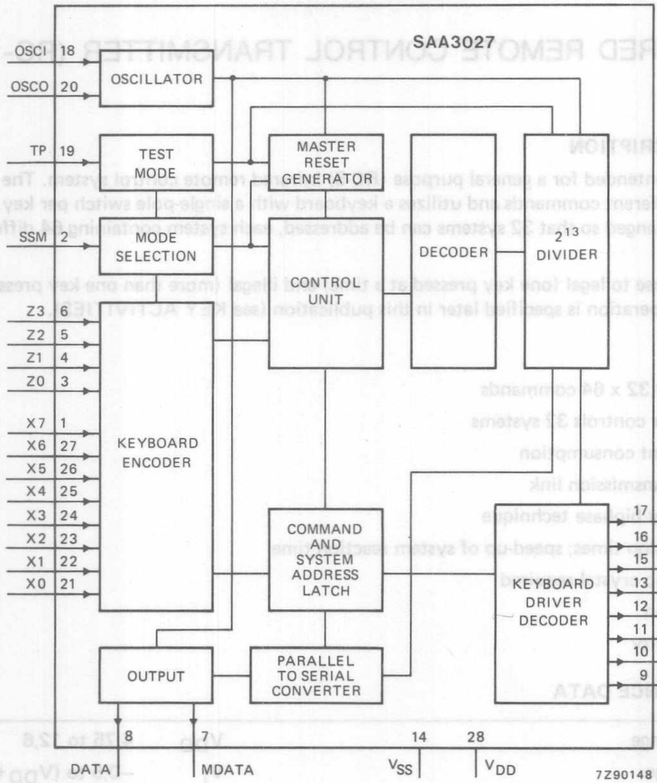



Fig. 1 Block diagram.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# INFRARED REMOTE CONTROL TRANSCODER (RC-5)

## GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for $I^2C$ bus operation.

### Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- $I^2C$ output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | 4,5 to | 5,5 | V |
| Supply current (quiescent) at $V_{DD}$ = 5,5 V; $T_{amb}$ = 25 °C | $I_{DD}$ | max. | 200 | $\mu$A |
| Operating ambient temperature range | $T_{amb}$ | −25 to | +85 | °C |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

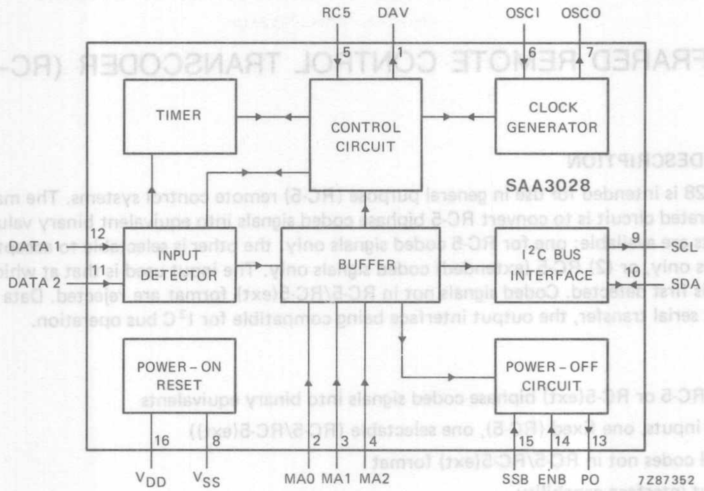



Fig. 1 Block diagram.

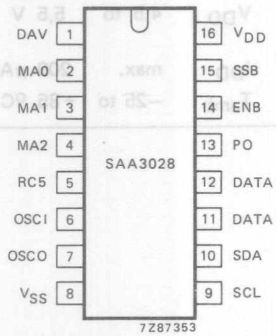



Fig. 2 Pinning diagram.

**PINNING**

| | | |
|---|---|---|
| 1 | DAV | data valid output with open drain N-channel transistor |
| 2 | MA0 | master address inputs |
| 3 | MA1 | |
| 4 | MA2 | |
| 5 | RC5 | data 2 input select |
| 6 | OSCI | oscillator input |
| 7 | OSCO | oscillator output |
| 8 | $V_{SS}$ | negative supply (ground) |
| 9 | SCL | serial clock line } $I^2C$ bus |
| 10 | SDA | serial data line |
| 11 | DATA 2 | data 2 input |
| 12 | DATA 1 | data 1 input |
| 13 | PO | power-off signal output with open drain N-channel transistor |
| 14 | ENB | enable input |
| 15 | SSB | set standby input |
| 16 | $V_{DD}$ | positive supply (+5 V) |

# INTERPOLATION AND MUTING CIRCUIT FOR COMPACT DISC DIGITAL AUDIO SYSTEM

## GENERAL DESCRIPTION

The SAA7000 interpolation and muting circuit descrambles and separates data into left and right channels and minimizes the effects of erroneous data on the performance of the Compact Disc Digital Audio System. Minor errors (those present in one data sample only) are replaced with audio data obtained by interpolation; more persistent errors are removed by muting.

### Features

- Descrambles data from error corrector SAA7020 and formats into left and right channels
- Minimizes the effect of erroneous data samples
- 16-bit serial data input (two's complement)
- Smoothed transitions before and after muting
- Interpolated data replaces single erroneous data samples
- Serial output for digital-to-analogue converters (DACs) or filter circuits
- Generates crystal-derived timing signals for system master data clock (4,2336 MHz), serving error corrector SAA7020 and digital filter SAA7030
- Selectable output format: offset binary or two's complement; 14 or 16-bit word

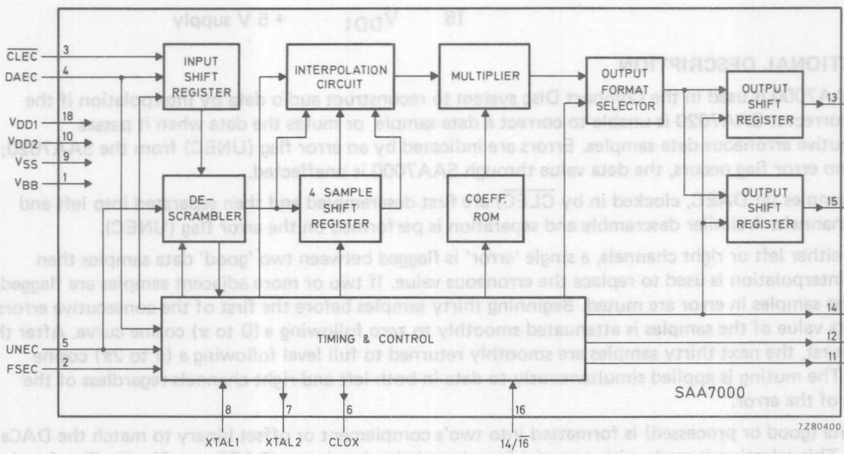



Fig. 1 Block diagram.

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

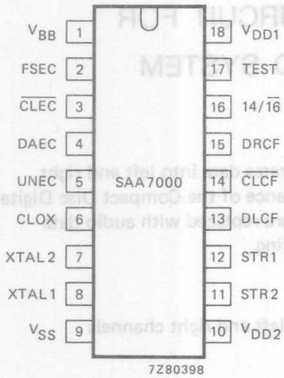



Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | FSEC | frame sync pulse input |
| 3 | $\overline{CLEC}$ | input data clock |
| 4 | DAEC | data input (two's complement) and output format selector |
| 5 | UNEC | error flag input |
| 6 | CLOX | buffered clock output (XTAL1) |
| 7 | XTAL2 | drive output to clock crystal |
| 8 | XTAL1 | external clock input |
| 9 | $V_{SS}$ | ground |
| 10 | $V_{DD2}$ | + 12 V supply |
| 11 | STR2 | strobe 2 output |
| 12 | STR1 | strobe 1 output |
| 13 | DLCF | left channel data output (format selected by DAEC) |
| 14 | $\overline{CLCF}$ | 14/16-bit clock burst output |
| 15 | DRCF | right channel data output (format selected by DAEC) |
| 16 | 14/$\overline{16}$ | selects bit length of clock burst output from $\overline{CLCF}$ |
| 17 | TEST | test input |
| 18 | $V_{DD1}$ | + 5 V supply |

## FUNCTIONAL DESCRIPTION

The SAA7000 is used in the Compact Disc system to reconstruct audio data by interpolation if the error corrector SAA7020 is unable to correct a data sample, or mutes the data when it passes consecutive erroneous data samples. Errors are indicated by an error flag (UNEC) from the SAA7020; when no error flag occurs, the data value through SAA7000 is unaffected.

Data samples (at DAEC, clocked in by $\overline{CLEC}$) are first descrambled and then separated into left and right channels. A similar descramble and separation is performed on the error flag (UNEC).

If, for either left or right channels, a single 'error' is flagged between two 'good' data samples then linear interpolation is used to replace the erroneous value. If two or more adjacent samples are flagged, then the samples in error are muted. Beginning thirty samples before the first of the consecutive errors, the data value of the samples is attenuated smoothly to zero following a (0 to $\pi$) cosine curve. After the error burst, the next thirty samples are smoothly returned to full level following a ($\pi$ to $2\pi$) cosine curve. The muting is applied simultaneously to data in both left and right channels regardless of the source of the error.

The data (good or processed) is formatted into two's complement or offset binary to match the DACs in use. This selection is made with a special function of the data input (DAEC, see Fig. 6). The data is then fed to the left and right outputs (DLCF and DRCF) and is clocked out by the output clock ($\overline{CLCF}$). Strobes (STR1 and STR2) are generated for the DACs and the digital filter (SAA7030). Fourteen or sixteen-bit DACs can be accommodated by the use of the select input (14/$\overline{16}$).

The SAA7000 automatically synchronizes to the error detector SAA7020 output using the frame sync pulse (FSEC) for internal timing reset and feeds a 2 x bit-rate clock (CLOX) to the system.

DEVELOPMENT DATA

**Pin functions**

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: −2,5 V ± 20%. |
| 2 | FSEC | Frame sync pulse (active HIGH) received from SAA7020 at the start of a data frame (12 data samples). FSEC is used to synchronize the descrambler to the data frames. For re-synchronization to occur, two consecutive FSEC pulses must be received each having a pulse width of approximately 6 CLOX cycles and the leading edge of the second pulse must be one data frame later than that of the first. FSEC is also used to synchronize the internal clock to the $\overline{\text{CLEC}}$ clock input, so aligning the gap in the internal clock to the FSEC pulse (see Fig. 4). |
| 3 | $\overline{\text{CLEC}}$ | Input data clock used to load serial data at DAEC into the input shift register. After a data sample has been loaded $\overline{\text{CLEC}}$ is held LOW to give a gap of 16 CLOX cycles (see Fig. 4). The period of the $\overline{\text{CLEC}}$ clock is 2 x the period of a CLOX cycle. |
| 4 | DAEC | Serial data samples are received at DAEC in two's complement form. The data is in 16-bit words separated by gaps; each word comprising two 8-bit symbols. The DAEC input is also used to select the output format; during the $\overline{\text{CLEC}}$ gap, a HIGH level at DAEC selects two's complement and a LOW level selects offset binary format (see Fig. 4). |
| 5 | UNEC | Error flag indicating unreliable data from SAA7020. During the period when data is clocked in at DAEC, UNEC is LOW only if the present 8-bit symbol is valid. During the period of the $\overline{\text{CLEC}}$ gap, UNEC is LOW only if the whole of the data word due to arrive 5 frames later is valid. |
| 6 | CLOX | Buffered XTAL1 clock output. |
| 7 | XTAL2 | Main clock crystal drive output. This pin should remain disconnected if a crystal is not used. |
| 8 | XTAL1 | Clock input from crystal circuit or for externally derived clock. |
| 9 | $V_{SS}$ | Ground (0 V). |
| 10 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |
| 11 | STR2 | Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 24 CLOX cycles and used to strobe data to the DACs. This pin should be left disconnected if SAA7030 is not used. |
| 12 | STR1 | Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 96 CLOX cycles – after each pair of data words have been clocked out. It is used to strobe data to SAA7030, or to the DACs if SAA7030 is not used. Both STR1 and STR2 are re-synchronized to XTAL1 to minimize jitter. |
| 13 | DLCF | Left channel data output; format in two's complement or offset binary, as selected at DAEC. |
| 14 | $\overline{\text{CLCF}}$ | Clock burst output of either 14 or 16 bits, as selected at pin 16. It is used to clock data from DLCF and DRCF (data is valid on $\overline{\text{CLCF}}$ falling edge, see Fig. 5). |
| 15 | DRCF | Right channel data output; format is two's complement or offset binary, as selected at DAEC. |
| 16 | $14/\overline{16}$ | Selects 14 or 16-bit bursts of output clock $\overline{\text{CLCF}}$. |
| 17 | TEST | This pin should be held LOW to ensure normal operation. |
| 18 | $V_{DD1}$ | Positive supply voltage: + 5 V ± 10%. |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); $V_{SS}$ = 0 V

| | | | | |
|---|---|---|---|---|
| Supply voltage 1 range (pin 18) | $V_{DD1}$ | −0,3 to | + 7,5 | V |
| Supply voltage 2 range (pin 10) | $V_{DD2}$ | −0,3 to | + 15 | V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to | + 0,3 | V |
| Input voltage range | $V_I$ | −0,3 to | + 7,5 | V |
| Output voltage range at $V_I$ = −0,3 to + 6,5 V; $T_{amb}$ = 25 °C | $V_O$ | −0,3 to | + 7,5 | V |
| Output current | $I_O$ | max. | 10 | mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to | + 70 | °C |
| Storage temperature range | $T_{stg}$ | −55 to | + 125 | °C |

## CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = −20 to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supplies** | | | | | |
| Supply voltage 1 (pin 18) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 10) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 18) | $I_{DD1}$ | 30 | 70 | 140 | mA |
| Supply current 2 (pin 10) | $I_{DD2}$ | 2 | 5 | 10 | mA |
| Back bias supply current (pin 1) | $-I_{BB}$ | – | – | 500 | μA |
| **Inputs** (except $V_{BB}$) | | | | | |
| Input voltage LOW | $V_{IL}$ | −0,3 | – | + 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | 6,5 | V |
| Input current (note 1) | $I_I$ | −1 | – | + 1 | μA |
| Input capacitance (not XTAL1) | $C_I$ | – | – | 7 | pF |
| **Outputs DLCF, DRCF, $\overline{\text{CLCF}}$, CLOX, STR1, STR2** (note 2) | | | | | |
| Output voltage LOW at $-I_{OL}$ = 1,6 mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH}$ = 0,2 mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | – | 150 | pF |
| **Output XTAL2** | | | | | |
| Operating frequency using crystal oscillator (Fig. 3) | $f_{XTAL}$ | 3,0 | 4,2336 | 4,5 | MHz |
| Operating frequency using driven input applied to XTAL1 | $f_{IN}$ | 3,0 | 4,2336 | 4,5 | MHz |
| **Input XTAL1** | | | | | |
| Input clock LOW | $t_{IXL}$ | 40 | – | – | % of period |
| Input clock HIGH | $t_{IXH}$ | 40 | – | – | % of period |
| **Crystal amplifier** (pins 7 and 8) | | | | | |
| Mutual conductance at 5 MHz | gm | 1,5 | – | – | mA/V |
| Bandwidth of mutual conductance at minimum 3 dB | $B_{gm}$ | 10 | – | – | MHz |
| Input capacitance | $C_I$ | – | – | 10 | pF |
| Output capacitance | $C_O$ | – | – | 7 | pF |
| Feedback capacitance | $C_{FB}$ | – | – | 5 | pF |
| Input leakage current | $I_I$ | −1 | – | + 1 | μA |
| Output current at 5 MHz | $I_o$ | −1 | – | + 1 | mA |
| Small signal gain at 5 MHz | $A_V$ | −4 | – | – | |

DEVELOPMENT DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Inputs DAEC, UNEC, $\overline{\text{CLEC}}$, FSEC** | | | | | |
| Input rise time (FSEC only) | $t_{IR}$ | – | – | 100 | ns |
| Input fall time (FSEC only) | $t_{IF}$ | – | – | 100 | ns |
| $\overline{\text{CLEC}}$ HIGH | $t_{ICH}$ | 100 | – | – | ns |
| $\overline{\text{CLEC}}$ LOW | $t_{ICL}$ | 100 | – | – | ns |
| DAEC to $\overline{\text{CLEC}}$ set-up time | $t_{IDS}$ | 40 | – | – | ns |
| $\overline{\text{CLEC}}$ to DAEC hold time | $t_{IDH}$ | 40 | – | – | ns |
| FSEC HIGH (note 3) | $t_{FSH}$ | 4 CLOX periods −400 | – | 8 CLOX periods + 190 | ns |
| DAEC/UNEC to FSEC set-up time | $t_{UFS}$ | 0 | – | – | ns |
| FSEC to DAEC/UNEC hold time (note 3) | $t_{UFH}$ | 8 CLOX periods + 325 | – | – | ns |
| **Output CLOX** (notes 4 and 5) | | | | | |
| Output clock LOW | $t_{OXL}$ | 30 | – | – | % of period |
| Output clock HIGH | $t_{OXH}$ | 30 | – | – | % of period |
| output clock rise time | $t_{OXR}$ | – | – | 50 | ns |
| Output clock fall time | $t_{OXF}$ | – | – | 40 | ns |
| **Outputs STR1, STR2** (note 6) | | | | | |
| Output strobe rise time | $t_{OSR}$ | – | 10 | 20 | ns |
| Output strobe fall time | $t_{OSF}$ | – | 6 | 20 | ns |
| Output strobe HIGH | $t_{OSH}$ | 1 CLOX period + 50 | 2 CLOX periods −20 | 4 CLOX periods | ns |
| Output strobe LOW | $t_{OSL}$ | 10 | – | – | CLOX periods |
| CLOX to STR1, STR2 delay time | $t_{XSL}$ | 0 | – | – | ns |
| | $t_{XSH}$ | – | – | 45 | ns |

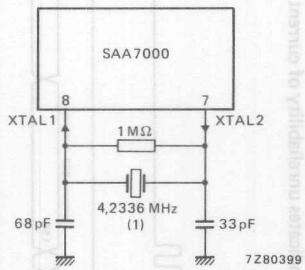
## CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Outputs $\overline{CLCF}$, DLCF, DRCF** (note 4) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 50 | ns |
| Output fall time | $t_{OF}$ | – | – | 40 | ns |
| Output data clock HIGH | $t_{OCH}$ | 120 | – | – | ns |
| Output data clock LOW | $t_{OCL}$ | 120 | – | – | ns |
| DLCF, DRCF to $\overline{CLCF}$ set-up time | $t_{ODS}$ | 50 | – | – | ns |
| $\overline{CLCF}$ to DLCF, DRCF hold time | $t_{ODH}$ | 100 | – | – | ns |
| $\overline{CLCF}$ LOW prior to STR1 (note 3) | $t_{CSL}$ | 52 | 60 | – | CLOX periods |

DEVELOPMENT DATA

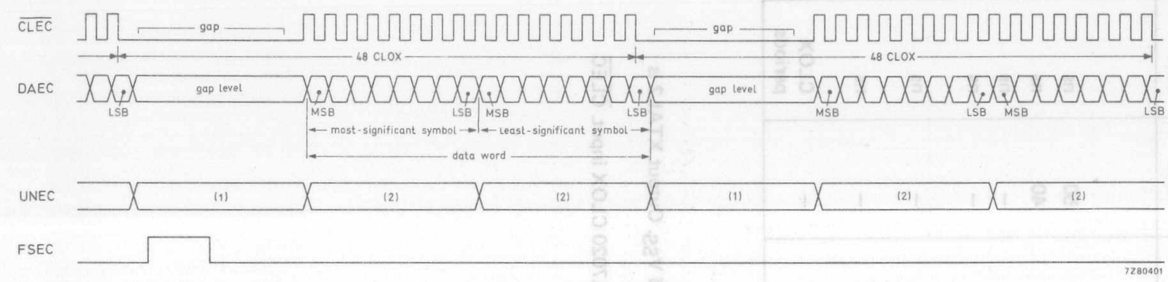
## NOTES TO THE CHARACTERISTICS

1. $V_I = -0,3$ to $+6,5$ V; $T_{amb} = 25$ °C.
2. All outputs, except XTAL2, are short-circuit protected to $V_{DD1}$ and $V_{SS}$. Output XTAL2 is protected to $V_{SS}$ only.
3. Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{CLEC}$ period is twice the CLOX period.
4. Output load capacitance is 50 pF.
5. XTAL1 (pin 8) is driven by an external clock.
6. Output load capacitance is 30 pF on STR1, STR2 outputs.




(1) Catalogue number of crystal is 6416 009 00111.

Fig. 3 Crystal oscillator circuit.




(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.

Fig. 4 Typical input waveforms.

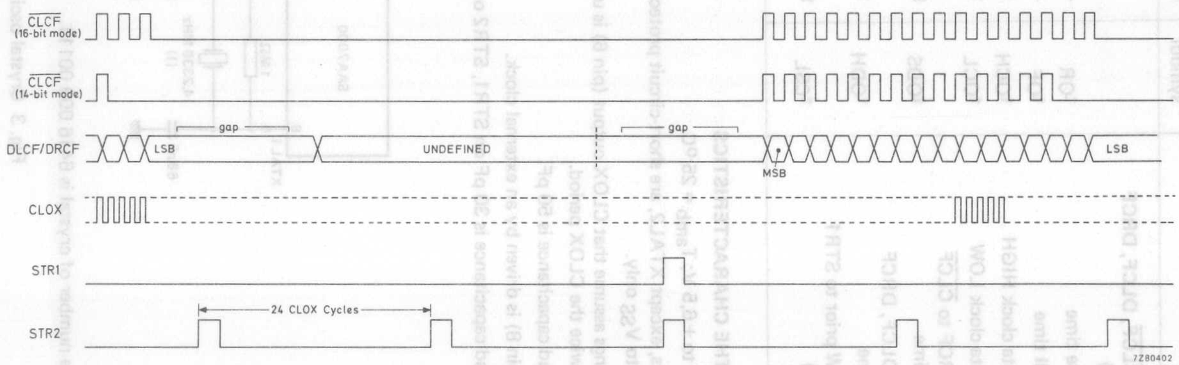
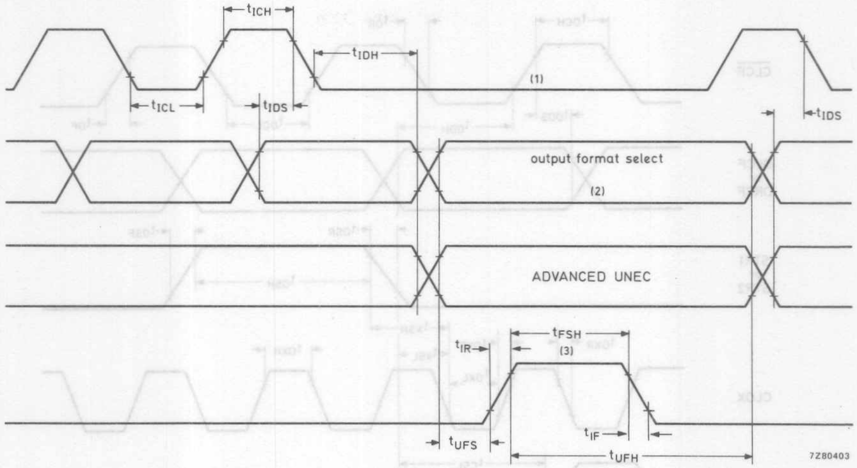



Fig. 5 Typical output waveforms.




(1) $\overline{\text{CLEC}}$ remains LOW for a minimum period of approximately 16 CLOX periods.

(2) Data during this time is used to determine the format of the output from SAA7000; when DAEC is HIGH a two's complement format is selected, when LOW an offset binary format is selected.

(3) Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{\text{CLEC}}$ period is twice the CLOX period.

Fig. 6 Input waveforms. Reference levels are 0,8 V and 2,4 V; $t_{IR}$ and $t_{IF}$ apply to FSEC waveform only.

DEVELOPMENT DATA

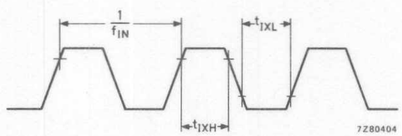



Fig. 7 Optional clock input waveform at XTAL1 (pin 8).

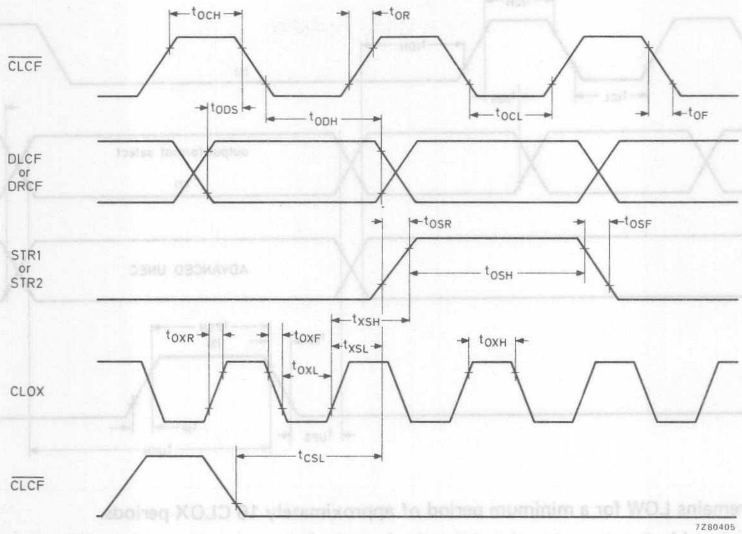



Fig. 8 Output waveforms. Reference levels are 0,8 V and 2,4 V. Output loadings on STR1 and STR2 are 30 pF; output loadings on CLOX, $\overline{CLCF}$, DLCF and DRCF are 50 pF.

# DEMODULATOR FOR COMPACT DISC DIGITAL AUDIO SYSTEM

## GENERAL DESCRIPTION

The SAA7010 demodulates and decodes the pulse code modulated input signal into digital data for the Compact Disc Digital Audio system. A 4,3 MHz (typical) clock locked to the disc rate is also produced.

### Features

- Phase-locked loop clock regenerator with frequency detector for locking
- High-frequency level detector with adaptive slicer for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Outputs to subcoding microprocessor
- Fully protected timing synchronization to incoming data

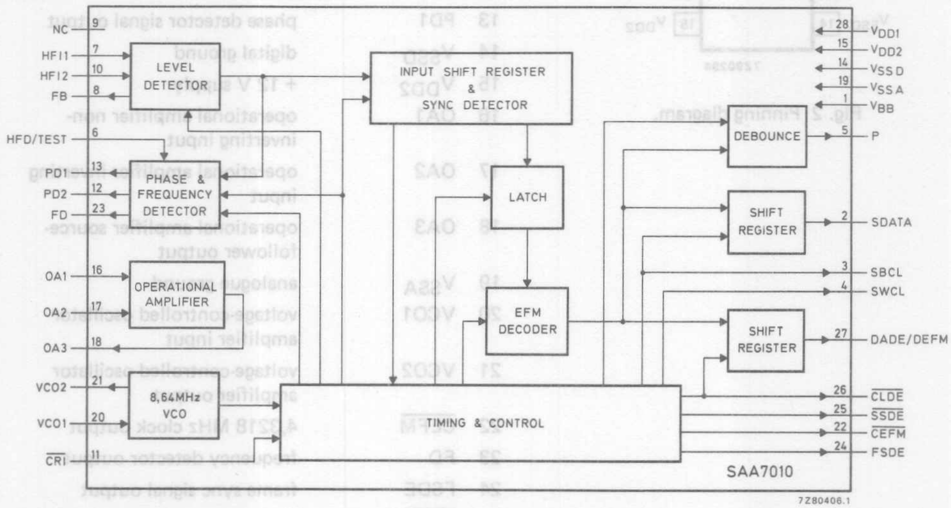



Fig. 1 Block diagram.

## PACKAGE OUTLINE

28-lead DIL; package (SOT-117).

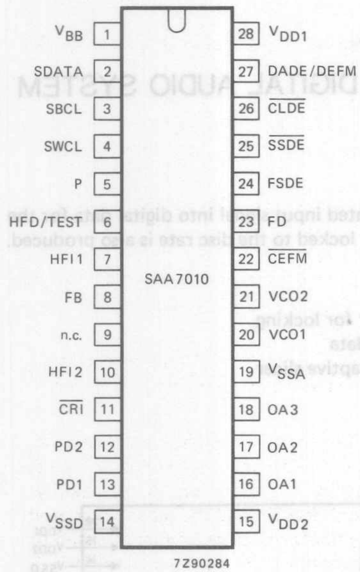



Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | SDATA | subcoding data output |
| 3 | SBCL | subcoding bit clock output |
| 4 | SWCL | subcoding word clock output |
| 5 | P | subcoding pause bit output |
| 6 | HFD/TEST | high-frequency detector input in normal operation. Selects test mode when at $V_{DD2}$ |
| 7 | HFI1 | level detector input |
| 8 | FB | current feedback from level detector |
| 9 | n.c. | not connected |
| 10 | HFI2 | alternative input to level detector |
| 11 | $\overline{CRI}$ | counter reset inhibit input |
| 12 | PD2 | phase detector reference output |
| 13 | PD1 | phase detector signal output |
| 14 | $V_{SSD}$ | digital ground |
| 15 | $V_{DD2}$ | + 12 V supply |
| 16 | OA1 | operational amplifier non-inverting input |
| 17 | OA2 | operational amplifier inverting input |
| 18 | OA3 | operational amplifier source-follower output |
| 19 | $V_{SSA}$ | analogue ground |
| 20 | VCO1 | voltage-controlled oscillator amplifier input |
| 21 | VCO2 | voltage-controlled oscillator amplifier output |
| 22 | $\overline{CEFM}$ | 4,3218 MHz clock output |
| 23 | FD | frequency detector output |
| 24 | FSDE | frame sync signal output |
| 25 | $\overline{SSDE}$ | symbol sync signal output |
| 26 | $\overline{CLDE}$ | data bit clock output |
| 27 | DADE/DEFM | serial data output/EFM digital output: selection determined by level at pin 11 |
| 28 | $V_{DD1}$ | + 5 V supply |

## FUNCTIONAL DESCRIPTION

The SAA7010 demodulator forms the front-end of the Compact Disc Digital Audio system, supplying demodulated data and timing signals to the error corrector (SAA7020) and to the subcoding micro-processor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. The level detector is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

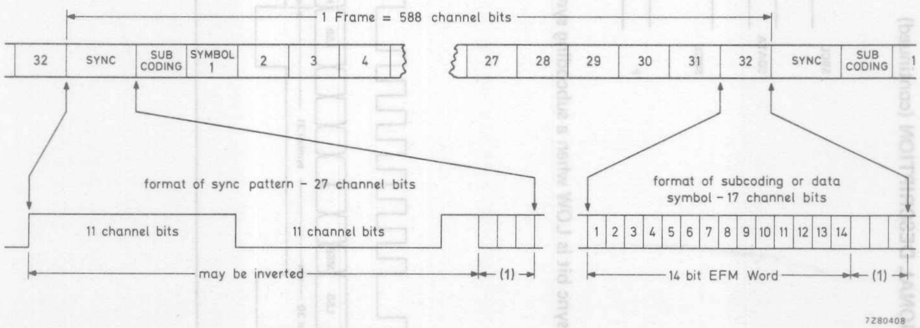
A frequency detector and a phase detector provide the coarse and fine control signals for the phase-locked loop (PLL) system. The loop gain is supplied by an internal operational amplifier which drives a voltage-controlled oscillator (VCO) running at twice the input data rate (typically 8,6436 MHz). The VCO output is divided by two by a clock generator in the timing and control circuits and the resulting output is used to clock the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.

After phase detection the data is clocked into the 23-bit input shift register which then detects the frame sync pattern. Within the timing and control circuits are minimum and maximum data length detectors which provide frequency limit signals for the frequency detector.

Also within the timing and control circuits are two divide-by-588 counters, one master and one slave, two divide-by-17 symbol rate counters and a lock indication counter. The frame sync signal is used to reset the divide-by-588 slave counter. This counter and one divide-by-17 symbol rate counter supply timing signals for clocking the EFM (eight-to-fourteen modulation) decoder and the subcoding output circuits. The data is read from the input shift register in 14-bit symbols which are first latched and then decoded into 8-bit data words. The subcoding part of the data consists of one word per frame (Fig. 3), so the output SDATA comprises a burst of 8 data bits accompanied by a 2,1906 MHz clock burst signal SBCL (Fig. 4). One bit of this subcoding output data is replaced by a subcoding frame sync bit which is decoded from one of two special EFM codes. The displaced bit (the pause (P) bit) is latched to its own output via a debounce circuit to remove erroneous changes.

DEVELOPMENT DATA

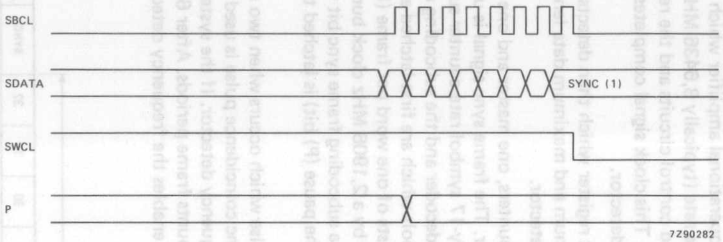
The divide-by-588 slave counter also provides a sync coincidence pulse which occurs when two detected sync pulses are precisely one frame apart (588 clock cycles). The sync coincidence pulse is used to reset the lock indication counter and disable the FD output from the frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.




(1) Merging and low frequency suppression bits.

Fig. 3 Data input signal.

## FUNCTIONAL DESCRIPTION (continued)




(1) The sync bit is LOW when a subcoding sync word is detected.

Fig. 4 Typical subcoding waveform outputs.

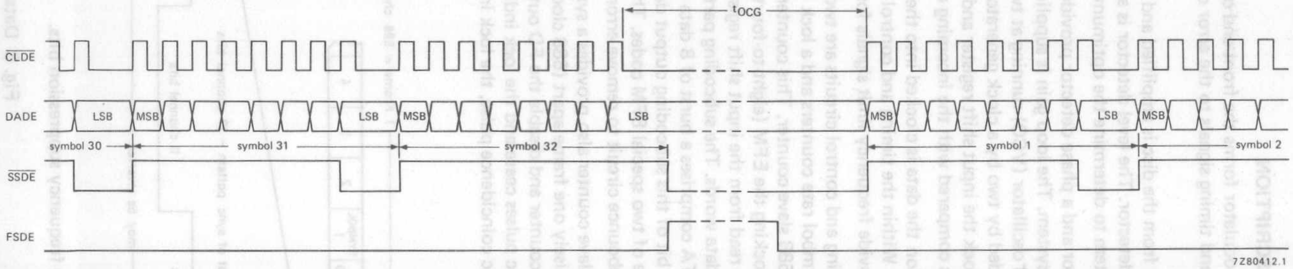



Fig. 5 Typical waveform outputs to SAA7020.

**FUNCTIONAL DESCRIPTION** (continued)

A delayed version of the sync coincidence pulse resets the divide-by-588 master counter. This counter is reset only by coincident sync pulses or sync pulses which occur during a predetermined 'window' at the start of each frame and is therefore protected from accidental reset by erroneous sync patterns. The window is wide enough to allow PLL bit-slips but narrow enough to avoid false sync signals generated by corrupt data. The divide-by-588 master counter may be allowed to free-run by taking $\overline{\text{CRI}}$ input (pin 11) LOW to inhibit the reset signal.

The divide-by-588 master counter and the second divide-by-17 symbol rate counter are used to time the data and clock outputs to the error corrector SAA7020 (Fig. 5). In this way, even if the data has been corrupted, the timing signals will be correct and are only re-synchronized after a complete frame has been sent to SAA7020.

The data output to SAA7020 comprises thirty-two 8-bit symbols per frame, with half-bit gaps between each symbol and a much longer gap during the frame sync period. It is this longer gap that changes in length when corrupt data upsets the timing system.

**Pin functions**

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: −2,5 V ± 20%. |
| 2 | SDATA | Subcoding data push-pull output. An 8-bit burst of data (including a 1-bit subcoding frame sync) is output serially once per frame coincident with SBCL. |
| 3 | SBCL | Subcoding bit clock push-pull output. An 8-bit burst clock, typically at 2,1609 MHz, is used to synchronize the subcoding data. |
| 4 | SWCL | Subcoding word clock push-pull output. A square-wave signal at data frame rate (7,35 kHz) used to synchronize the subcoding words and the pause (P) bit. |
| 5 | P | Subcoding pause bit push-pull output. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data. |
| 6 | HFD/TEST | External high-frequency detector input. When this signal is HIGH the frequency detector output (FD) and phase detector are enabled. When pin 6 is connected to $V_{DD2}$, the device enters TEST mode. |
| 7 | HFI1 | Level detector input. A signal of between 0,25 and 2,5 V (peak-to-peak value) is required to drive the level detector correctly. |
| 8 | FB | Current feedback from the level detector. |
| 9 | n.c. | Not connected. |
| 10 | HFI2 | Alternative input to the level detector. |
| 11 | $\overline{\text{CRI}}$ | Counter reset inhibit signal input. When LOW, this signal allows the divide-by-588 master counter to free-run and causes pin 27 output to be converted to DEFM. During power-up, pin 11 should be held HIGH for 10 ms. |
| 12 | PD2 | Phase detector reference signal, maximum impedance 10 kΩ. |
| 13 | PD1 | Phase detector output signal, maximum impedance 10 kΩ. The differential d.c. content of PD1 and PD2 signals is a measure of the phase difference between the data and the internal 4,3218 MHz clock. |
| 14 | $V_{SSD}$ | Digital ground. Main ground terminal. |
| 15 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |

| pin no. | mnemonic | description |
|---|---|---|
| 16 | OA1 | Operational amplifier non-inverting input. |
| 17 | OA2 | Operational amplifier inverting input. |
| 18 | OA3 | Operational amplifier source follower output. |
| 19 | $V_{SSA}$ | Analogue ground. Ground terminal for operational amplifier and VCO only. Connected internally to $V_{SSD}$ via a 25 Ω (nominal) resistor. |
| 20 | VCO1 | Voltage-controlled oscillator amplifier input. The amplifier is a simple inverter operating up to 10 MHz. Frequency control is achieved via an external tuned circuit using variable capacitance diodes. |
| 21 | VCO2 | Voltage-controlled oscillator amplifier output. The load for the inverting transistor may be turned off for test purposes by reducing $V_{DD2}$ to 0 V. |
| 22 | $\overline{\text{CEFM}}$ | Internal 4,3218 MHz clock generator push-pull output. |
| 23 | FD | Frequency detector three-state push-pull output. This output has a 1kΩ (typical) impedance when active but assumes a high impedance state once the system is in lock. |
| 24 | FSDE | Frame sync signal push-pull output (to SAA7020). It provides a positive-going pulse at the end of each data frame. Typical frequency = 7,35 kHz. |
| 25 | $\overline{\text{SSDE}}$ | Symbol sync signal push-pull output for each data symbol. Typical frequency = 254 kHz. |
| 26 | $\overline{\text{CLDE}}$ | Data bit clock push-pull output (to SAA7020). An 8-bit clock burst at 2,1609 MHz (typical) which is used to synchronize the data to SAA7020 (see Fig. 5). |
| 27 | DADE/DEFM | Data push-pull output (to SAA7020). Serial data comprising 32 x 8-bit symbols per frame, synchronized to $\overline{\text{CLDE}}$ (see Fig. 5). This output is converted to DEFM when $\overline{\text{CRI}}$ (pin 11) is LOW. DEFM is the digital signal appearing at the output of the level detector. |
| 28 | $V_{DD1}$ | Positive supply voltage: + 5 V ± 10%. |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134);
$V_{SSA} = V_{SSD} = 0$ V.

| | | |
|---|---|---|
| Supply voltage 1 range (pin 28) | $V_{DD1}$ | −0,3 to + 7,5 V |
| Supply voltage 2 range (pin 15) | $V_{DD2}$ | −0,3 to + 15 V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to + 0,3 V |
| Input voltage range | $V_I$ | −0,3 to + 7,5 V |
| Output voltage range (except FD, OA3) | $V_O$ | −0,3 to + 7,5 V |
| Output voltage range (FD, OA3 only) | $V_O$ | −0,3 to + 15 V |
| Output current (each output) | $I_O$ | max. 10 mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 70 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## CHARACTERISTICS

$V_{SSA} = V_{SSD} = 0$ V; $T_{amb} = -20$ to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| Supply voltage 1 (pin 28) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 15) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 28) | $I_{DD1}$ | 30 | 60 | 150 | mA |
| Supply current 2 (pin 15) | $I_{DD2}$ | 4 | 8 | 21 | mA |
| Back bias supply current (pin 1) | $-I_{BB}$ | – | – | 500 | μA |
| **DIGITAL CIRCUITS** | | | | | |
| **Input HFD, $\overline{\text{CRI}}$** | | | | | |
| Input voltage LOW | $V_{IL}$ | −0,3 | – | + 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | 6,5 | V |
| Input current (note 1) | $I_I$ | −1 | – | + 1 | μA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Outputs DADE/DEFM, $\overline{\text{CLDE}}$, FSDE, $\overline{\text{SSDE}}$, SBCL, SDATA, P, SWCL, $\overline{\text{CEFM}}$** (note 2) | | | | | |
| Output voltage LOW at $-I_{OL} = 1{,}6$ mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH} = 0{,}2$ mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | – | 150 | pF |

DEVELOPMENT DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **DIGITAL CIRCUITS** (continued) | | | | | |
| **Output FD** | | | | | |
| Output voltage LOW at $-I_{OL}$ = 100 $\mu$A | $V_{OL}$ | 0 | – | 0,5 | V |
| Output voltage HIGH at $I_{OH}$ = 100 $\mu$A | $V_{OH}$ | 8,0 | – | $V_{DD2}$ + 0,5 | V |
| Output leakage current at $V_O$ = 0 to 6 V (note 3) | $\pm I_L$ | – | – | 1 | $\mu$A |
| Output impedance | $Z_O$ | – | 1 | – | k$\Omega$ |
| **Outputs PD1, PD2** | | | | | |
| Output impedance | $Z_O$ | – | 5 | 10 | k$\Omega$ |
| **LEVEL DETECTOR** | | | | | |
| **Inputs HFI1, HFI2** | | | | | |
| A.C. input voltage range (peak-to-peak value) | $V_{I(p-p)}$ | 0,25 | – | 2,5 | V |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Output FB** | | | | | |
| Output current at $V_{FB}$ = 2 V | $I_{FB}$ | – | 150 | – | $\mu$A |
| **OPERATIONAL AMPLIFIER** (note 4) | | | | | |
| **Inputs OA1, OA2** | | | | | |
| Common-mode voltage range | $V_{CIM}$ | 1,5 | – | 6,0 | V |
| Input offset voltage | $\pm V_{IOF}$ | – | 20 | – | mV |
| Input current (note 1) | $\pm I_I$ | – | – | 1 | $\mu$A |
| Input offset current (note 5) | $\pm I_{IOF}$ | – | – | 0,1 | $\mu$A |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Common-mode rejection ratio | CMRR | 40 | – | – | dB |
| Open loop gain (d.c.) | A | 40 | – | – | dB |
| Gain bandwidth product (20 dB/decade roll-off) | | 1 | 5 | – | MHz |
| **Output OA3** | | | | | |
| Output voltage LOW at $-I_{OL}$ = 1 mA | $V_{OL}$ | 0 | – | 1 | V |
| Output voltage HIGH at $I_{OH}$ = 1 mA | $V_{OH}$ | 8,0 | – | $V_{DD2}$ + 0,5 | V |

DEVELOPMENT DATA

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **VCO** | | | | | |
| **Input VCO1, output VCO2** | | | | | |
| Mutual conductance at 100 kHz | $g_m$ | 1,5 | – | – | mA/V |
| Bandwidth (–3 dB cut-off) | $B_{gm}$ | 20 | – | – | MHz |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Output capacitance | $C_O$ | – | – | 7 | pF |
| Feedback capacitance | $C_{FB}$ | – | – | 5 | pF |
| Input leakage current (note 1) | $\pm I_I$ | – | – | 1 | $\mu$A |
| Output current at 10 MHz | $\pm I_O$ | – | 1 | – | mA |
| Small-signal voltage gain at 100 kHz | $A_V$ | 4 | – | – | V/V |
| **TIMING** | | | | | |
| Operating frequency (except VCO) | $F_{CEFM}$ | 0,1 | – | 5 | MHz |
| Operating frequency (VCO only) | $F_{VCO}$ | 0,2 | – | 10 | MHz |
| **Outputs $\overline{\text{CLDE}}$, DADE, $\overline{\text{SSDE}}$, FSDE, $\overline{\text{CEFM}}$** (Fig. 6 and note 6) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 50 | ns |
| Output fall time | $t_{OF}$ | – | – | 40 | ns |
| $\overline{\text{CLDE}}$ period | $t_{OCP}$ | 400 | – | – | ns |
| $\overline{\text{CLDE}}$ HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| $\overline{\text{CLDE}}$ LOW time | $t_{OCL}$ | 150 | – | – | ns |
| DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time | $t_{ODS}$ | 100 | – | – | ns |
| $\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time | $t_{ODH}$ | 100 | – | – | ns |
| $\overline{\text{SSDE}}$ LOW time (note 7) | $t_{SSL}$ | | 3 | – | $\overline{\text{CEFM}}$ |
| $\overline{\text{CLDE}}$ LOW time during FSDE (Fig. 5 and note 8) | $t_{OCG}$ | 16 | 46 | – | period |
| **Outputs SBCL, SDATA, P, SWCL** (Fig. 7) | | | | | |
| Output rise time (SBCL, SDATA) (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (SBCL, SDATA) (note 6) | $t_{OF}$ | – | – | 40 | ns |
| Output rise time (P, SWCL) (note 9) | $t_{OSR}$ | – | – | 200 | ns |
| Output fall time (P, SWCL) (note 9) | $t_{OSF}$ | – | – | 200 | ns |
| SBCL HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| SBCL LOW time | $t_{OCL}$ | 150 | – | – | ns |
| SDATA to SBCL set-up time | $t_{ODS}$ | 100 | – | – | ns |
| P to SWCL set-up time | $t_{ODSP}$ | 1 | – | – | ns |
| SBCL to SDATA hold time | $t_{ODH}$ | 100 | – | 500 | ns |
| SBCL to SWCL hold time | $t_{SWH}$ | 0 | – | – | $\mu$s |
| SWCL duty cycle ($t_{HIGH}/t_{period}$) | | 40 | 50 | 60 | % |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **TIMING** (continued) | | | | | |
| **Output FD** | | | | | |
| Output rise time (note 6) | $t_{FDR}$ | – | | 1 | μs |
| Output fall time (note 6) | $t_{FDF}$ | – | – | 1 | μs |
| **Outputs DEFM, $\overline{\text{CEFM}}$** (Fig. 8) | | | | | |
| Output rise time (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (note 6) | $t_{OF}$ | – | – | 40 | ns |
| DEFM to $\overline{\text{CEFM}}$ set-up time (note 10) | $t_{ODS}$ | 50 | – | – | ns |
| $\overline{\text{CEFM}}$ to DEFM hold time (note 10) | $t_{ODH}$ | 70 | – | – | ns |
| $\overline{\text{CEFM}}$ HIGH time | $t_{OCH}$ | 50 | – | – | ns |
| $\overline{\text{CEFM}}$ LOW time | $t_{OCL}$ | 50 | – | – | ns |

**NOTES TO THE CHARACTERISTICS**

1. At $T_{amb}$ = 25 °C; $V_{IN}$ = –0,3 to + 6,5 V; $V_{DD1}$ = 6,5 V.
2. Short-circuit protected to $V_{DD1}$ and $V_{SS}$. The maximum load capacitance that can be applied before short-circuit protection becomes operative is 150 pF.
3. At $T_{amb}$ = 25 °C; output in high impedance state.
4. All tests performed within common-mode voltage range.
5. At $T_{amb}$ = 25 °C.
6. Output loading = 50 pF.
7. $\overline{\text{SSDE}}$ remains LOW for only one negative edge of $\overline{\text{CLDE}}$.
8. Excessive bit-slip may cause gap to disappear. $\overline{\text{CLDE}}$ remains LOW when FSDE is HIGH.
9. Output loading = 150 pF.
10. Free running VCO frequency tuned to nominal and PLL in lock with a typical application circuit.

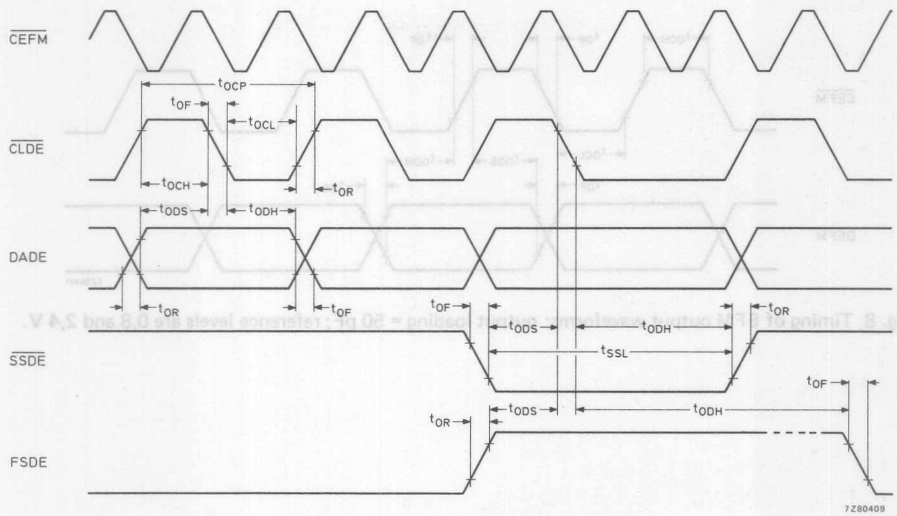



Fig. 6 Timing of waveform outputs to SAA7020.



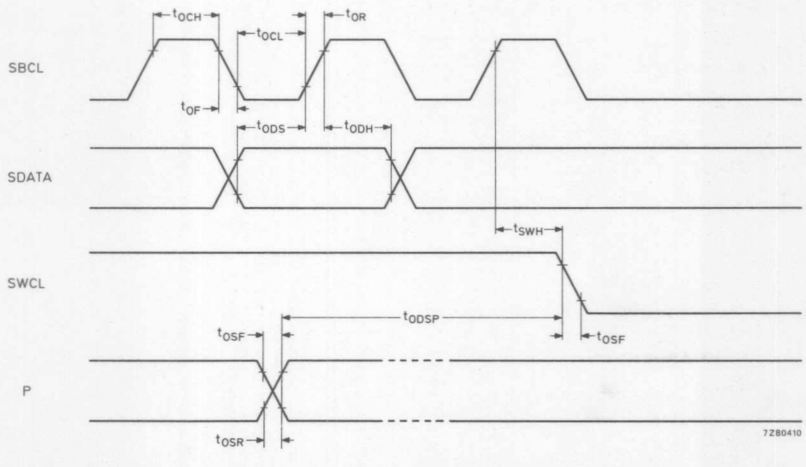



Fig. 7 Timing of waveform outputs for subcoding: reference levels are 0,8 and 2,4 V; SBCL and SDATA output loading = 50 pF; SWCL and P output loading = 150 pF; SWCL has a 50% duty cycle.

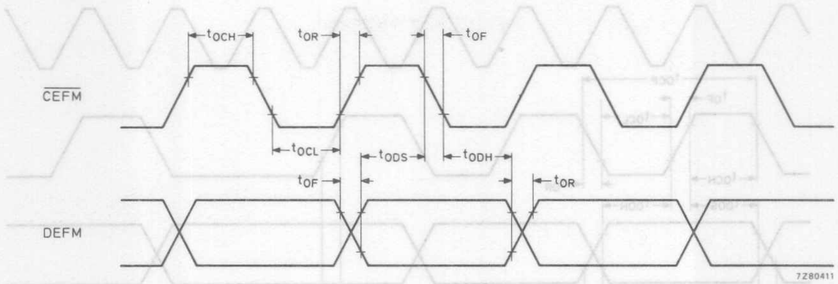



Fig. 8 Timing of EFM output waveforms: output loading = 50 pF; reference levels are 0,8 and 2,4 V.

# DEMODULATOR FOR COMPACT DISC DIGITAL AUDIO SYSTEM

## GENERAL DESCRIPTION

The SAA7011 demodulates and decodes the pulse code modulated input signal into digital data for the Compact Disc Digital Audio system. A separate pin for eight-to-fourteen modulation (EFM) digital output is provided and a 4,3 MHz (typical) clock locked to the disc rate is produced.

### Features

- Phase-locked loop clock regenerator with frequency detector for locking
- High frequency level detector with adaptive slicer for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Outputs to subcoding microprocessor
- Fully protected timing synchronization to incoming data

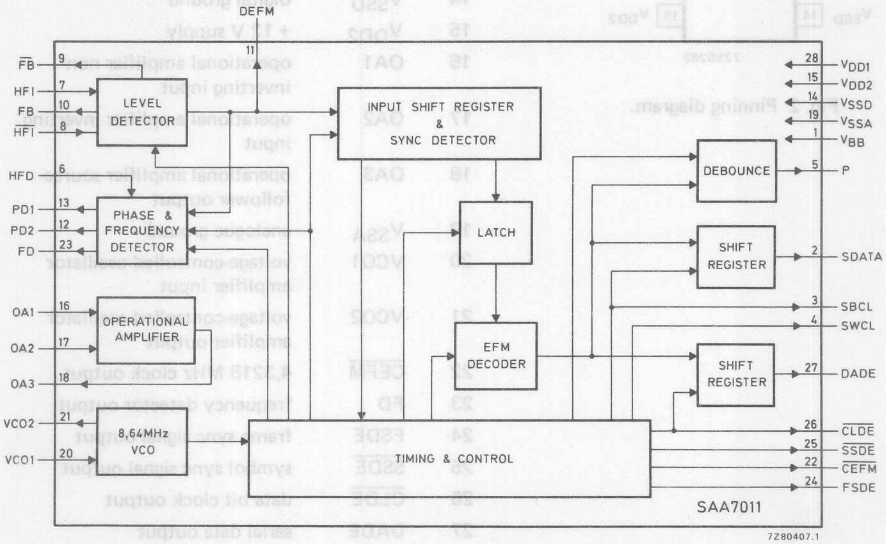



Fig. 1 Block diagram.

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

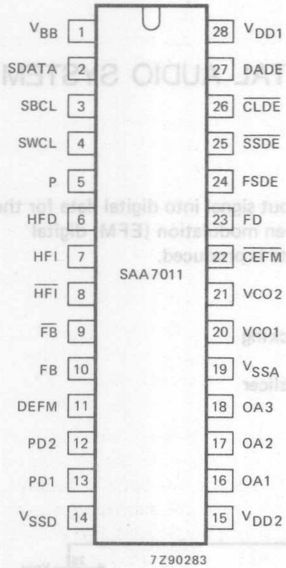



Fig. 2 Pinning diagram.

**PINNING**

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | SDATA | subcoding data output |
| 3 | SBCL | subcoding bit clock output |
| 4 | SWCL | subcoding word clock output |
| 5 | P | subcoding pause bit output |
| 6 | HFD | high-frequency detector input |
| 7 | HFI | level detector non-inverting input |
| 8 | $\overline{\text{HFI}}$ | level detector inverting input |
| 9 | $\overline{\text{FB}}$ | level detector inverted feedback output |
| 10 | FB | level detector non-inverted feedback output |
| 11 | DEFM | EFM digital output |
| 12 | PD2 | phase detector reference output |
| 13 | PD1 | phase detector signal output |
| 14 | $V_{SSD}$ | digital ground |
| 15 | $V_{DD2}$ | + 12 V supply |
| 16 | OA1 | operational amplifier non-inverting input |
| 17 | OA2 | operational amplifier inverting input |
| 18 | OA3 | operational amplifier source-follower output |
| 19 | $V_{SSA}$ | analogue ground |
| 20 | VCO1 | voltage-controlled oscillator amplifier input |
| 21 | VCO2 | voltage-controlled oscillator amplifier output |
| 22 | $\overline{\text{CEFM}}$ | 4,3218 MHz clock output |
| 23 | FD | frequency detector output |
| 24 | FSDE | frame sync signal output |
| 25 | $\overline{\text{SSDE}}$ | symbol sync signal output |
| 26 | $\overline{\text{CLDE}}$ | data bit clock output |
| 27 | DADE | serial data output |
| 28 | $V_{DD1}$ | + 5 V supply |

## FUNCTIONAL DESCRIPTION

The SAA7011 demodulator forms the front-end of the Compact Disc Digital Audio system, supplying demodulated data and timing signals to the error corrector (SAA7020) and to the subcoding micro-processor.

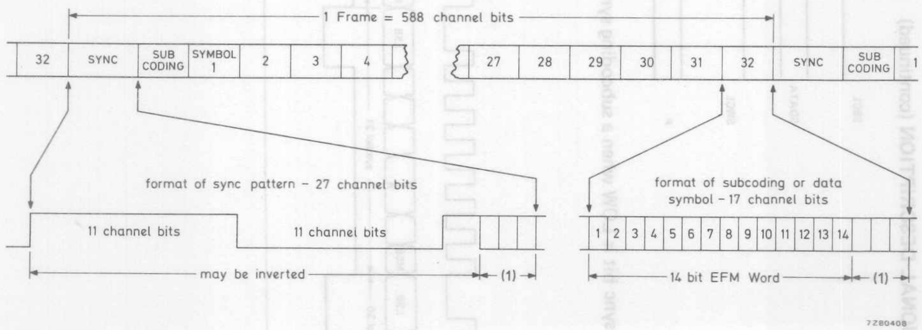
The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. The level detector is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

A frequency detector and a phase detector provide the coarse and fine control signals for the phase-locked loop (PLL) system. The loop gain is supplied by an internal operational amplifier which drives a voltage-controlled oscillator (VCO) running at twice the input data rate (typically 8,6436 MHz). The VCO output is divided by two by a clock generator in the timing and control circuits and the resulting output is used to clock the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.

After phase detection the data is clocked into the 23-bit input shift register which then detects the frame sync pattern. Within the timing and control circuits are minimum and maximum data length detectors which provide frequency limit signals for the frequency detector.

Also within the timing and control circuits are two divide-by-588 counters, one master and one slave, two divide-by-17 symbol rate counters and a lock indication counter. The frame sync signal is used to reset the divide-by-588 slave counter. This counter and one divide-by-17 symbol rate counter supply timing signals for clocking the EFM (eight-to-fourteen modulation) decoder and the subcoding output circuits. The data is read from the input shift register in 14-bit symbols which are first latched and then decoded into 8-bit data words. The subcoding part of the data consists of one word per frame (Fig. 3), so the output SDATA comprises a burst of 8 data bits accompanied by a 2,1906 MHz clock burst signal SBCL (Fig. 4). One bit of this subcoding output data is replaced by a subcoding frame sync bit which is decoded from one of two special EFM codes. The displaced bit (the pause (P) bit) is latched to its own output via a debounce circuit to remove erroneous changes.

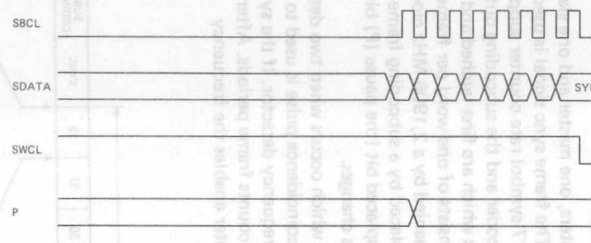
The divide-by-588 slave counter also provides a sync coincidence pulse which occurs when two detected sync pulses are precisely one frame apart (588 clock cycles). The sync coincidence pulse is used to reset the lock indication counter and disable the FD output from the frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.




(1) merging and low frequency suppression bits.

Fig. 3 Data input signal.

FUNCTIONAL DESCRIPTION (continued)




(1) The sync bit is LOW when a subcoding sync word is detected.

Fig. 4 Typical subcoding waveform outputs.

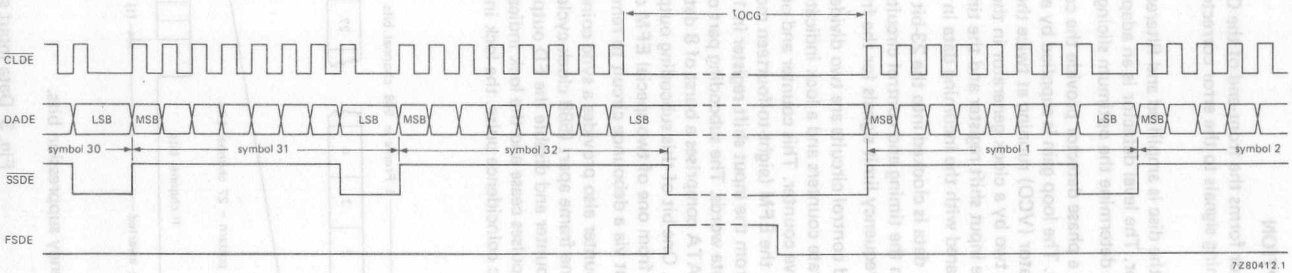



Fig. 5 Typical waveform outputs to SAA7020.

## FUNCTIONAL DESCRIPTION (continued)

A delayed version of the sync coincidence pulse resets the divide-by-588 master counter. This counter is reset only by coincident sync pulses or sync pulses which occur during a predetermined 'window' at the start of each frame and is therefore protected from accidental reset by erroneous sync patterns. The window is wide enough to allow PLL bit-slips but narrow enough to avoid false sync signals generated by corrupt data.

The divide-by-588 master counter and the second divide-by-17 symbol rate counter are used to time the data and clock outputs to the error corrector SAA7020 (Fig. 5). In this way, even if the data has been corrupted, the timing signals will be correct and are only re-synchronized after a complete frame has been sent to SAA7020.

The data output to SAA7020 comprises thirty-two 8-bit symbols per frame, with half-bit gaps between each symbol and a much longer gap during the frame sync period. It is this longer gap that changes in length when corrupt data upsets the timing system.

### Pin functions

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: −2,5 V ± 20%. |
| 2 | SDATA | Subcoding data push-pull output. An 8-bit burst of data (including a 1-bit subcoding frame sync) is output serially once per frame coincident with SBCL. |
| 3 | SBCL | Subcoding bit clock push-pull output. An 8-bit burst clock, typically at 2,1609 MHz, is used to synchronize the subcoding data. |
| 4 | SWCL | Subcoding word clock push-pull output. A square-wave signal at data frame rate (7,35 kHz) used to synchronize the subcoding words and the pause (P) bit. |
| 5 | P | Subcoding pause bit push-pull output. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data. |
| 6 | HFD | External high-frequency detector input. When this signal is HIGH the frequency detector output (FD) and phase detector are enabled. |
| 7 | HFI | Level detector non-inverting input. A differential signal of between 1,0 and 2,5 V (peak-to-peak value) is required to drive the level detector correctly. |
| 8 | $\overline{HFI}$ | Level detector inverting input. |
| 9 | $\overline{FB}$ | Level detector inverted feedback output. The outputs $\overline{FB}$ and FB have a typical impedance of 10 kΩ and will default to 0,5 x $V_{DD1}$ when a drop-out is detected. |
| 10 | FB | Level detector non-inverted feedback output. |
| 11 | DEFM | EFM digital output from the level detector. |
| 12 | PD2 | Phase detector reference signal, typical impedance 15 kΩ. |
| 13 | PD1 | Phase detector output signal, typical impedance 15 kΩ. The differential d.c. content of PD1 and PD2 signals is a measure of the phase difference between the data and the internal 4,3218 MHz clock. |
| 14 | $V_{SSD}$ | Digital ground. Main ground terminal. |
| 15 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |
| 16 | OA1 | Operational amplifier non-inverting input. |
| 17 | OA2 | Operational amplifier inverting input. |

| pin no. | mnemonic | description |
|---|---|---|
| 18 | OA3 | Operational amplifier source follower output. |
| 19 | $V_{SSA}$ | Analogue ground. Ground terminal for operational amplifier and VCO only. Connected internally to $V_{SSD}$ via a 25 Ω (nominal) resistor. |
| 20 | VCO1 | Voltage-controlled oscillator amplifier input. The amplifier is a simple inverter operating up to 10 MHz. Frequency control is achieved via an external tuned circuit using variable capacitance diodes. |
| 21 | VCO2 | Voltage-controlled oscillator amplifier output. The load for the inverting transistor may be turned off for test purposes by reducing $V_{DD2}$ to 0 V. |
| 22 | $\overline{\text{CEFM}}$ | Internal 4,3218 MHz clock generator push-pull output. |
| 23 | FD | Frequency detector three-state push-pull output. This output has a 1 kΩ (typical) impedance when active but assumes a high impedance state once the system is in lock. |
| 24 | FSDE | Frame sync signal push-pull output (to SAA7020). It provides a positive-going pulse at the end of each data frame. Typical frequency = 7,35 kHz. |
| 25 | $\overline{\text{SSDE}}$ | Symbol sync signal push-pull output for each data symbol. Typical frequency = 254 kHz. |
| 26 | CLDE | Data bit clock push-pull output (to SAA7020). An 8-bit clock burst at 2,1609 MHz (typical) which is used to synchronize the data to SAA7020 (see Fig. 5). |
| 27 | DADE | Data push-pull output (to SAA7020). Serial data comprising 32 x 8-bit symbols per frame, synchronized to $\overline{\text{CLDE}}$ (see Fig. 5). |
| 28 | $V_{DD1}$ | Positive supply voltage: + 5 V ± 10%. |

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134);
$V_{SSA} = V_{SSD} = 0$ V

| | | |
|---|---|---|
| Supply voltage 1 range (pin 28) | $V_{DD1}$ | −0,3 to + 7,5 V |
| Supply voltage 2 range (pin 15) | $V_{DD2}$ | −0,3 to + 15 V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to + 0,3 V |
| Input voltage range | $V_I$ | −0,3 to + 7,5 V |
| Output voltage range (except FD, OA3) | $V_O$ | −0,3 to + 7,5 V |
| Output voltage range (FD, OA3 only) | $V_O$ | −0,3 to + 15 V |
| Output current (each output) | $I_O$ | max. 10 mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 70 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## CHARACTERISTICS

$V_{SSA} = V_{SSD} = 0$ V; $T_{amb} = -20$ to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| Supply voltage 1 (pin 28) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 15) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 28) | $I_{DD1}$ | 30 | 60 | 150 | mA |
| Supply current 2 (pin 15) | $I_{DD2}$ | 4 | 8 | 21 | mA |
| Back bias supply current (pin 1) | $-I_{BB}$ | – | – | 500 | μA |
| **DIGITAL CIRCUITS** | | | | | |
| **Input HFD** | | | | | |
| Input voltage LOW | $V_{IL}$ | −0,3 | – | +0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | 6,5 | V |
| Input current (note 1) | $I_I$ | −1 | – | + 1 | μA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Outputs DADE, $\overline{\text{CLDE}}$, FSDE, $\overline{\text{SSDE}}$, SBCL, SDATA, P, SWCL, $\overline{\text{CEFM}}$** (note 2) | | | | | |
| Output voltage LOW at $-I_{OL} = 1,6$ mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH} = 0,2$ mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | – | 150 | pF |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **DIGITAL CIRCUITS** (continued) | | | | | |
| **Output FD** | | | | | |
| Output voltage LOW at $-I_{OL}$ = 100 $\mu$A | $V_{OL}$ | 0 | – | 0,5 | V |
| Output voltage HIGH at $I_{OH}$ = 100 $\mu$A | $V_{OH}$ | 8,0 | – | $V_{DD2}$ + 0,5 | V |
| Output leakage current at $V_O$ = 0 to 6 V (note 3) | $\pm I_L$ | – | – | 1 | $\mu$A |
| Output impedance | $Z_O$ | – | 1 | – | kΩ |
| **Outputs PD1, PD2** | | | | | |
| Output impedance | $Z_O$ | – | 15 | – | kΩ |
| **LEVEL DETECTOR** | | | | | |
| **Inputs HFI, $\overline{\text{HFI}}$** | | | | | |
| A.C. input voltage range (peak-to-peak value) | $V_{I(p-p)}$ | 1,0 | – | 2,5 | V |
| Input offset current (note 4) | $I_{IDF}$ | –0,2 | – | + 0,2 | $\mu$A |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Outputs FB, $\overline{\text{FB}}$** | | | | | |
| Output impedance | $Z_O$ | – | 10 | – | kΩ |
| **OPERATIONAL AMPLIFIER** (note 5) | | | | | |
| **Inputs OA1, OA2** | | | | | |
| Common-mode voltage range | $V_{CIM}$ | 1,5 | – | 6,0 | V |
| Input offset voltage | $\pm V_{IOF}$ | – | 20 | – | mV |
| Input current (note 1) | $\pm I_I$ | – | – | 1 | $\mu$A |
| Input offset current (note 4) | $\pm I_{IOF}$ | – | – | 0,1 | $\mu$A |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Common-mode rejection ratio | CMRR | 40 | – | – | dB |
| Open loop gain (d.c.) | A | 40 | – | – | dB |
| Gain bandwidth product (20 dB/decade roll-off) | | 1 | 5 | – | MHz |
| **Output OA3** | | | | | |
| Output voltage LOW at $-I_{OL}$ = 1 mA | $V_{OL}$ | 0 | – | 1 | V |
| Output voltage HIGH at $I_{OH}$ = 1 mA | $V_{OH}$ | 8,0 | – | $V_{DD2}$ + 0,5 | V |

DEVELOPMENT DATA

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **VCO** | | | | | |
| **Input VCO1, output VCO2** | | | | | |
| Mutual conductance at 100 kHz | $g_m$ | 1,5 | – | – | mA/V |
| Bandwidth (–3 dB cut-off) | $B_{gm}$ | 20 | – | – | MHz |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Output capacitance | $C_O$ | – | – | 7 | pF |
| Feedback capacitance | $C_{FB}$ | – | – | 5 | pF |
| Input leakage current (note 1) | $\pm I_I$ | – | – | 1 | μA |
| Output current at 10 MHz | $\pm I_O$ | – | 1 | – | mA |
| Small-signal voltage gain at 100 kHz | $A_V$ | 4 | – | – | V/V |
| **TIMING** | | | | | |
| Operating frequency (except VCO) | $F_{CEFM}$ | 0,1 | – | 5 | MHz |
| Operating frequency (VCO only) | $F_{VCO}$ | 0,2 | – | 10 | MHz |
| **Outputs $\overline{CLDE}$, DADE, SSDE, FSDE, CEFM** (Fig. 6 and note 6) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 50 | ns |
| Output fall time | $t_{OF}$ | – | – | 40 | ns |
| $\overline{CLDE}$ period | $t_{OCP}$ | 400 | – | – | ns |
| $\overline{CLDE}$ HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| $\overline{CLDE}$ LOW time | $t_{OCL}$ | 150 | – | – | ns |
| DADE/$\overline{SSDE}$/FSDE to $\overline{CLDE}$ set-up time | $t_{ODS}$ | 100 | – | – | ns |
| $\overline{CLDE}$ to DADE/$\overline{SSDE}$/FSDE hold time | $t_{ODH}$ | 100 | – | – | ns |
| $\overline{SSDE}$ LOW time (note 7) | $t_{SSL}$ | – | 3 | – | CEFM period |
| $\overline{CLDE}$ LOW time during FSDE (Fig. 5 and note 8) | $t_{OCG}$ | 16 | 46 | – | CEFM period |
| **Outputs SBCL, SDATA, P, SWCL** (Fig. 7) | | | | | |
| Output rise time (SBCL, SDATA) (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (SBCL, SDATA) (note 6) | $t_{OF}$ | – | – | 40 | ns |
| Output rise time (P, SWCL) (note 9) | $t_{OSR}$ | – | – | 200 | ns |
| Output fall time (P, SWCL) (note 9) | $t_{OSF}$ | – | – | 200 | ns |
| SBCL HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| SBCL LOW time | $t_{OCL}$ | 150 | – | – | ns |
| SDATA to SBCL set-up time | $t_{ODS}$ | 100 | – | – | ns |
| P to SWCL set-up time | $t_{ODSP}$ | 1 | – | – | ns |
| SBCL to SDATA hold time | $t_{ODH}$ | 100 | – | 500 | ns |
| SBCL to SWCL hold time | $t_{SWH}$ | 0 | – | – | μs |
| SWCL duty cycle ($t_{HIGH}/t_{period}$) | | 40 | 50 | 60 | % |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **TIMING** (continued) | | | | | |
| **Output FD** | | | | | |
| Output rise time (note 6) | $t_{FDR}$ | – | – | 1 | μs |
| Output fall time (note 6) | $t_{FDF}$ | – | – | 1 | μs |
| **Outputs DEFM, $\overline{\text{CEFM}}$** (Fig. 8) | | | | | |
| Output rise time (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (note 6) | $t_{OF}$ | – | – | 40 | ns |
| DEFM to $\overline{\text{CEFM}}$ set-up time (note 10) | $t_{ODS}$ | 50 | – | – | ns |
| $\overline{\text{CEFM}}$ to DEFM hold time (note 10) | $t_{ODH}$ | 70 | – | – | ns |
| $\overline{\text{CEFM}}$ HIGH time | $t_{OCH}$ | 50 | – | – | ns |
| $\overline{\text{CEFM}}$ LOW time | $t_{OCL}$ | 50 | – | – | ns |

NOTES TO THE CHARACTERISTICS

1. At $T_{amb}$ = 25 °C; $V_{IN}$ = –0,3 to + 6,5 V; $V_{DD1}$ = 6,5 V.
2. Short-circuit protected to $V_{DD1}$ and $V_{SS}$. The maximum load capacitance that can be applied before short-circuit protection becomes operative is 150 pF.
3. At $T_{amb}$ = 25 °C; output in high impedance state.
4. At $T_{amb}$ = 25 °C.
5. All tests performed within common-mode voltage range.
6. Output loading = 50 pF.
7. $\overline{\text{SSDE}}$ remains LOW for only one negative edge of $\overline{\text{CLDE}}$.
8. Excessive bit-slip may cause gap to disappear. $\overline{\text{CLDE}}$ remains LOW when FSDE is HIGH.
9. Output loading = 150 pF.
10. Free running VCO frequency tuned to nominal and PLL in lock with a typical application circuit.

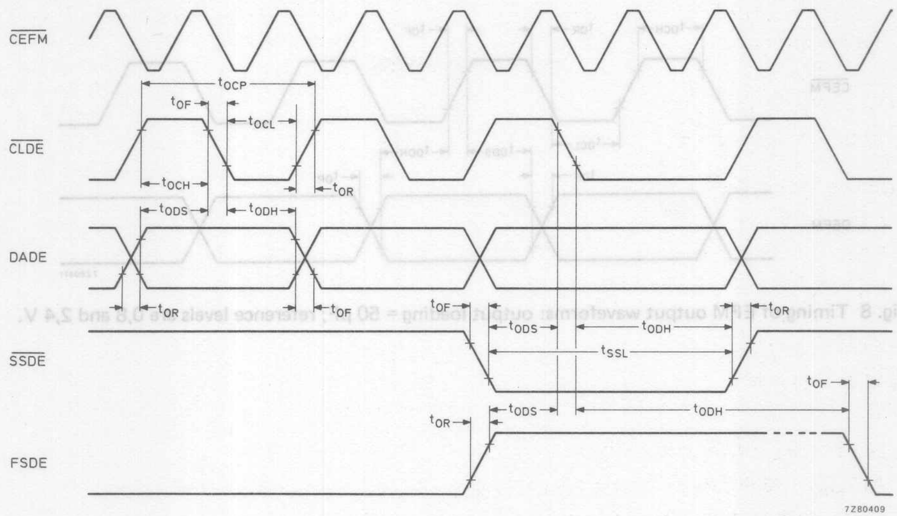



Fig. 6 Timing of waveform outputs to SAA7020.

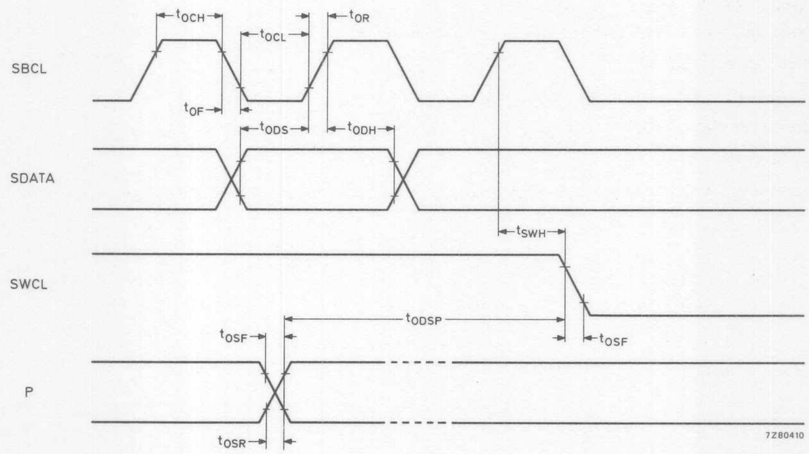



Fig. 7 Timing of waveform outputs for subcoding: reference levels are 0,8 and 2,4 V; SBCL and SDATA output loading = 50 pF; SWCL and P output loading = 150 pF; SWCL has a 50% duty cycle.

DEVELOPMENT DATA

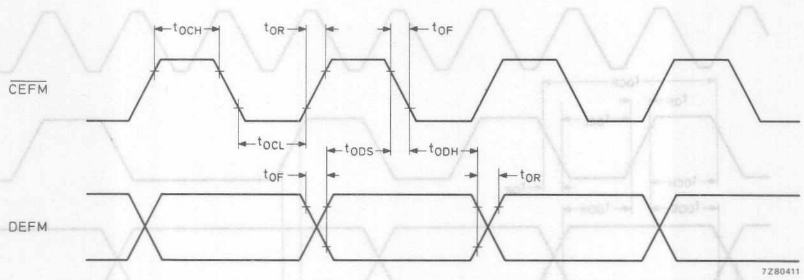



Fig. 8 Timing of EFM output waveforms: output loading = 50 pF; reference levels are 0,8 and 2,4 V.

# ERROR CORRECTOR FOR COMPACT DISC DIGITAL AUDIO SYSTEM

## GENERAL DESCRIPTION

The SAA7020 detects and corrects errors in digital data received from the demodulator (SAA7010). The data is received serially in frames of 32 x 8-bit symbols and, after processing, is transmitted in a 16-bit serial format to the interpolating and muting circuit (SAA7000). An error flag is generated to warn of data in which errors have not been corrected.

### Features

- Internal timing and control circuits
- Serial data input and output
- 8-bit bidirectional data bus to external RAM (2K x 8 bits)
- Corrects up to seven erroneous frames of data
- Generates error flag to identify unreliable data
- Provides a motor speed control output which stabilizes the input data rate and eliminates wow and flutter.

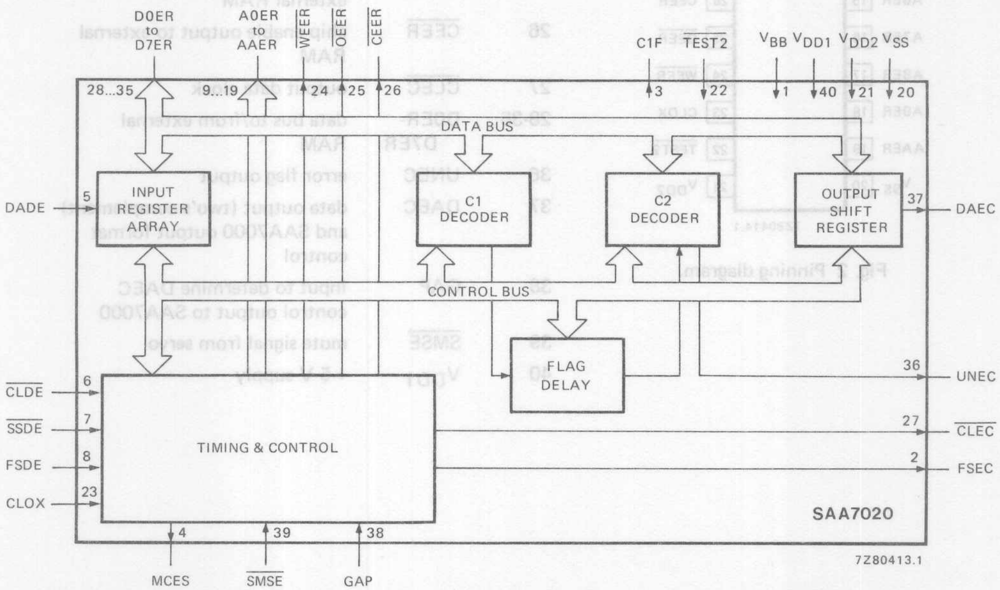



Fig. 1 Block diagram.

## PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

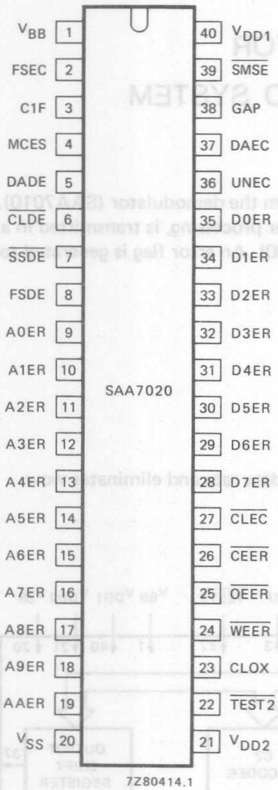



Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | FSEC | frame sync pulse output |
| 3 | C1F | C1 decoder error flag |
| 4 | MCES | motor speed control output |
| 5 | DADE | serial data input |
| 6 | $\overline{\text{CLDE}}$ | data bit clock input |
| 7 | $\overline{\text{SSDE}}$ | symbol sync signal input |
| 8 | FSDE | frame sync signal input |
| 9-19 | A0ER-AAER | address outputs to external RAM |
| 20 | $V_{SS}$ | ground |
| 21 | $V_{DD2}$ | + 12 V supply |
| 22 | $\overline{\text{TEST2}}$ | test input |
| 23 | CLOX | basic clock input |
| 24 | $\overline{\text{WEER}}$ | write enable output to external RAM |
| 25 | $\overline{\text{OEER}}$ | output enable signal to external RAM |
| 26 | $\overline{\text{CEER}}$ | chip enable output to external RAM |
| 27 | $\overline{\text{CLEC}}$ | output data clock |
| 28-35 | D0ER-D7ER | data bus to/from external RAM |
| 36 | UNEC | error flag output |
| 37 | DAEC | data output (two's complement) and SAA7000 output format control |
| 38 | GAP | input to determine DAEC control output to SAA7000 |
| 39 | $\overline{\text{SMSE}}$ | mute signal from servo |
| 40 | $V_{DD1}$ | +5 V supply |

## FUNCTIONAL DESCRIPTION

The SAA7020 error corrector receives data samples from the Compact Disc Digital Audio demodulating system (SAA7010), processes the data samples and then passes them to the interpolating and muting circuit (SAA7000). The processing detects erroneous data and then, if possible, corrects the errors. If error correction is not possible, a flag (UNEC) is generated to warn of unreliable data output. The SAA7020 also controls the motor speed of the disc drive servo.

Serial data received from the demodulator (SAA7010) is arranged in frames of 32 x 8-bit symbols; 24 of the symbols contain audio samples, the remaining eight symbols contain parity information for error detection/correction. The data (DADE) is clocked into the input register array at the demodulator rate by $\overline{\mathrm{CLDE}}$. The input register array comprises a register which accumulates symbols ready for parallel output to an external RAM and a FIFO register which acts as a jitter reduction circuit.

The jitter reduction circuit uses the difference between the input data rate ($\overline{\mathrm{CLDE}}$) and the system data rate (derived from CLOX) to generate the motor speed control signal $\overline{\mathrm{MCES}}$ (Fig. 3). This forms a feedback loop with the disc drive motor to control the disc speed and hence the input data rate. In this way unwanted effects such as wow and flutter are eliminated from the Compact Disc system, the FIFO being capable of handling deviations from the system data rate of up to ± 2 frames.

An 8-bit bidirectional bus is used for transferring data to and from the external RAM (2K x 8 bits) and an 11-bit bus for addressing. Three bits control the RAM; write enable $\overline{\mathrm{WEER}}$, output enable $\overline{\mathrm{OEER}}$ and chip enable $\overline{\mathrm{CEER}}$ (the latter is for operation with dynamic RAMs).

The error correction process makes use of data interleaving and two Reed-Solomon codes, C1 and C2. The C1 decoder can correct one erroneous symbol in a 32-symbol frame after de-interleaving; the C2 decoder can correct two erroneous symbols in a group of 28 symbols. Input data is de-interleaved and read from the RAM by the C1 decoder where syndromes are formed to check for erroneous symbols. If one error is detected it is corrected and the data is written back to the RAM with some parity symbols being discarded. If more than one error is detected the data is written back to the RAM unchanged but internal C1 flags are set to mark these symbols as unreliable. The data in the RAM is then further de-interleaved and read back to the C2 decoder. The symbols are then checked for errors as previously, if one error is detected it is corrected and the symbols are again written back to the RAM. If two error flags are detected erasure correction is attempted when the flags are received from C1. The corrected data is then written back to the RAM. If more than two symbols are in error the data is written back to the RAM unchanged but a flag is set to mark these symbols as unreliable. At this stage the remaining parity bits are discarded.

After processing, the data is held in the RAM to give a 5-frame delay so that the error warning flag UNEC can be sent to the interpolation and muting circuit (SAA7000). The UNEC flag is also output when $\overline{\mathrm{SMSE}}$ is active, this warns of data to be immediately muted. At the end of the 5-frame delay, the data is read back to the output shift register to be serially shifted out at DAEC.

**Pin functions**

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: −2,5 V ± 20%. |
| 2 | FSEC | Frame sync pulse output, data is valid on the falling edge (Figs 5 and 9). |
| 3 | C1F | This output pin flags uncorrectable C1 errors. |
| 4 | MCES | Motor control error signal; this open drain output provides a pulse width modulated signal to control the rate of data entry. If the data rate has been correct for a period, MCES duty cycle = 50%; if low, the duty cycle < 50%; if high, the duty cycle > 50% (Fig. 3). |
| 5 | DADE | Serial data input. The data is clocked in by $\overline{\text{CLDE}}$ in 8-bit symbols, the most-significant bit first (Figs 4 and 6). |
| 6 | $\overline{\text{CLDE}}$ | Data clock input, data is accepted into DADE on the negative transition of $\overline{\text{CLDE}}$ (Figs 4 and 6). |
| 7 | $\overline{\text{SSDE}}$ | Input indicating the last bit of a symbol. A symbol is counted and clocked in when $\overline{\text{SSDE}}$ is LOW during the negative transition of $\overline{\text{CLDE}}$; for correct operation, $\overline{\text{SSDE}}$ must remain LOW for only one negative transition in eight (Figs 4 and 6). |
| 8 | FSDE | Input indicating the end of a data frame. Indication is given when FSDE is HIGH during a negative transition of $\overline{\text{CLDE}}$. |
| 9-19 | A0ER-AAER | Eleven address outputs to the external RAM. When data is being received at DADE, $\overline{\text{CLDE}}$, etc. then addresses A0ER to AAER are completely exercised every four frames allowing refresh to be automatic for dynamic RAMs (Figs 7 and 8). |
| 20 | $V_{SS}$ | Ground. |
| 21 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |
| 22 | TEST2 | Test input. Connect to $V_{DD1}$ or $V_{DD2}$ for normal operation. |
| 23 | CLOX | System clock input, typical frequency = 4,2336 MHz (Fig. 6). |
| 24 | $\overline{\text{WEER}}$ | Write enable output to external RAM; when LOW, SAA7020 is writing to the RAM (Fig. 7). |
| 25 | $\overline{\text{OEER}}$ | Output enable to external RAM; when HIGH, memory output buffers must be in the high impedance state (Figs 7 and 8). |
| 26 | $\overline{\text{CEER}}$ | Chip enable output for use with dynamic memories (Figs 7 and 8). |
| 27 | $\overline{\text{CLEC}}$ | Output data clock; data is valid on the falling edge (Figs 5 and 9). |
| 28-35 | D0ER-D7ER | Input/output ports for 8-bit bidirectional bus from/to external RAM. The outputs are in the high impedance state when $\overline{\text{OEER}}$ is LOW (Figs 7 and 8). |
| 36 | UNEC | Error flag output; when HIGH, indicates that output data is unreliable. During active data output (i.e. when $\overline{\text{CLEC}}$ is operating) UNEC applies to each symbol of 8 bits of data output at that time. Before each data word of two symbols is output, UNEC applies to the whole data word that will follow in five frames time. |

FUNCTIONAL DESCRIPTION (continued)

| pin no. | mnemonic | description |
|---|---|---|
| 37 | DAEC | Serial data output. Data is clocked out by $\overline{CLEC}$ and is in 16-bit words separated by gaps. Each word is in two's complement format with the most-significant bit first and comprises two 8-bit symbols. Data is valid on the falling edge of $\overline{CLEC}$. During the gap between the data words, the state of pin 38 (GAP) acts as an output from DAEC (Figs 5 and 9). |
| 38 | GAP | The input level at this pin is reflected in the state of the output from DAEC between data words and is used to control the output format of the SAA7000. When GAP is HIGH, DAEC gap level is HIGH, and vice versa (Fig. 5). |
| 39 | $\overline{SMSE}$ | Select muting input. If $\overline{SMSE}$ is held LOW, the UNEC output will be held HIGH causing the interpolation and muting circuit (SAA7000) to mute the data. |
| 40 | $V_{DD1}$ | Positive supply voltage: + 5 V ± 10%. |

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); $V_{SS}$ = 0 V

| | | |
|---|---|---|
| Supply voltage 1 range (pin 40) | $V_{DD1}$ | −0,3 to + 7,5 V |
| Supply voltage 2 range (pin 21) | $V_{DD2}$ | −0,3 to + 15 V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to + 0,3 V |
| Input voltage range (except TEST) | $V_I$ | −0,3 to + 7,5 V |
| Input voltage range (TEST only) | $V_I$ | −0,3 to + 15 V |
| Output voltage range (except MCES) | $V_O$ | −0,3 to + 7,5 V |
| Output voltage range (MCES only) applied through a 10 kΩ resistor | $V_O$ | −0,35 to + 15 V |
| Output current | $I_O$ | max. 10 mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 70 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

DEVELOPMENT DATA

## CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = –20 to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supplies** | | | | | |
| Supply voltage 1 (pin 40) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 21) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 40) | $I_{DD1}$ | – | 145 | 280 | mA |
| Supply current 2 (pin 21) | $I_{DD2}$ | – | 14 | 26 | mA |
| Back bias supply current (pin 1) | $-I_{BB}$ | | | 500 | μA |
| **Inputs** (except D0ER-D7ER) | | | | | |
| Input voltage LOW | $V_{IL}$ | –0,3 | – | + 0,8 | V |
| Input voltage HIGH (except $\overline{SMSE}$) | $V_{IH}$ | 2,4 | – | 6,5 | V |
| Input voltage HIGH ($\overline{SMSE}$ only) | $V_{IH}$ | 2,0 | – | 6,5 | V |
| Input current (note 1) | $I_I$ | –1 | – | + 1 | μA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Input/output D0ER-D7ER** | | | | | |
| Input voltage LOW | $V_{IL}$ | –0,3 | – | + 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | 6,5 | V |
| Input current (notes 1 and 2) | $I_I$ | –10 | – | + 10 | μA |
| Input capacitance | $C_I$ | – | – | 10 | pF |
| Output voltage LOW at $-I_{OL}$ = 1,6 mA (notes 3 and 4) | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH}$ = 0,2 mA (notes 3 and 4) | $V_{OH}$ | 3,0 | | $V_{DD1}$ +0,5 | V |
| Load capacitance (notes 3 and 4) | $C_L$ | – | – | 150 | pF |
| **Outputs A0ER-AAER, $\overline{WEER}$, $\overline{OEER}$, $\overline{CEER}$, DAEC, UNEC, FSEC, $\overline{CLEC}$** (notes 3 and 4) | | | | | |
| Output voltage LOW at $-I_{OL}$ = 1,6 mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH}$ = 0,2 mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | – | 150 | pF |
| **Output MCES** (open drain) (note 5) | | | | | |
| Output voltage LOW with pin 4 connected to $V_{DD2}$ via a 10 kΩ resistor | $V_{OL}$ | 0 | – | 0,4 | V |
| Output current with output OFF and pin 4 connected to $V_{DD2}$ via a 10 kΩ resistor; $T_{amb}$ = 25 °C | $I_{OH}$ | – | – | 20 | μA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Input CLOX** (note 6) | | | | | |
| Operating frequency | $f_{IN}$ | 3,0 | 4,2336 | 4,5 | MHz |
| Input clock LOW | $t_{IXL}$ | 40 | – | – | ns |
| Input clock HIGH | $t_{IXH}$ | 40 | – | – | ns |
| **Inputs DADE, $\overline{\text{CLDE}}$, $\overline{\text{SSDE}}$, FSDE** (note 7) | | | | | |
| Input rise time | $t_{IR}$ | – | – | 50 | ns |
| Input fall time | $t_{IF}$ | – | – | 50 | ns |
| $\overline{\text{CLDE}}$ period | $t_{ICP}$ | 1 CLOX period | – | 20 | μs |
| $\overline{\text{CLDE}}$ HIGH | $t_{ICH}$ | 100 | | | ns |
| $\overline{\text{CLDE}}$ LOW | $t_{ICL}$ | 100 | – | | ns |
| DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time | $t_{IDS}$ | 50 | | | ns |
| $\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time | $t_{IDH}$ | 80 | | | ns |
| $\overline{\text{SSDE}}$ LOW time | $t_{SSL}$ | – | 1 | | $\overline{\text{CLDE}}$ period |
| $\overline{\text{CLDE}}$ gap after FSDE | $t_{FCG}$ | 6 | – | – | CLOX periods |
| **Input $\overline{\text{SMSE}}$** (note 7) | | | | | |
| Input rise time | $t_{IR}$ | – | 1 | 100 | μs |
| Input fall time | $t_{IF}$ | – | 1 | 100 | μs |
| SMSE to UNEC output delay time | $t_{SMD}$ | – | – | 20 | CLOX periods |
| **Outputs $\overline{\text{CLEC}}$, DAEC, UNEC, FSEC** (notes 3, 4, 7 and 8) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 50 | ns |
| Output fall time | $t_{OF}$ | – | – | 40 | ns |
| $\overline{\text{CLEC}}$ HIGH | $t_{OCH}$ | 130 | – | 350 | ns |
| $\overline{\text{CLEC}}$ LOW | $t_{OCL}$ | 130 | | | ns |
| FSEC HIGH | $t_{FSH}$ | 6 CLOX periods −180 | – | 6 CLOX periods + 180 | ns |
| $\overline{\text{CLEC}}$ to FSEC delay time | $t_{CFD}$ | 3 CLOX periods −300 | | 3 CLOX periods + 300 | ns |
| DAEC/UNEC to FSEC set-up time | $t_{UFS}$ | 100 | – | – | ns |
| FSEC to DAEC/UNEC hold time | $t_{UFH}$ | 12 | – | – | CLOX periods |

DEVELOPMENT DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **RAM interfaces A0ER-AAER, D0ER-D7ER, $\overline{\text{OEER}}$, $\overline{\text{CEER}}$, $\overline{\text{WEER}}$** (notes 3, 4 and 7) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 30 | ns |
| Output fall time | $t_{OF}$ | – | – | 25 | ns |
| Cycle time | $t_{C}$ | 390 | | 670 | ns |
| *Read cycle timing* | | | | | |
| $\overline{\text{CEER}}$ HIGH time | $t_{CEH}$ | 65 | – | – | ns |
| $\overline{\text{CEER}}$ LOW time | $t_{CEL}$ | 265 | – | – | ns |
| A0ER-AAER to $\overline{\text{CEER}}$ set-up time | $t_{ACS}$ | 0 | – | – | ns |
| $\overline{\text{CEER}}$ to A0ER-AAER hold time | $t_{ACH}$ | 300 | – | – | ns |
| D0ER-D7ER to $\overline{\text{OEER}}$ set-up time | $t_{DOS}$ | 85 | – | – | ns |
| $\overline{\text{OEER}}$ to D0ER-D7ER hold time | $t_{DOH}$ | 0 | – | – | ns |
| D0ER-D7ER to A0ER-AAER set-up time | $t_{DAS}$ | 85 | – | – | ns |
| A0ER-AAER to D0ER-D7ER hold time | $t_{DAH}$ | 0 | – | – | ns |
| $\overline{\text{OEER}}$ to D0ER-D7ER from RAM active | $t_{OLZ}$ | 0 | – | – | ns |
| $\overline{\text{OEER}}$ to D0ER-D7ER from RAM high impedance state | $t_{OHZ}$ | 0 | – | 100 | ns |
| $\overline{\text{OEER}}$ LOW to A0ER-AAER valid | $t_{OAD}$ | –25 | – | + 25 | ns |
| *Write cycle timing* | | | | | |
| $\overline{\text{CEER}}$ HIGH time | $t_{CEH}$ | 196 | – | – | ns |
| $\overline{\text{CEER}}$ LOW time | $t_{CEL}$ | 196 | – | – | ns |
| A0ER-AAER to $\overline{\text{CEER}}$ set-up time | $t_{ACS}$ | 100 | – | – | ns |
| A0ER-AAER to $\overline{\text{WEER}}$ set-up time | $t_{AWS}$ | 50 | – | – | ns |
| $\overline{\text{WEER}}$ to A0ER-AAER hold time | $t_{AWH}$ | 50 | – | – | ns |
| $\overline{\text{WEER}}$ to $\overline{\text{CEER}}$ set-up time | $t_{WCS}$ | 50 | – | – | ns |
| $\overline{\text{CEER}}$ to $\overline{\text{WEER}}$ hold time | $t_{WCH}$ | 65 | – | – | ns |
| D0ER-D7ER to $\overline{\text{CEER}}$ set-up time | $t_{DCS}$ | 50 | – | – | ns |
| $\overline{\text{CEER}}$ to D0ER-D7ER hold time | $t_{DCH}$ | 150 | – | – | ns |
| $\overline{\text{WEER}}$ to $\overline{\text{CEER}}$ recovery time | $t_{WR}$ | 65 | – | – | ns |
| D0ER-D7ER to $\overline{\text{WEER}}$ set-up time | $t_{DWS}$ | 150 | – | – | ns |
| $\overline{\text{WEER}}$ to D0ER-D7ER hold time | $t_{DWH}$ | 100 | – | – | ns |
| $\overline{\text{OEER}}$ to D0ER-D7ER output active | $t_{DOZ}$ | 100 | – | – | ns |
| $\overline{\text{OEER}}$ to D0ER-D7ER output in high impedance state | $t_{ODZ}$ | 20 | – | – | ns |

## NOTES TO THE CHARACTERISTICS

1. Measured from −0,3 to + 6,5 V at $T_{amb}$ = 25 °C; $V_{DD1}$ = 6,5 V.
2. Input/output port in high impedance state (OFF); measured from 0 to 6 V at $T_{amb}$ = 25 °C.
3. Output loading: 1 TTL gate + $C_L$ = 50 pF.
4. All outputs are protected against short-circuit to $V_{SS}$ and $V_{DD1}$. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
5. Phase detector gain for average MCES output voltage = 1,1 V per frame. Phase detector control range = ± 2 frames.
6. All maximum or minimum values assume respective frequency where appropriate.
7. Reference levels = 0,8 V and 2,4 V.
8. The DAEC level during the advanced UNEC period is defined by the state at pin 38 (GAP). If this state changes during $\overline{\text{CLEC}}$ LOW, the timings are applicable. If the state at pin 38 changes at other times, DAEC follows with a delay of between 20 and 500 ns.

DEVELOPMENT DATA

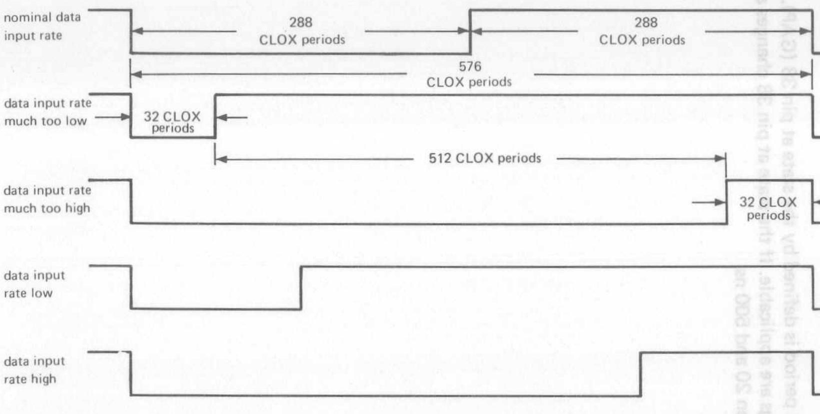



Fig. 3 MCES output waveforms: waveforms are updated each frame (576 CLOX periods); open drain output, rise times depend on external pull-up circuit. This output has an internal clamp to prevent the voltage at pin 4 (MCES) rising above $V_{DD2}$ + 1,8 V maximum.

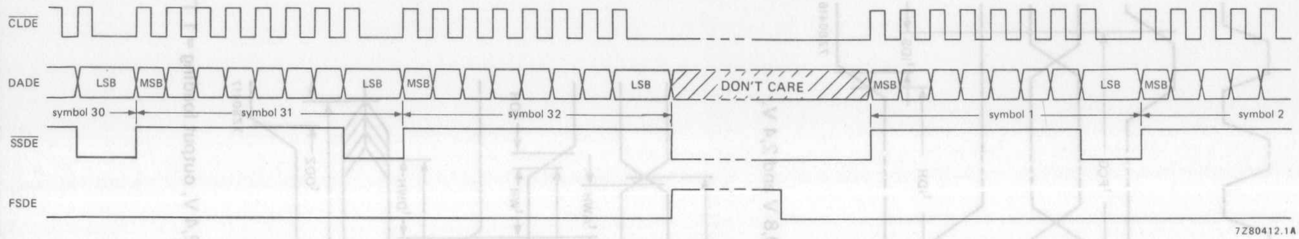
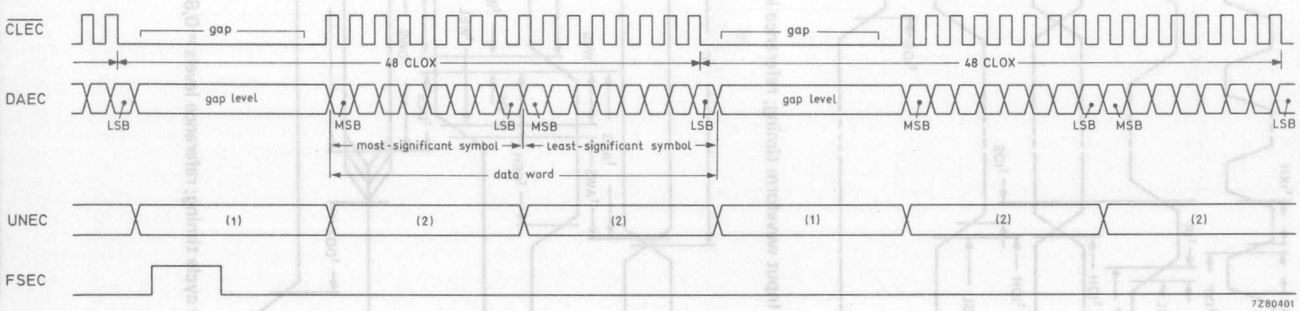



Fig. 4 Typical input waveforms from SAA7010/SAA7011.




(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.

Fig. 5 Typical output waveforms to SAA7000.

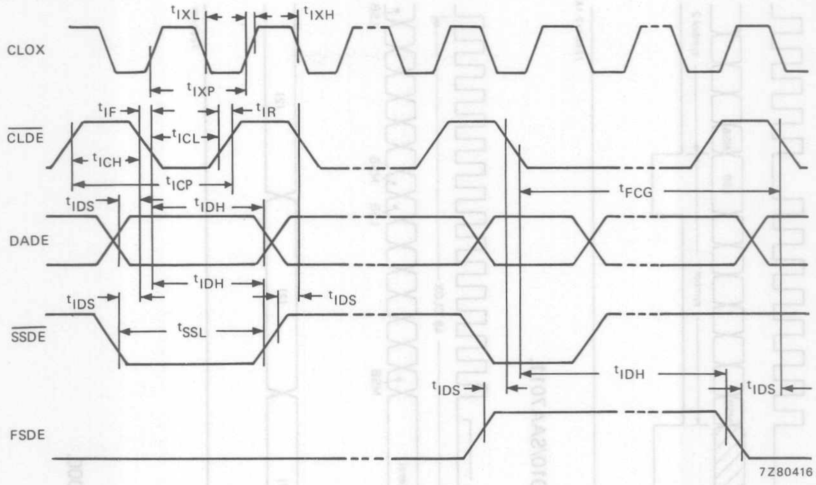



Fig. 6 Input waveform timing; reference levels = 0,8 V and 2,4 V.

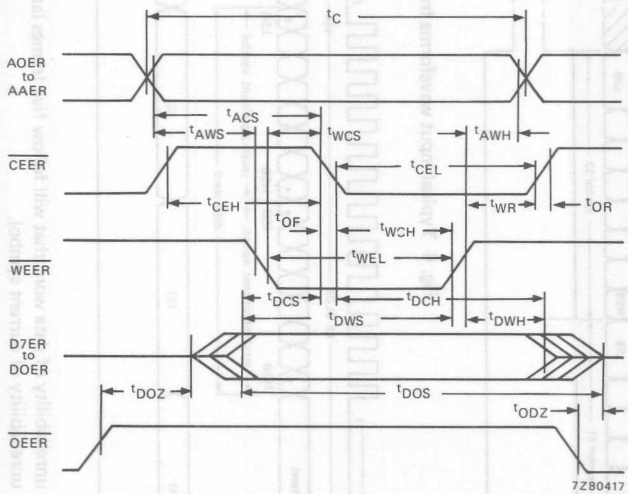



Fig. 7 RAM interface write cycle timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and $C_L$ = 50 pF.

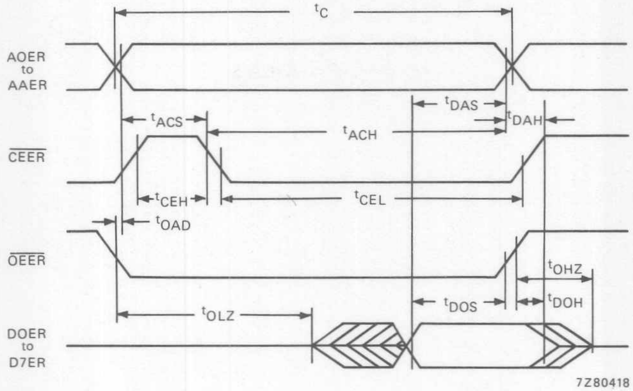
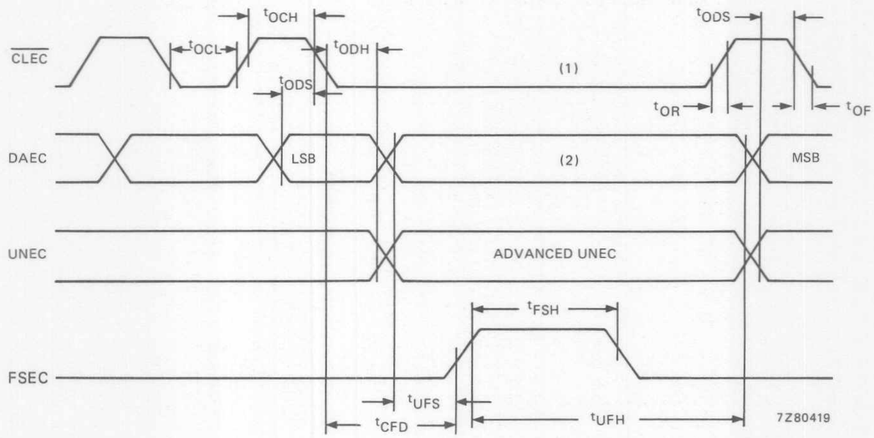



Fig. 8 RAM interface read cycle timing; reference levels = 0,8 V and 2,4 V; output loading = 1 TTL gate and $C_L$ = 50 pF; $\overline{WEER}$ is HIGH during read cycle.




(1) $\overline{CLEC}$ remains LOW for 8 $\overline{CLEC}$ cycle periods.
(2) DAEC level during this period is defined by the level on pin 38 (GAP). If GAP changes during $\overline{CLEC}$ active, the above timings apply. If GAP changes at other times, DAEC follows with a delay of 20 to 500 ns.

Fig. 9 Output waveform timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and $C_L$ = 50 pF.

# DIGITAL FILTER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

## GENERAL DESCRIPTION

The SAA7030 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. The circuit incorporates two identical filters, each with a sampling rate of four times that of the normal digital audio sampling.

### Features

- Suppresses spurious lobes in the audio spectrum
- Improves the signal quality for digital-to-analogue conversion
- Allows a low-order analogue post filter to be used after the digital-to-analogue convertor (DAC)
- Option of offset binary or two's complement data output format
- Electrically-selectable d.c. offset/no offset on data output
- Overflow detection and protection
- Directly compatible with the interpolation and muting circuit (SAA7000)
- Generates a latch output strobe to the DAC

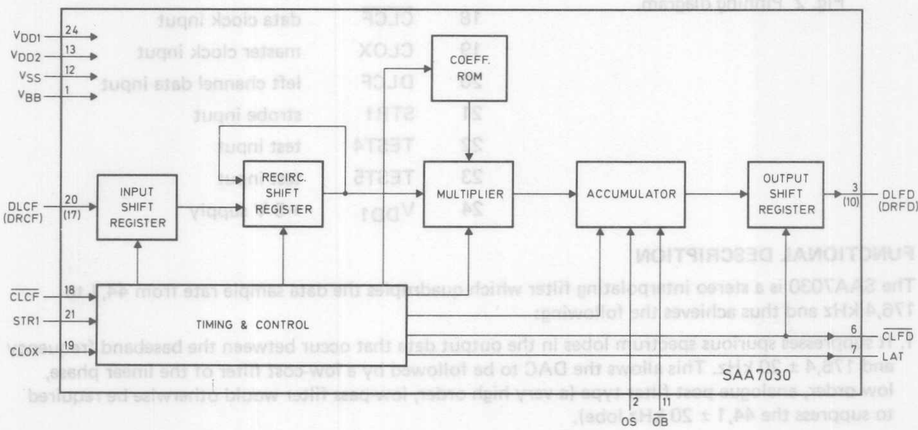



Fig. 1 Block diagram.

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

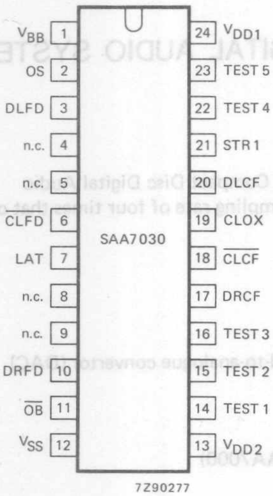



Fig. 2 Pinning diagram.

**PINNING**

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | OS | offset/no offset select input |
| 3 | DLFD | left channel data output |
| 4 | n.c. | not connected |
| 5 | n.c. | not connected |
| 6 | $\overline{\text{CLFD}}$ | data clock output |
| 7 | LAT | strobe output |
| 8 | n.c. | not connected |
| 9 | n.c. | not connected |
| 10 | DRFD | right channel data output |
| 11 | $\overline{\text{OB}}$ | offset binary/two's complement select input |
| 12 | $V_{SS}$ | ground |
| 13 | $V_{DD2}$ | + 12 V supply |
| 14 | TEST1 | test output |
| 15 | TEST2 | test input |
| 16 | TEST3 | test input |
| 17 | DRCF | right channel data input |
| 18 | $\overline{\text{CLCF}}$ | data clock input |
| 19 | CLOX | master clock input |
| 20 | DLCF | left channel data input |
| 21 | STR1 | strobe input |
| 22 | TEST4 | test input |
| 23 | TEST5 | test input |
| 24 | $V_{DD1}$ | + 5 V supply |

**FUNCTIONAL DESCRIPTION**

The SAA7030 is a stereo interpolating filter which quadruples the data sample rate from 44,1 to 176,4 kHz and thus achieves the following:

1. It suppresses spurious spectrum lobes in the output data that occur between the baseband frequency and 176,4 ± 20 kHz. This allows the DAC to be followed by a low-cost filter of the linear phase, low order, analogue post filter type (a very high order, low-pass filter would otherwise be required to suppress the 44,1 ± 20 kHz lobe).
2. It performs noise-shaping so that a 14-bit DAC yields the same in-band quantizing signal-to-noise ratio as from a 16-bit DAC supplied with unprocessed 44,1 kHz samples.

The circuit incorporates two identical filters (one per channel). Each is a finite impulse response, linear phase transversal filter. The filter length is 96 bits with 16-bit data words and 12-bit coefficients. The composition of each filter is as follows:

serial-to-parallel input shift register;
sixteen 24-bit shift registers for data storage;
96 x 12-bit coefficient ROM;
12 x 16-bit array multiplier;
28-bit accumulator;
parallel-to-serial output shift register.

Overflow protection is incorporated in the filters so that, in the unlikely event of accumulator overflow, the output limits cleanly. Overflow only occurs if the input samples continuously reverse sign coincidently with the coefficients, so that the products of the two entered into the accumulator are continually of the same sign.

The data inputs may run asynchronously with the master clock (CLOX) provided that the data inputs are always complete before the rising edge of the 44,1 kHz input strobe (STR1). A 176,4 kHz output strobe (LAT) is provided, the rising edge of which follows the completion of the serial output data stream. This strobe pulse is timed to be used to gate the master clock (CLOX) if required.

The input OS provides selection of –3% d.c. offset or no offset of the data output voltage level. The format of the output data is selected via the input $\overline{OB}$ to be in offset binary or two's complement form.

DEVELOPMENT DATA

**Pin functions**

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: –2,5 V ± 20%. |
| 2 | OS | Offset select input. When connected to $V_{DD1}$, the data output has a fixed d.c. offset of –3%. When connected to $V_{SS}$, the data output has no offset. |
| 3 | DLFD | Left channel data output. The data is 14-bit serial with most-significant bit first and is valid on the falling edge of the output clock ($\overline{CLFD}$). |
| 6 | $\overline{CLFD}$ | Data clock output. Typical frequency = 4,2336 MHz ( = CLOX). The falling edge of this clock defines output data valid. |
| 7 | LAT | Strobe output at 176,4 kHz. The rising edge of this pulse indicates that the output of a 14-bit data word is complete. |
| 10 | DRFD | Right channel data output (see DLFD). |
| 11 | $\overline{OB}$ | Offset binary/two's complement select input. When connected to $V_{SS}$, the output data is coded in offset binary. When connected to $V_{DD1}$, the output data is coded in two's complement. |
| 12 | $V_{SS}$ | Ground (0 V). |
| 13 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |
| 14 | TEST1 | Test output; not used in normal operation. |
| 15 | TEST2 | Test input; in normal operation this pin should be connected to $V_{SS}$ or $V_{DD1}$. |
| 16 | TEST3 | Test input; in normal operation this pin should be connected to $V_{SS}$ or $V_{DD1}$. |
| 17 | DRCF | Right channel data input. Data should be 16-bit serial with most-significant-bit first and in offset binary code. It is valid on the falling edge of the input data clock ($\overline{CLCF}$). |
| 18 | $\overline{CLCF}$ | Input data clock. The falling edge of this clock defines input data valid. |
| 19 | CLOX | Master clock input. Runs continuously at a typical frequency of 4,2336 MHz. |
| 20 | DLCF | Left channel data input (see DRCF). |

FUNCTIONAL DESCRIPTION (continued)

| pin no. | mnemonic | description |
|---|---|---|
| 21 | STR1 | Strobe input at 44,1 kHz. The internal timing chain of the SAA7030 is synchronized by the rising edge of STR1 which must be synchronous with CLOX within the tolerance specified in CHARACTERISTICS. The rising edge should follow the completion of the input data stream. |
| 22 | TEST4 | Test input; in normal operation this pin should be connected to $V_{DD1}$. |
| 23 | TEST5 | Test input; in normal operation this pin should be connected to $V_{DD1}$. |
| 24 | $V_{DD1}$ | Positive supply voltage: + 5 V ± 10%. |

Pins 4, 5, 8 and 9 have no internal connection.

## HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); $V_{SS} = 0$ V

| | | |
|---|---|---|
| Supply voltage 1 range (pin 24) | $V_{DD1}$ | −0,3 to + 7,5 V |
| Supply voltage 2 range (pin 13) | $V_{DD2}$ | −0,3 to + 15 V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to + 0,3 V |
| Input voltage range | $V_I$ | −0,3 to + 7,5 V |
| Output voltage range | $V_O$ | −0,3 to + 7,5 V |
| Output current | $I_O$ | max. 10 mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 70 °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 °C |

## CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = -20$ to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supplies** | | | | | |
| Supply voltage 1 (pin 24) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 13) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 24) | $I_{DD1}$ | 50 | 120 | 240 | mA |
| Supply current 2 (pin 13) | $I_{DD2}$ | 3,5 | 8,0 | 15,0 | mA |
| Back bias supply current (pin 1) at $V_{DD1} \leq 5,5$ V; $V_{DD2} \leq 13,2$ V | $-I_{BB}$ | – | – | 500 | μA |
| **Inputs** | | | | | |
| Input voltage LOW | $V_{IL}$ | −0,3 | – | + 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | 6,5 | V |
| Input current at $T_{amb} = 25$ °C; $V_I = -0,3$ to + 6,5 V | $\pm I_I$ | – | – | 1 | μA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Outputs** (note 1) | | | | | |
| Output voltage LOW at $-I_{OL} = 1,6$ mA | $V_{OL}$ | −0,3 | – | + 0,4 | V |
| Output voltage HIGH at $I_{OH} = 0,2$ mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | 50 | 150 | pF |
| **Input CLOX** | | | | | |
| Operating frequency | $f_{IX}$ | 1,0 | 4,23 | 4,5 | MHz |
| Input clock LOW | $t_{IXL}$ | 25 | – | – | % of $t_{IXP}$ |
| Input clock HIGH | $t_{IXH}$ | 25 | – | – | % of $t_{IXP}$ |

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Inputs $\overline{CLCF}$, DLCF, DRCF, STR1** | | | | | |
| $\overline{CLCF}$ frequency | $f_{IC}$ | 0,1 | 2,12 | 4,50 | MHz |
| $\overline{CLCF}$ LOW time | $t_{ICL}$ | 75 | – | – | ns |
| $\overline{CLCF}$ HIGH time | $t_{ICH}$ | 75 | – | – | ns |
| DLCF/DRCF to $\overline{CLCF}$ set-up time | $t_{IDS}$ | 25 | – | – | ns |
| $\overline{CLCF}$ to DLCF/DRCF hold time | $t_{IDH}$ | 75 | – | – | ns |
| $\overline{CLCF}$ LOW to STR1 time | $t_{CSL}$ | 0 | – | – | ns |
| STR1 LOW time | $t_{ISL}$ | 4 | – | – | CLOX |
| STR1 HIGH time | $t_{ISH}$ | 1 | – | – | cycles |
| CLOX to STR1 rising | $t_{XSL}$ | –5 | – | – | ns |
| CLOX to STR1 HIGH | $t_{XSH}$ | – | – | 55 | ns |
| **Outputs $\overline{CLFD}$, DRFD, DLFD, LAT** (notes 2 and 3) | | | | | |
| Output rise time (except LAT) | $t_{OR}$ | – | 10 | 30 | ns |
| Output fall time (except LAT) | $t_{OF}$ | – | 8 | 15 | ns |
| Output rise time (LAT only) | $t_{LR}$ | – | 7 | 15 | ns |
| Output fall time (LAT only) | $t_{LF}$ | – | 6 | 10 | ns |
| $\overline{CLFD}$ HIGH time | $t_{OCH}$ | 40 | 75 | – | ns |
| $\overline{CLFD}$ LOW time | $t_{OCL}$ | 40 | 105 | – | ns |
| DRFD/DLFD to $\overline{CLFD}$ set-up time | $t_{ODS}$ | 20 | 70 | – | ns |
| $\overline{CLFD}$ to DRFD/DLFD hold time | $t_{ODH}$ | 50 | 120 | – | ns |
| $\overline{CLFD}$ LOW prior to LAT rising | $t_{CLD}$ | 100 | 350 | – | ns |
| CLOX to LAT starting to change (note 4) | $t_{XLS}$ | 0 | 30 | – | ns |
| CLOX to LAT reaching final value | $t_{XLF}$ | 0 | 80 | – | ns |
| $\overline{CLFD}$ LOW to rising edge of CLOX with rising edge to STR1 | $t_{XCL}$ | 50 | 400 | – | ns |
| LAT HIGH time | $t_{LH}$ | – | 1 | – | CLOX cycle |

NOTES TO THE CHARACTERISTICS

1. All outputs are protected against short-circuit to $V_{SS}$ and $V_{DD1}$. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
2. Output loading $C_L$ = 50 pF.
3. Reference levels are 0,8 and 2 V.
4. Rising edge of LAT occurs in the first CLOX LOW period following the rising edge to STR1 and then recurs at every 24th CLOX cycle.

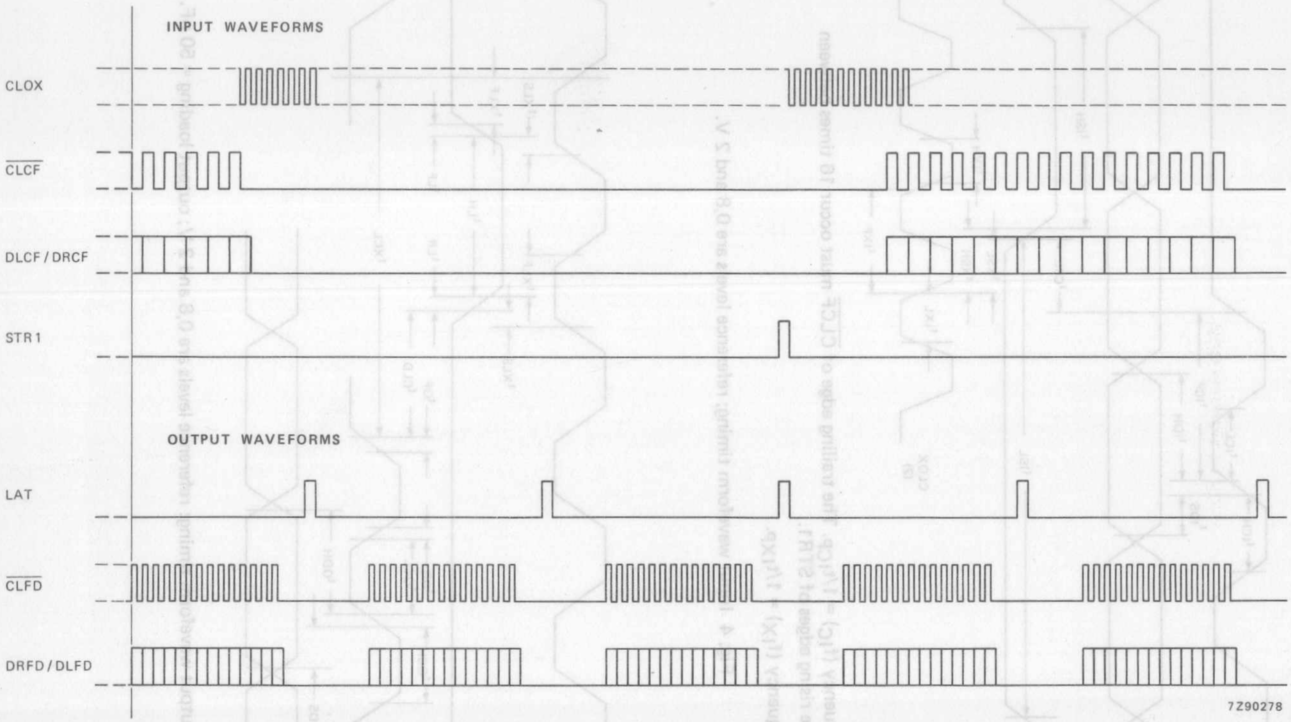
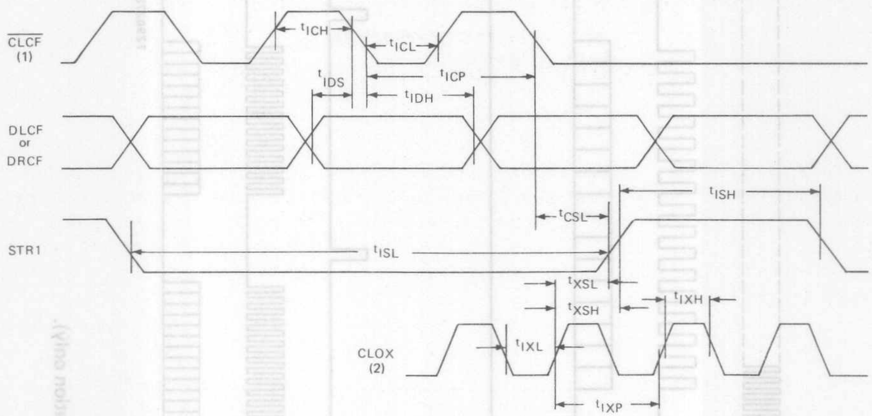



Fig. 3 Typical input and output waveforms (for illustration only).




(1) $\overline{CLCF}$ frequency ($f_{IC}$) = $1/t_{ICP}$. The trailing edge of $\overline{CLCF}$ must occur 16 times between consecutive rising edges of STR1.

(2) CLOX frequency ($f_{IX}$) = $1/t_{IXP}$.

Fig. 4 Input waveform timing; reference levels are 0,8 and 2 V.

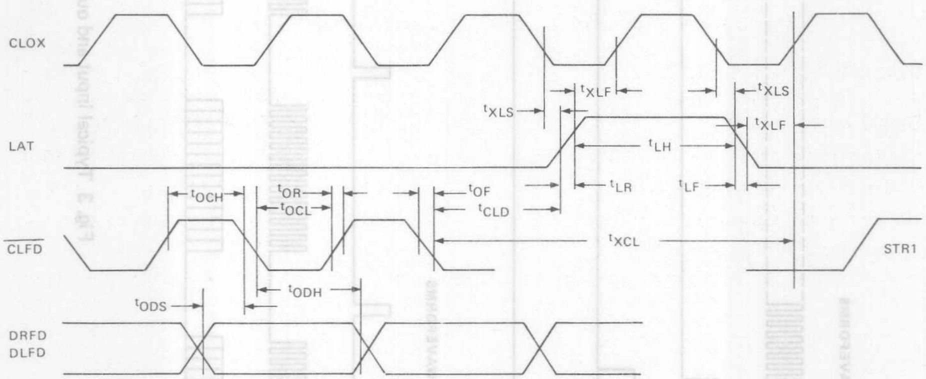



Fig. 5 Output waveform timing: reference levels are 0,8 and 2 V; output loading = 50 pF.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# SENSITIVE 1 GHz DIVIDER-BY-64

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 $^{o}$C. It features a high sensitivity and low harmonic contents of the output signal. The difference between SAB1164 and SAB1165 is the output resistance (see Fig. 7)

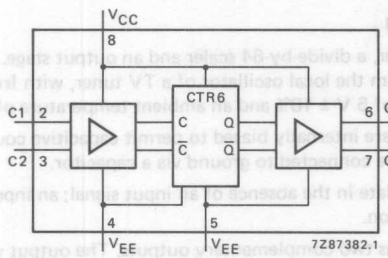



Fig. 1 Block diagram. CTR6 = 6 binary dividers = (÷ 64).

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 8) | $V_{CC}$ | | 5 ± 10% V |
| Input frequency range (pins 2 and 3) | $f_i$ | | 70 to 1000 MHz |
| Output voltage swing (pins 6 and 7) | $V_{o(p-p)}$ | typ. | 1 V |
| Supply current; unloaded (pin 8) | $I_{CC}$ | typ. | 42 mA |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 70 $^{o}$C |

## PACKAGE OUTLINES

SAB1164P: 8-lead DIL; plastic (SOT-97A).
SAB1165P: 8-lead DIL; plastic (SOT-97A).

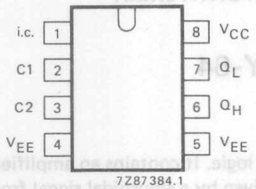



Fig. 2 Pinning diagram.

**PINNING**

| | |
|---|---|
| $V_{CC}$ | positive supply |
| $V_{EE}$ | 0 V; ground |
| $C_1$, $C_2$ | differential inputs |
| $Q_H$, $Q_L$ | complementary outputs |
| i.c. | internally connected |

## FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the $V_{CC}$ pin to ground are recommended.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (d.c.) | $V_{CC}$ | max. | 7 | V |
| Input voltage | $V_i$ | | 0 to $V_{CC}$ | V |
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Junction temperature | $T_j$ | max. | 125 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From crystal to ambient | $R_{th\ c\text{-}a}$ | = | 120 | K/W |

## D.C. CHARACTERISTICS

$V_{EE}$ = 0 V (ground); $V_{CC}$ = 5 V; $T_{amb}$ = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

| | | | | |
|---|---|---|---|---|
| Output voltage | | | | |
| HIGH level | $V_{OH}$ | max. | $V_{CC}$ | V |
| LOW level | $V_{OL}$ | max. | $V_{CC}$−0,8 | V |
| Supply current | $I_{CC}$ | typ. | 42 | mA |
| | | max. | 50 | mA |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# SENSITIVE 1 GHz DIVIDER-BY-256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

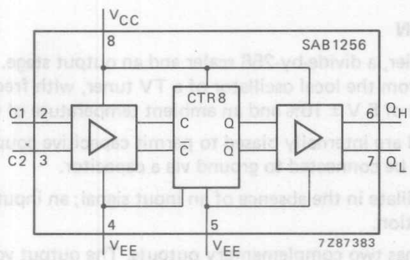



Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 8) | $V_{CC}$ | | 5 ± 10% V |
| Input frequency range (pins 2 and 3) | $f_i$ | | 70 to 1000 MHz |
| Output voltage swing (pins 6 and 7) | $V_{o(p-p)}$ | typ. | 1 V |
| Supply current, unloaded (pin 8) | $I_{CC}$ | typ. | 47 mA |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 70 °C |

## PACKAGE OUTLINE

SAB1256P: 8-lead DIL; plastic (SOT-97A).

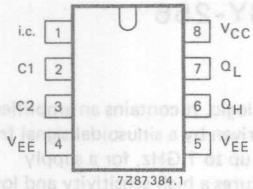



Fig. 2 Pinning diagram.

PINNING

| | |
|---|---|
| $V_{CC}$ | positive supply |
| $V_{EE}$ | 0 V; ground |
| $C_1$, $C_2$ | differential inputs |
| $Q_H$, $Q_L$ | complementary outputs |
| i.c. | internally connected |

## FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the $V_{CC}$ pin to ground are recommended.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (d.c.) | $V_{CC}$ | max. | 7 V |
| Input voltage | $V_i$ | | 0 to $V_{CC}$ V |
| Storage temperature | $T_{stg}$ | | −55 to + 125 °C |
| Junction temperature | $T_j$ | max. | 125 °C |

## THERMAL RESISTANCE

| | | |
|---|---|---|
| From crystal to ambient | $R_{th\ c\text{-}a}$ | = 120 K/W |

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.

Features:

SAF1032P receiver/decoder:

- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:

- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

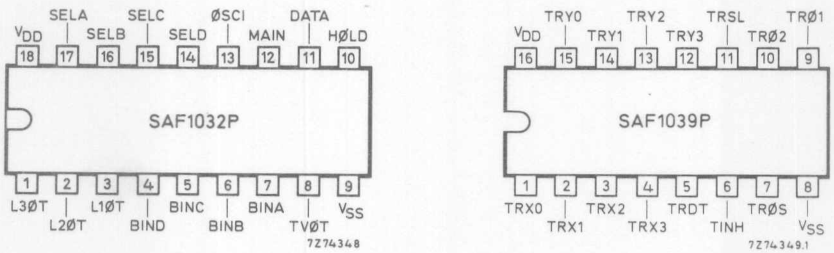



Fig. 1 Pin designations.

## PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102A).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

**PINNING**

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

**SAF1032P**

| | | | | | |
|---|---|---|---|---|---|
| 1 | L3ØT | linear output | 10 | HØLD | control input |
| 2 | L2ØT | linear output | 11 | DATA | data input |
| 3 | L1ØT | linear output | 12 | MAIN | reset input |
| 4 | BIND | binary 8 output | 13 | ØSCI | clock input |
| 5 | BINC | binary 4 output | 14 | SELD | binary 8 output |
| 6 | BINB | binary 2 output | 15 | SELC | binary 4 output |
| 7 | BINA | binary 1 output | 16 | SELB | binary 2 output |
| 8 | TVØT | on/off input/output | 17 | SELA | binary 1 output |
| 9 | $V_{SS}$ | | 18 | $V_{DD}$ | |

**SAF1039P**

| | | | | | |
|---|---|---|---|---|---|
| 1 | TRX0 | keyboard input | 9 | TRØ1 | oscillator control input |
| 2 | TRX1 | keyboard input | 10 | TRØ2 | oscillator control input |
| 3 | TRX2 | keyboard input | 11 | TRSL | keyboard select line |
| 4 | TRX3 | keyboard input | 12 | TRY3 | keyboard input |
| 5 | TRDT | data output | 13 | TRY2 | keyboard input |
| 6 | TINH | inhibit output/mode select input | 14 | TRY1 | keyboard input |
| 7 | TRØS | oscillator output | 15 | TRY0 | keyboard input |
| 8 | $V_{SS}$ | | 16 | $V_{DD}$ | |

# SERVO-MOTOR CONTROL CIRCUIT

## GENERAL DESCRIPTION

The SAK150BT is a bipolar integrated circuit intended for remote control applications in digital proportional systems or other closed-loop position control applications, in which it will translate the width of its input pulses into a mechanical position. It incorporates a linear one-shot for improved positional accuracy. The circuit has additional outputs for driving external p-n-p transistors to form a bidirectional bridge.

**Features**

- high output current
- bidirectional bridge output facility with single power supply
- adjustable deadband
- adjustable proportional range
- high linearity
- wide supply voltage range
- low standby supply current
- provides stabilized supply for external circuit

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | | 3 to 9 | V |
| Supply current, standby, at $V_{CC}$ = 4,8 V | $I_{CC}$ | typ. | 3 | mA |
| Stabilized supply voltage for external circuit | $V_Z$ | typ. | 2 | V |
| Output current at $V_{CC}$ = 4,8 V | $I_O$ | max. | 500 | mA |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

## PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

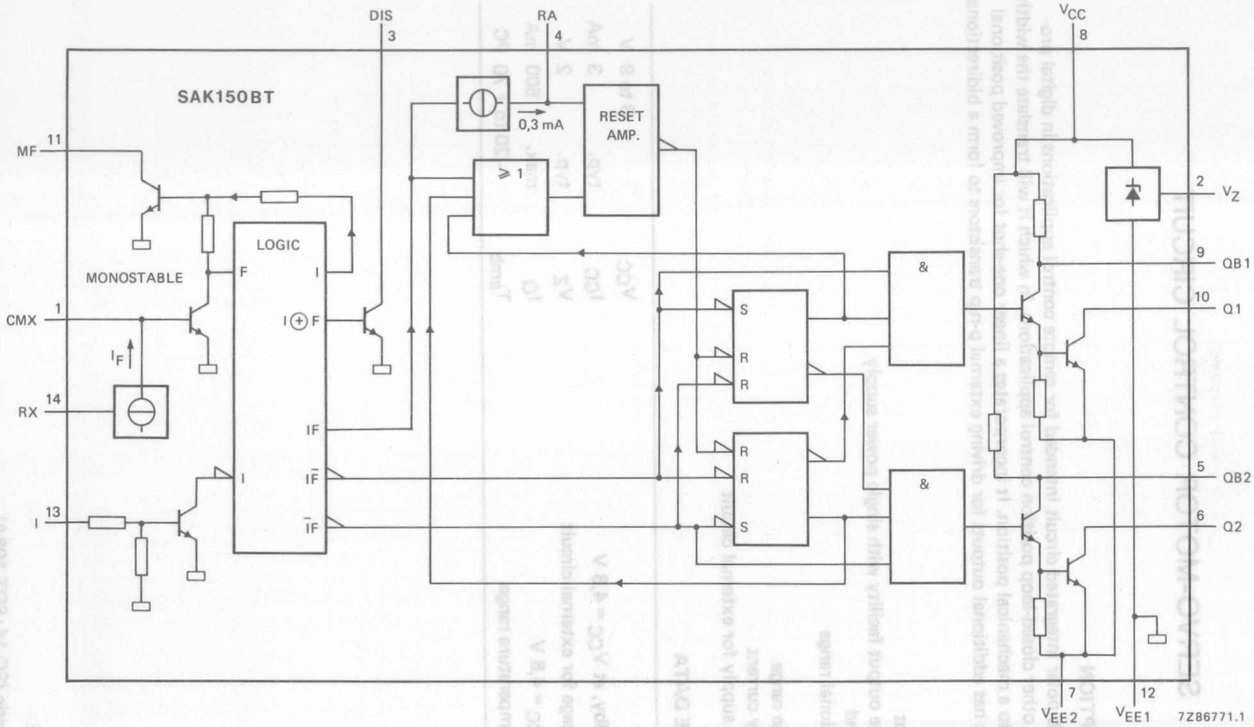



Fig. 1 Block diagram. The blocks marked "&" are AND gates, the block marked "≥ 1" is an OR gate, the blocks with inputs marked S and R are set-reset flip-flops and the block marked "RESET AMP" may be considered as a high-gain amplifier for the upper input with the lower input giving a small shift of the switching level of the upper input. The triangles at some of the inputs and outputs are polarity indicators showing that the internal logic 1-state at that input or output corresponds with the external logic L-level (LOW). At inputs and outputs without polarity indicator the internal logic 1-state corresponds with the external logic H-level (HIGH).

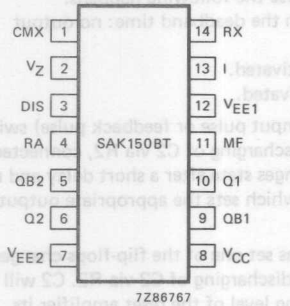



Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | CMX | external monostable capacitor |
| 2 | $V_Z$ | stabilized voltage output |
| 3 | DIS | discharging resistor |
| 4 | RA | reset amplifier |
| 5 | QB2 | p-n-p driver output |
| 6 | Q2 | power output |
| 7 | $V_{EE2}$ | ground of output stage |
| 8 | $V_{CC}$ | positive supply |
| 9 | QB1 | p-n-p driver output |
| 10 | Q1 | power output |
| 11 | MF | monostable feedback |
| 12 | $V_{EE1}$ | ground of circuit (except output stage) |
| 13 | I | input |
| 14 | RX | external resistor |

## FUNCTIONAL DESCRIPTION (See also Fig. 5)

The SAK150BT has two sets of outputs on which it is capable of producing output pulses of variable width. The output arrangement is such that these output pulses can drive a servo-motor in both directions. The servo-motor actuates a potentiometer. The width of the output pulses is reduced to zero when the position of the potentiometer slider corresponds with the width of the input pulses.

The circuit operates as follows. The positive-going leading edges of the input pulses trigger a monostable element. Its output pulses have a duration that is a linear function of the position of the potentiometer slider. These pulses therefore will be referred to as feedback pulses.

The presence of both the input pulse and the feedback pulse switches on a current source of approx. 0,3 mA which charges an external capacitor C2 connected from RA (pin 4) to ground. The variation of the voltage on this capacitor after some time causes the output of the high-gain reset amplifier to change state and reset the two output flip-flops.

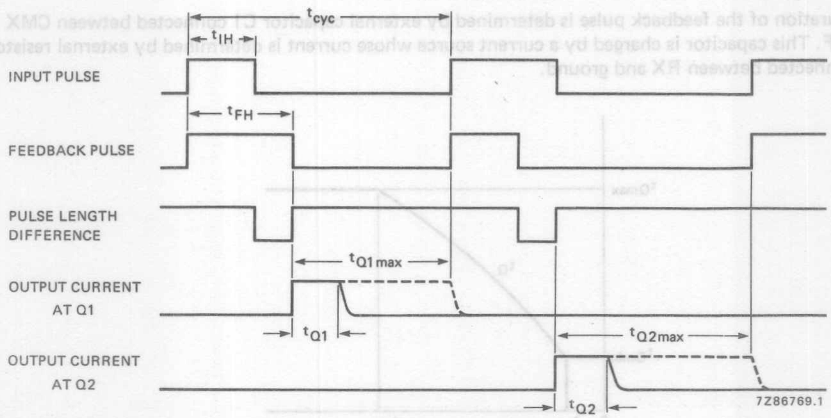



Fig. 3 Timing diagram.

Depending on the relative durations of input pulse and feedback pulse the following happens.

1. Difference in duration of input pulse and feedback pulse less than the deadband time: no output signals generated.
2. Input pulse shorter than feedback pulse: outputs Q1 and QB1 activated.
3. Input pulse longer than feedback pulse: outputs Q2 and QB2 activated.

The trailing (negative-going) edge of the shorter of the two pulses (input pulse or feedback pulse) switches off the current source that charged C2. It further switches on the discharging of C2 via R2, connected to DIS (pin 3). As a consequence the output of the reset amplifier changes state after a short delay and no longer resets the flip-flops. Finally the logic bloc generates a signal which sets the appropriate output flip-flop but inhibits the output.

At the trailing edge of the longer of the two pulses the signal that has set one of the flip-flops changes state. This enables the corresponding output. It further finishes the discharging of C2 via R2. C2 will now be charged via R32. When the voltage on C2 reaches the switching level of the reset amplifier its output signal will reset the flip-flops again and this will terminate the output pulse (see Fig. 3). The duration of the output pulse is proportional with the charge required by C2 to reach the switching level of the reset amplifier, and this charge is proportional to the time that C2 has been discharged via R2, i.e. the difference in duration of the input pulse and the feedback pulse.

The maximum output pulse duration is reached when the output pulse is terminated by the next input pulse.

**Supply: $V_{CC}$, $V_{EE1}$, $V_{EE2}$ and $V_Z$** (pins 8, 12, 7 and 2)

The SAK150BT contains a voltage stabilizer. This permits the circuit to be used over a very wide supply voltage range without substantial variation of its performance. The stabilized supply voltage is available at $V_Z$ (pin 2) to supply an external peripheral circuit, e.g. a feedback potentiometer.

The circuit has two ground pins, one for the output stage ($V_{EE2}$) and one for the rest of the circuit ($V_{EE1}$).

**Input I** (pin 13)

Input pulses should be positive-going, i.e. the time that the input signal is HIGH is the input parameter. Usual values are 1 to 2 ms for the pulse to be HIGH and 20 ms for the pulse repetition time.

**Feedback pulse duration: CMX, MF and RX** (pins 1, 11 and 4)

The duration of the feedback pulse is determined by external capacitor C1 connected between CMX and MF. This capacitor is charged by a current source whose current is determined by external resistor R1 connected between RX and ground.

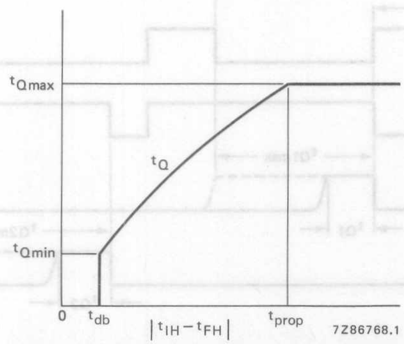



Fig. 4 Output current pulse duration.

The output current pulse duration $t_Q$ as a function of the difference between input pulse duration $t_{IH}$ and feedback pulse duration $t_{FH}$ in Fig. 4. There is no output signal for differences less than the deadband time $t_{db}$. The maximum output pulse duration ($t_{Qmax}$) at outputs Q1 and Q2 is equal to $t_{cyc}$-$t_{dB}$. The maximum pulse duration is reached at a pulse duration difference $t_{prop}$ minus $t_{IH}$ respectively $t_{FH}$.

**Deadband time**

The deadband time is the maximum difference in duration between the input pulse and the feedback pulse that will not give an output signal (see Fig. 4). The deadband time is determined by external resistor and capacitor R2 and C2 connected to RA and by the switching level $V_{SW}$ of the reset amplifier and by its switching level shift $\Delta V_{SW}$, according to the following approximative formula:

$$t_{db} \approx R2 \times C2 \times \ln\left(\frac{V_{SW} + \Delta V_{SW}}{V_{SW}}\right) \approx \frac{R_2 \times C_2}{50}.$$

**Proportional range**

The output pulse width is proportional to the difference of the input pulse and the internal pulse. The range is

$$t_{prop} \approx R2 \times C2 \times \ln\left(1 - \frac{(V_{CC}{}^* - V_{SW})\,(e^{tCVC/R3 \times C2} - 1)}{V_{SW}}\right)$$

in which: $V_{CC}{}^* = \dfrac{V_{CC} - V_Z}{R31 + R32} \times R31 + V_Z$ and $R3 = \dfrac{R31 \times R32}{R31 + R32}$.

The maximum pulse width is limited by the beginning of the new input pulse.
The minimum pulse width is

$$t_{Qmin} \approx R3 \times C2 \times \ln\left(1 - \frac{\Delta V_{SW}}{V_{CC}{}^* - V_{SW} + \Delta V_{SW}}\right).$$

**Outputs Q1, CB1, Q2 and QB2** (pins 10, 9, 6 and 5)

The outputs Q1 and Q2 are open-collector outputs capable of sinking up to 500 mA. The outputs QB1 and QB2 are intended to drive external p-n-p transistors. Together with the Q outputs these p-n-p transistors may form a bidirectional bridge output with a single power supply, see Fig. 4.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage, d.c. | $V_{CC}$ | max. | 12 | V |
| Current at $V_Z$ | $-I_{VZ}$ | max. | 3 | mA |
| Input voltage | $V_I$ | max. | 12 | V |
| | $-V_I$ | max. | 5 | V |
| Voltage at CMX | $-V_{CMX}$ | max. | 5 | V |
| Current at CMX | $I_{CMX}$ | max. | 5 | mA |
| Current at RX | $-I_{RX}$ | max. | 1 | mA |
| Voltage at MF | $V_{MF}$ | max. | 12 | V |
| Current at MF | $I_{MF}$ | max. | 3 | mA |
| | $-I_{MF}$ | max. | 3 | mA |
| Current at RA | $I_{RA}$ | max. | 6 | mA |
| | $-I_{RA}$ | max. | 5 | mA |
| Output voltage, Q1 and Q2 | $V_Q$ | max. | 24 | V |
| Output current, Q1 and Q2, repetitive peak | $I_{QRM}$ | max. | 800 | mA |
| | $-I_Q$ | max. | 10 | $\mu$A |
| Output voltage, QB1 and QB2 | $V_{QB}$ | max. | 12 | V |
| Output current, QB1 and QB2 | $I_{QB}$ | max. | 70 | mA |
| | $-I_{QB}$ | max. | 10 | mA |
| Storage temperature range | $T_{stg}$ | | −35 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

$V_{CC}$ = 3 to 9 V; $V_{EE1}$ = $V_{EE2}$ = 0 V; $T_{amb}$ = −20 to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply: $V_{CC}$ and $V_Z$** (pins 8 and 2) | | | | | |
| Supply current at $V_{CC}$ = 4,8 V; $T_{amb}$ = 25 °C; output stages OFF | $I_{CC}$ | – | 3 | – | mA |
| Stabilized voltage output | $V_Z$ | – | 1,95 | – | V |
| Variation with temperature | $\Delta V_Z/\Delta T$ | – | 6 | – | mV/K |
| Output current at $V_{CC}$ = 4,8 V for $\Delta V_Z$ = 60 mV | $-I_Z$ | – | – | 1 | mA |
| **Input I** (pin 13) | | | | | |
| Input voltage | | | | | |
| HIGH | $V_{IH}$ | 2,4 | – | – | V |
| LOW | $V_{IL}$ | – | – | 0,6 | V |
| Input current | | | | | |
| HIGH at $V_I$ = 2,4 V | $I_{IH}$ | – | – | 250 | μA |
| LOW at $V_I$ = 0,6 V | $-I_{IL}$ | – | – | 30 | μA |
| **External resistor pin RX** (pin 14) | | | | | |
| Voltage at $-I_{RX}$ = 100 μA | $V_{RX}$ | – | 0,7 | – | V |
| Current range | $I_{RX}$ | 10 | – | 200 | μA |
| **Monostable feedback pin MF** (pin 11) | | | | | |
| Voltage at $I_{MF}$ = 2 mA | $V_{MF}$ | – | – | 300 | mV |
| Output current | $I_{MF}$ | – | – | 3 | mA |
| **Reset amplifier pin RA** (pin 4) | | | | | |
| Switching level of reset amplifier, | $V_{sw}$ | – | 1,9 | – | V |
| Shift of switching level | $\Delta V_{SW}$ | – | 40 | – | mV |
| Input current | | | | | |
| HIGH | $I_{RA}$ | – | – | 6 | mA |
| LOW | $-I_{RA}$ | – | 300 | – | μA |
| **External monostable capacitor pin CMX** (pin 1) | | | | | |
| Current | $I_{CMX}$ | – | – | 1 | mA |
| | $-I_{CMX}$ | – | $I_{RX}$ | – | mA |
| **Outputs Q1 and Q2** (pins 10 and 6) | | | | | |
| Output voltage at $V_{CC}$ = 4,8 V; $I_{QB}$ = 50 mA; $I_Q$ = 500 mA | $V_Q$ | – | 450 | 550 | mV |
| Output current at $V_{CC}$ = 4,8 V; $I_{QB}$ = 20 mA | $I_Q$ | – | – | 500 | mA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Outputs QB1 and QB2** (pins 9 and 5) | | | | | |
| Output voltage at $V_{CC}$ = 4,8 V; $I_{QB}$ = 50 mA | $V_{QB}$ | – | 1,2 | 1,9 | V |
| Output current at $V_{CC}$ = 4,8 V | $I_{QB}$ | – | – | 50 | mA |
| **Discharging pin DIS** (pin 3) | | | | | |
| Output voltage LOW at $I_{DIS}$ = 2 mA | $V_{DISL}$ | – | – | 300 | mV |
| Output current | | | | | |
| HIGH at $V_{DIS}$ = 9 V | $I_{DISH}$ | – | – | 500 | nA |
| LOW | $I_{DISL}$ | – | – | 5 | mA |

## APPLICATION INFORMATION

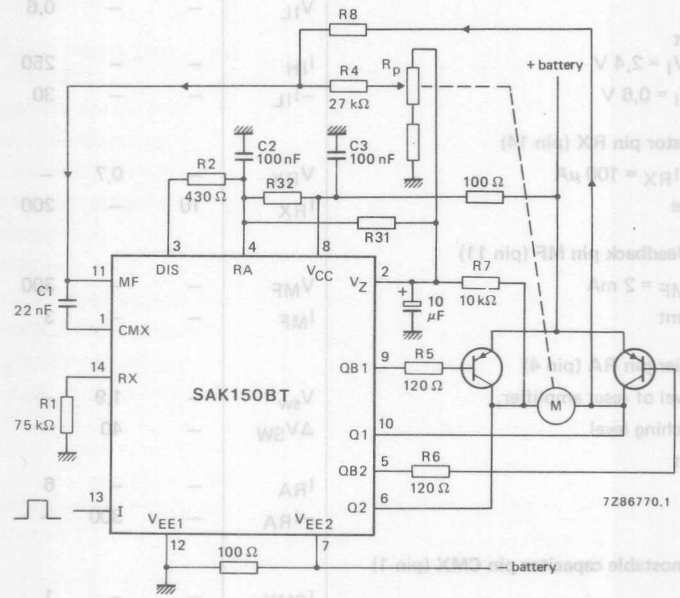



Fig. 5 Typical application of the SAK150BT for remote control of a model. The arrangement may be the last part at the receiving side, e.g. after a multi-channel time division multiplex system, to drive the steering motor. The potentiometer $R_p$ is actuated by the motor.

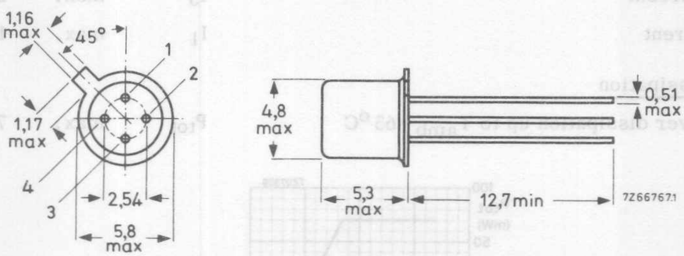
# LOW-LEVEL AMPLIFIER

The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

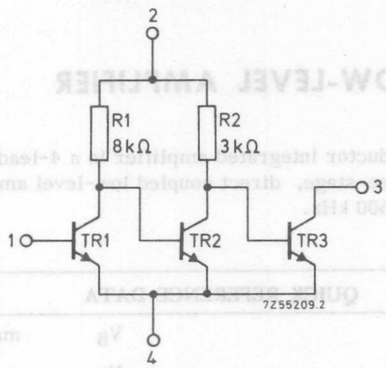
| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| Supply voltage | $V_B$ | max. | 8 | V |
| Output voltage | $V_{3-4}$ | max. | 7 | V |
| Output current | $I_3$ | max. | 25 | mA |
| Transducer gain at $P_o$ = 10 mW | | | | |
| $R_L$ = 150 Ω; f = 1 kHz | $G_{tr}$ | typ. | 77 | dB |
| Operating ambient temperature | $T_{amb}$ | | −20 to +100 | °C |

**PACKAGE OUTLINE** Dimensions in mm

TO-72 (SOT-18/17)



CIRCUIT DIAGRAM




**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

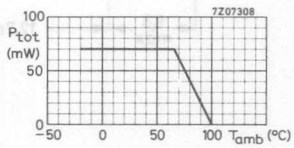
| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_B$ | max. | 8 | V |
| Output voltage | $V_{3-4}$ | max. | 7 | V |
| Input voltage | $-V_{1-4}$ | max. | 5 | V |

Currents

| | | | | |
|---|---|---|---|---|
| Output current | $I_3$ | max. | 25 | mA |
| Input current | $I_1$ | max. | 10 | mA |

Power dissipation

| | | | | |
|---|---|---|---|---|
| Total power dissipation up to $T_{amb} = 65\,^{o}C$ | $P_{tot}$ | max. | 70 | mW |

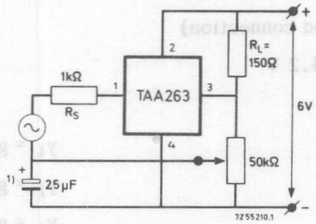



Temperatures

| | | | |
|---|---|---|---|
| Storage temperature | $T_{stg}$ | -55 to +125 | $^{o}C$ |
| Operating ambient temperature (see derating curve above) | $T_{amb}$ | -20 to +100 | $^{o}C$ |

**CHARACTERISTICS** $T_{amb} = 25\ ^oC$

Test circuit:




| | | | | |
|---|---|---|---|---|
| Currents | | | | |
| Output current | $I_3$ | typ. | 12 | mA |
| Total current drain (no signal) | $I_2+I_3$ | < | 16 | mA |
| Over-all small signal current gain | | | | |
| f = 1 kHz | $h_{f\ tot}$ | typ. | $5.10^5$ | |
| Transducer gain | | | | |
| f = 1 kHz; $P_o$ = 10 mW | $G_{tr}$ | > | 70 | dB |
| | | typ. | 77 | dB |
| Output power at f = 1 kHz; $d_{tot}$ = 10% | $P_o$ | > | 10 | mW |
| $d_{tot}$ = 5% | $P_o$ | > | 8 | mW |
| Noise figure | | | | |
| f = 400 Hz to 6 kHz | F | typ. | 5 | dB |
| | | < | 10 | dB |
| f = 450 kHz; $\Delta$f = 5 kHz | F | typ. | 2.7 | dB |

1) $Z \leqslant 10\ \Omega$ at f = 1 kHz

**CHARACTERISTICS** (continued) $T_{amb} = 25\ ^oC$

y parameters (point 4 common connection)

$V_B = 6$ V; $I_3 = 3$ mA; $V_{3-4} = 4.2$ V

| | | | | |
|---|---|---|---|---|
| f = 1 kHz | | | | |
| Input admittance | $y_i = g_i$ | typ. | 20 | $\mu\Omega^{-1}$ |
| Transfer admittance | $y_f = g_f$ | typ. | 11 | $\Omega^{-1}$ |
| Output admittance | $y_o = g_o$ | typ. | 60 | $\mu\Omega^{-1}$ |
| f = 450 kHz | | | | |
| Input conductance | $g_i$ | typ. | 15 | $\mu\Omega^{-1}$ |
| Input capacitance | $C_i$ | typ. | 14 | pF |
| Transfer admittance | $\lvert y_f \rvert$ | typ. | 9.4 | $\Omega^{-1}$ |
| Phase angle of transfer admittance | $\varphi_f$ | typ. | $125^o$ | |
| Output conductance | $g_o$ | typ. | 20 | $\mu\Omega^{-1}$ |
| Output capacitance | $C_o$ | typ. | 13 | pF |

# INTEGRATED MOST AMPLIFIER

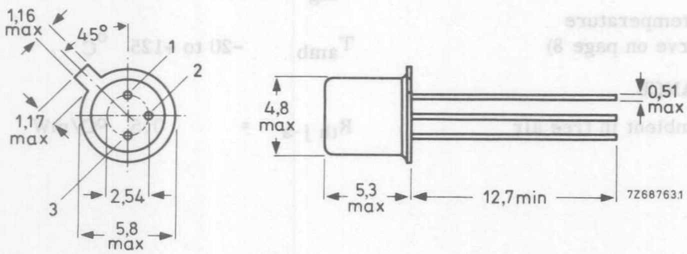
The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.
The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

**QUICK REFERENCE DATA**

| | | | | |
|---|---|---|---|---|
| Drain-source voltage ($V_{GS}$ = 0) | $-V_{DSS}$ | max. | 20 | V |
| Drain current | $-I_D$ | max. | 25 | mA |
| Gate-source voltage<br>$-I_D$ = 10 mA; $-V_{DS}$ = 10 V | $-V_{GS}$ | typ. | 11 | V |
| Gate-source resistance<br>$-V_{GS}$ up to 20 V; $T_j$ up to 125 °C | $r_{GS}$ | > | 100 | GΩ |
| Transfer admittance at f = 1 kHz<br>$-I_D$ = 10 mA; $-V_{DS}$ = 10 V | $\|y_{fs}\|$ | typ. | 75 | $m\Omega^{-1}$ |

**PACKAGE OUTLINE** Dimensions in mm

TO-18 (SOT-18/13)

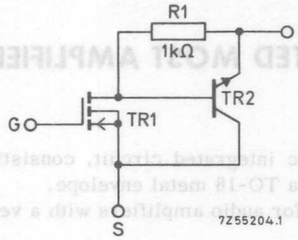



1 = drain
2 = gate
3 = source

Source connected to the case

Accessories supplied on request: 56246, 56263

CIRCUIT DIAGRAM




**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

| | | | | |
|---|---|---|---|---|
| Drain-source voltage ($V_{GS}$ = 0) | $-V_{DSS}$ | max. | 20 | V |
| Gate-source voltage ($I_D$ = 0) | $-V_{GSO}$ | max. | 20 | V |
| Non repetitive peak gate-source voltage (t ≤ 10 ms) | $-V_{GSM}$ | max. | 100 | V |

Current

| | | | | |
|---|---|---|---|---|
| Drain current | $-I_D$ | max. | 25 | mA |

Power dissipation

| | | | | |
|---|---|---|---|---|
| Total power dissipation up to $T_{amb}$ = 25 °C | $P_{tot}$ | max. | 200 | mW |

Temperatures

| | | | |
|---|---|---|---|
| Storage temperature | $T_{stg}$ | -55 to +125 | °C |
| Operating ambient temperature (see derating curve on page 8) | $T_{amb}$ | -20 to +125 | °C |

**THERMAL RESISTANCE**

| | | | | |
|---|---|---|---|---|
| From junction to ambient in free air | $R_{th\ j\text{-}a}$ | = | 0.5 | °C/mW |

**CHARACTERISTICS** $T_j = 25\ ^oC$ unless otherwise specified

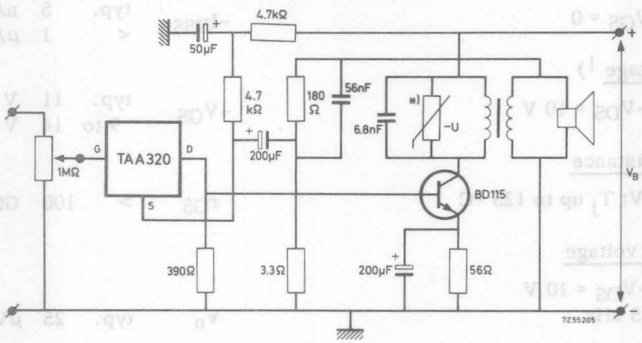
| | | | | |
|---|---|---|---|---|
| Drain current | | | | |
| $-V_{DS} = 20$ V; $V_{GS} = 0$ | $-I_{DSS}$ | typ. | 5 | nA |
| | | < | 1 | $\mu$A |
| Gate-source voltage [1]) | | | | |
| $-I_D = 10$ mA; $-V_{DS} = 10$ V | $-V_{GS}$ | typ. | 11 | V |
| | | 9 to | 14 | V |
| Gate-source resistance | | | | |
| $-V_{GS}$ up to 20 V; $T_j$ up to 125 $^oC$ | $r_{GS}$ | > | 100 | G$\Omega$ |
| Equivalent noise voltage | | | | |
| $-I_D = 10$ mA; $-V_{DS} = 10$ V<br>B = 50 Hz to 15 kHz | $v_n$ | typ. | 25 | $\mu$V |
| y parameters at f = 1 kHz | | | | |
| $-I_D = 10$ mA; $-V_{DS} = 10$ V | | | | |
| Transfer admittance | $\lvert y_{fs} \rvert$ | typ. | 75 | m$\Omega^{-1}$ |
| | | 40 to | 120 | m$\Omega^{-1}$ |
| Input capacitance | $C_{is}$ | typ. | 8 | pF |
| Feedback capacitance | $-C_{rs}$ | typ. | 1.5 | pF |
| Output conductance | $g_{os}$ | typ. | 0.65 | m$\Omega^{-1}$ |

**NOTE**

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/$^oC$ with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115




* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_B$ | = | 100 | V |
| Collector current of BD115 | $I_C$ | typ. | 50 | mA |
| Drain current of TAA320 | $-I_D$ | typ. | 9.5 | mA |
| Primary d.c. resistance of output transformer | | | 140 | Ω |
| Primary inductance of output transformer | | | 2.7 | H |
| A.C. collector load for BD115 | | | 1.8 | kΩ |

Performance at f = 1 kHz; feedback = 16 dB

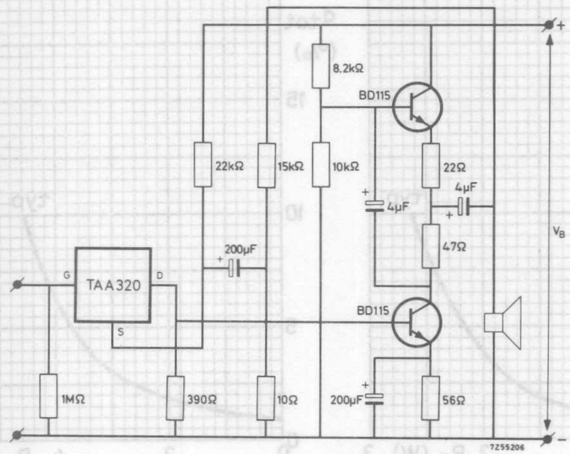
| | | | | |
|---|---|---|---|---|
| Output power at $d_{tot}$ = 10% (on primary of the output transformer) | $P_o$ | typ. | 2.6 | W |
| Input voltage for $P_o$ = 50 mW | $V_{i(rms)}$ | typ. | 13.5 | mV |
| Input voltage for $P_o$ = 2 W | $V_{i(rms)}$ | typ. | 86 | mV |
| Total distortion at $P_o$ = 2 W | $d_{tot}$ | typ. | 3.6 | % |
| Minimum frequency response (-3 dB) | | | 60 Hz to 20 | kHz |
| Signal-noise ratio at $P_o$ = 2 W | | typ. | 73 | dB |

Mounting instruction for BD115

Proper continuous operation is ensured up to $T_{amb}$ = 50 °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 $cm^2$ with a clamping washer of type 56218.
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 $cm^2$.
Recommended diameter of hole in heatsink: 7.7 mm.

**APPLICATION INFORMATION** (continued)

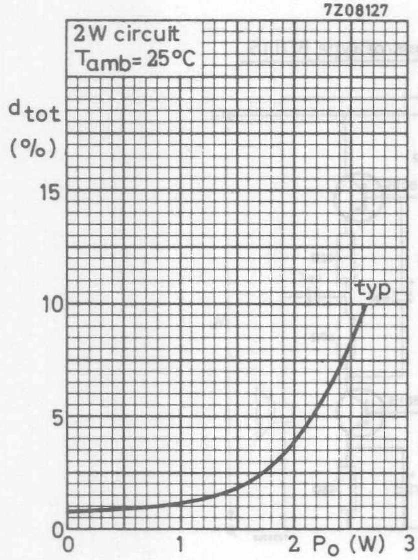
4 W audio amplifier with TAA320 and 2 transistors of type BD115.

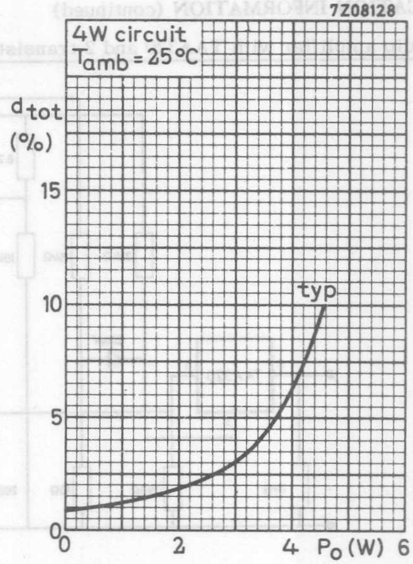


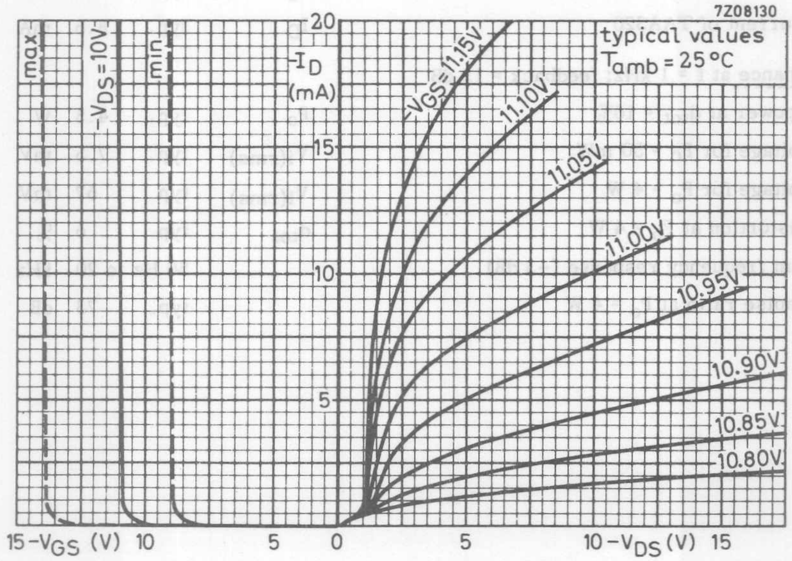

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_B$ | = | 200 | V |
| Collector current of a BD115 | $I_C$ | typ. | 52 | mA |
| Drain current of TAA320 | $-I_D$ | typ. | 8.6 | mA |

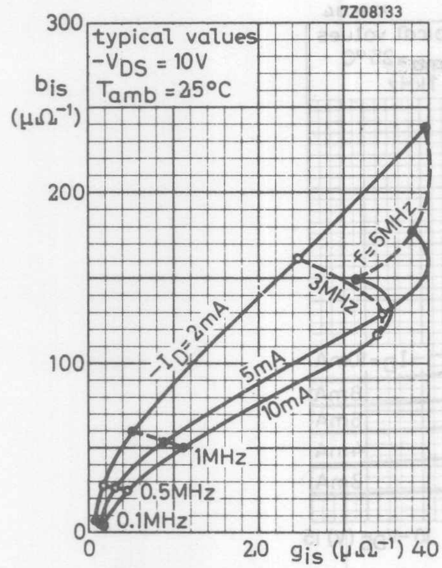
Performance at f = 1 kHz; feedback = 12 dB

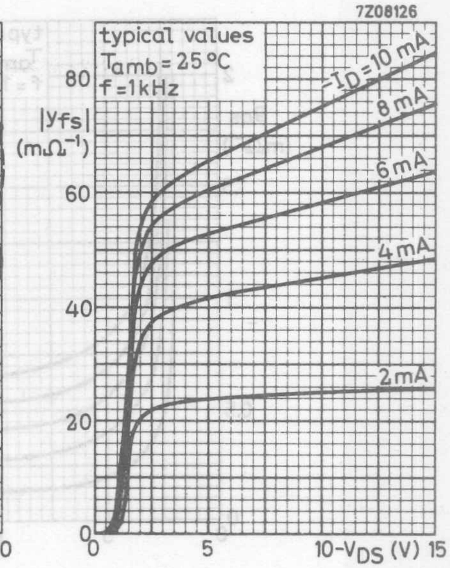
| | | | | |
|---|---|---|---|---|
| Output power at $d_{tot}$ = 10% | $P_o$ | typ. | 4.5 | W |
| Input voltage for $P_o$ = 50 mW | $V_{i(rms)}$ | typ. | 7.5 | mV |
| Input voltage for $P_o$ = 4 W | $V_{i(rms)}$ | typ. | 67 | mV |
| Total distortion at $P_o$ = 4 W | $d_{tot}$ | typ. | 6 | % |
| Minimum frequency response (-3 dB) | | 50 Hz to 20 | | kHz |
| Signal-noise ratio at $P_o$ = 4 W | | typ. | 73 | dB |

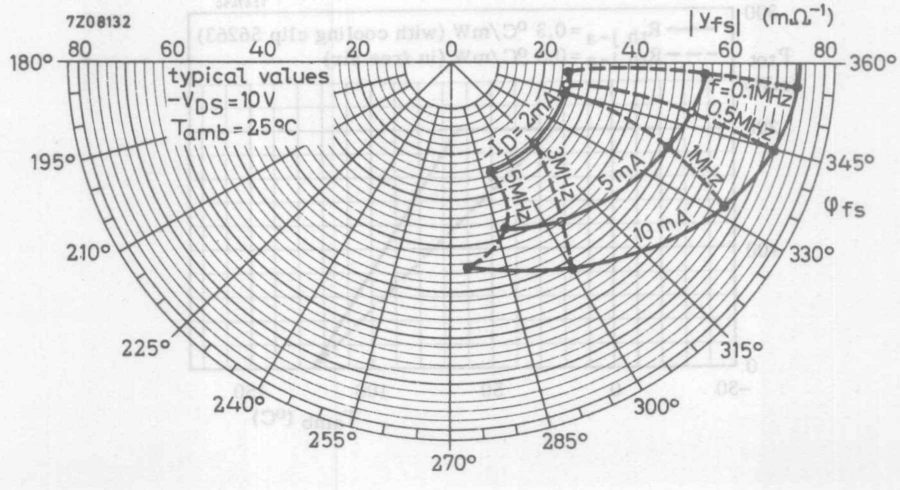

7Z08127
2W circuit
Tamb = 25 °C
dtot (%)
typ
Po (W)

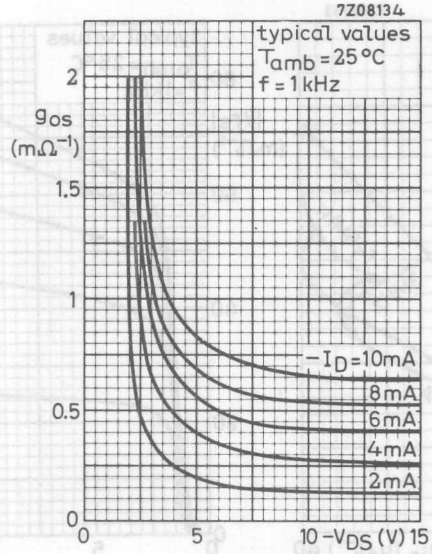

7Z08128
4W circuit
Tamb = 25 °C
dtot (%)
typ
Po (W)


7Z08130
typical values
Tamb = 25 °C
max
−VDS = 10V
min
−ID (mA)
−VGS = 11.15V
11.10V
11.05V
11.00V
10.95V
10.90V
10.85V
10.80V
−VGS (V)
−VDS (V)

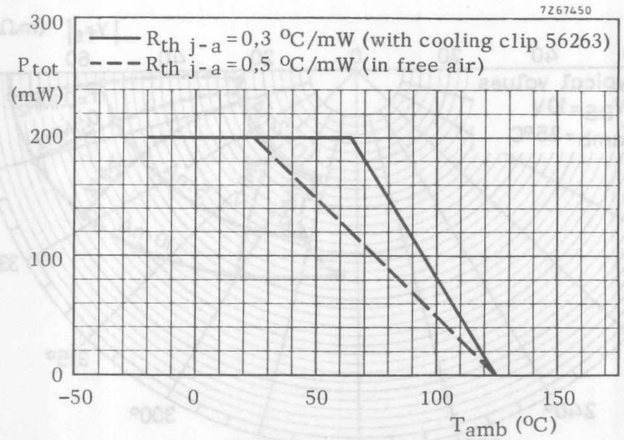

7Z08133
typical values
$-V_{DS}$ = 10V
$T_{amb}$ = 25°C
$b_{is}$ ($\mu\Omega^{-1}$)
$g_{is}$ ($\mu\Omega^{-1}$)
$-I_D$ = 2mA
5mA
10mA
f = 5MHz
3MHz
1MHz
0.5MHz
0.1MHz


7Z08126
typical values
$T_{amb}$ = 25 °C
f = 1kHz
$|y_{fs}|$ ($m\Omega^{-1}$)
$-V_{DS}$ (V)
$-I_D$ = 10 mA
8 mA
6 mA
4 mA
2 mA

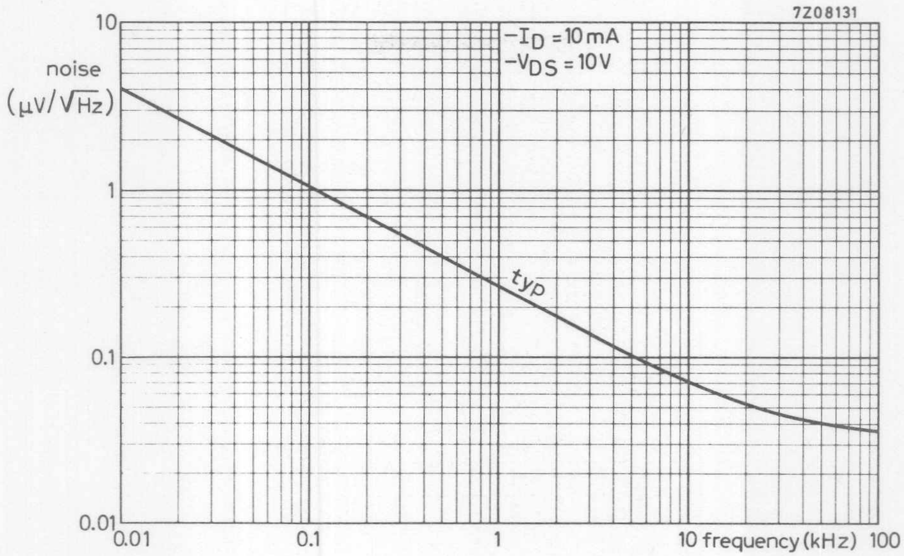

7Z08132
$|y_{fs}|$ ($m\Omega^{-1}$)
typical values
$-V_{DS}$ = 10V
$T_{amb}$ = 25°C
$\varphi_{fs}$
f = 0.1MHz
0.5MHz
1MHz
3MHz
5MHz
$-I_D$ = 2mA
5 mA
10 mA



7Z08134
typical values
$T_{amb}$ = 25 °C
f = 1 kHz
$g_{os}$
($m\Omega^{-1}$)
2
1.5
1
0.5
0
$-I_D$ = 10mA
8mA
6mA
4mA
2mA
0
5
10
15
$-V_{DS}$ (V)

7Z67450
$R_{th\ j-a}$ = 0,3 °C/mW (with cooling clip 56263)
$R_{th\ j-a}$ = 0,5 °C/mW (in free air)
$P_{tot}$
(mW)
300
200
100
0
−50
0
50
100
150
$T_{amb}$ (°C)


7Z08131
noise
(μV/√Hz)
10
1
0.1
0.01
−I_D = 10 mA
−V_DS = 10 V
typ
0.01
0.1
1
10 frequency (kHz) 100

# INTEGRATED MOST LEVEL SENSOR

The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

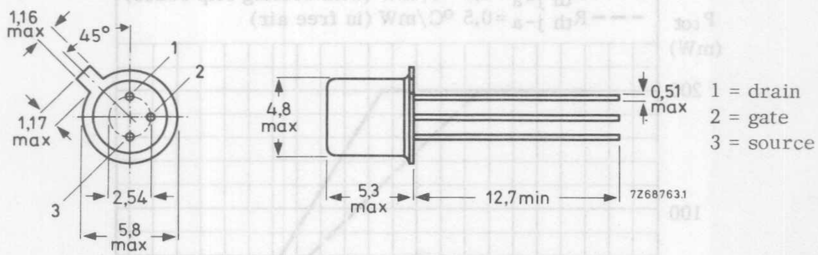
**QUICK REFERENCE DATA**

| | | | | | |
|---|---|---|---|---|---|
| Drain-source voltage ($V_{GS}$ = 0) | | $-V_{DSS}$ | max. | 20 | V |
| Drain current | | $-I_D$ | max. | 60 | mA |
| Gate-source voltage [1] | | | | | |
| $-I_D$ = 10 mA; $-V_{DS}$ = 10 V | group 1: | $-V_{GS}$ | typ. | 10,6 | V |
| | | | 10,0 to | 11,2 | V |
| | group 2: | $-V_{GS}$ | typ. | 11,3 | V |
| | | | 10,7 to | 11,9 | V |
| | group 3: | $-V_{GS}$ | typ. | 12,0 | V |
| | | | 11,4 to | 12,6 | V |
| | group 4: | $-V_{GS}$ | typ. | 12,7 | V |
| | | | 12,1 to | 13,3 | V |
| Gate cut-off current at $T_{amb}$ = 25 °C | | | | | |
| $-V_{GS}$ = 20 V; $I_D$ = 0 | | $-I_{GSO}$ | typ. | 1 | pA |
| $-V_{GS}$ = 20 V; $V_{DS}$ = 0 | | $-I_{GSS}$ | typ. | 1 | pA |

**PACKAGE OUTLINE**

Dimensions in mm

TO-18 (SOT-18/13)

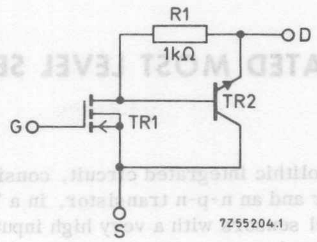



source connected to the case

Accessories supplied on request: 56246; 56263

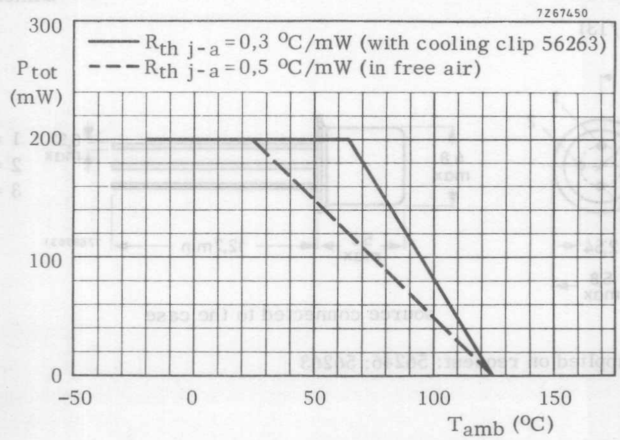
1) For explanation of the group codification see b under 'Notes'.

**CIRCUIT DIAGRAM**




**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Voltages | | | | |
| Drain-source voltage ($V_{GS}$ = 0) | $-V_{DSS}$ | max. | 20 | V |
| Gate-source voltage ($I_D$ = 0) | $-V_{GSO}$ | max. | 20 | V |
| Non-repetitive peak gate-source voltage (t ≤10 ms) | $\pm V_{GSM}$ | max. | 100 | V |
| Current | | | | |
| Drain current | $-I_D$ | max. | 60 | mA |
| Peak drain current (t < 200 ms; δ 0,001) | $-I_{DM}$ | max. | 100 | mA |
| Temperatures | | | | |
| Storage temperature | $T_{stg}$ | | -65 to +125 | $^oC$ |
| Operating ambient temperature (see curve below) | $T_{amb}$ | | -20 to +125 | $^oC$ |



**CHARACTERISTICS** $T_j = 25\ ^{o}C$ unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Drain current | | | | |
| $-V_{DS} = 20$ V; $V_{GS} = 0$ | $-I_{DSS}$ | typ. | 5 | nA |
| | | < | 1 | μA |
| Drain-source voltage [1] | | | | |
| $-I_D = 10$ mA; $-V_{GS} = 20$ V | $-V_{DS}$ | < | 1 | V |
| $-I_D = 60$ mA; $-V_{GS} = 20$ V | $-V_{DS}$ | < | 1,5 | V |
| Gate-source voltage (see note b) | | | | |
| $-I_D = 10$ mA; $-V_{DS} = 10$ V group 1: | $-V_{GS}$ | typ. | 10,6 | V |
| | | | 10,0 to 11,2 | V |
| group 2: | $-V_{GS}$ | typ. | 11,3 | V |
| | | | 10,7 to 11,9 | V |
| group 3: | $-V_{GS}$ | typ. | 12,0 | V |
| | | | 11,4 to 12,6 | V |
| group 4: | $-V_{GS}$ | typ. | 12,7 | V |
| | | | 12,1 to 13,3 | V |
| Gate cut-off current | | | | |
| $-V_{GS} = 20$ V; $I_D = 0$ | $-I_{GSO}$ | typ. | 1 | pA [2] |
| $-V_{GS} = 20$ V; $V_{DS} = 0$ | $-I_{GSS}$ | typ. | 1 | pA [2] |

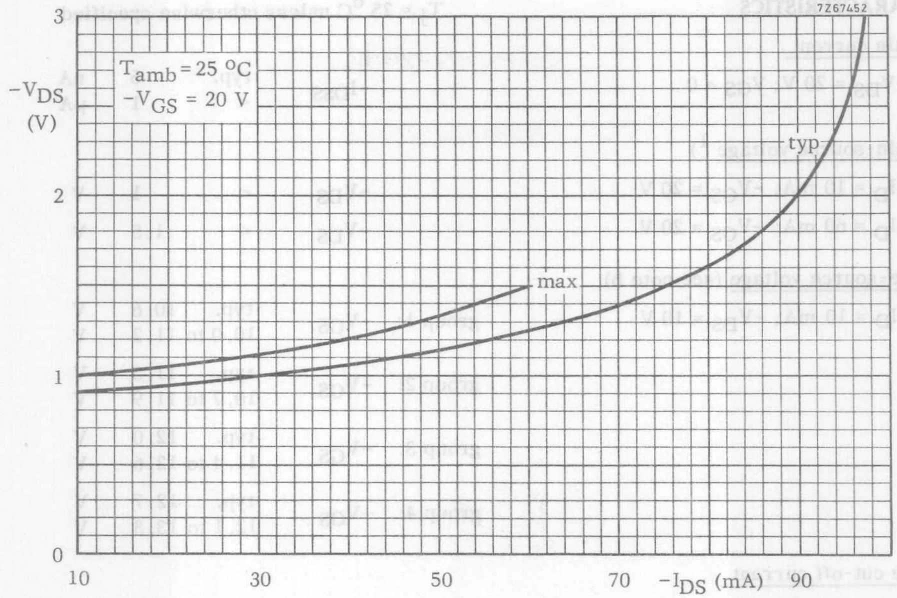
**NOTES**

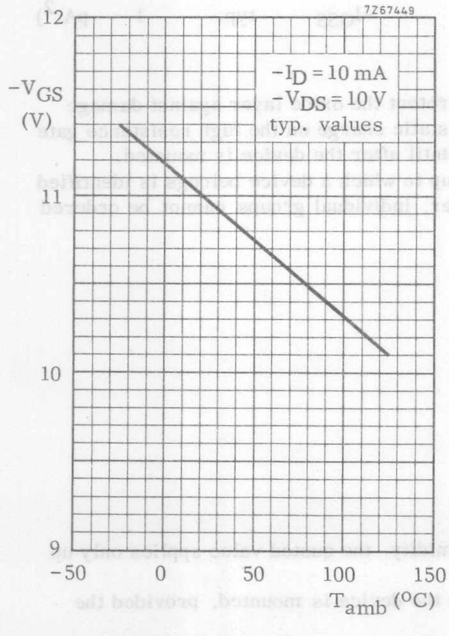
a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.

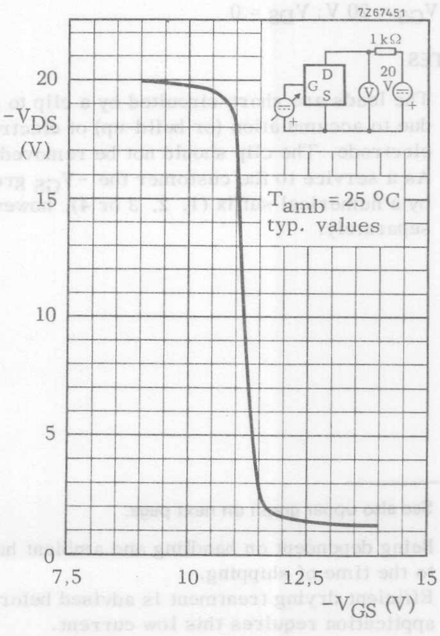
b. As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

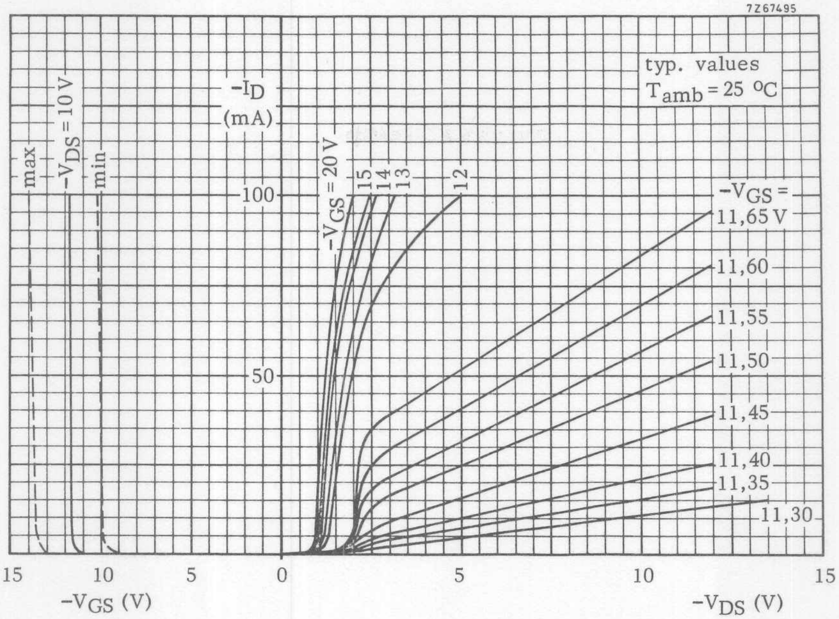
---

1. See also upper graph on next page.
2. Being dependent on handling and ambient humidity. the quoted value applies only up to the time of shipping.
Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.


7Z67452
$T_{amb} = 25\ ^oC$
$-V_{GS} = 20$ V
$-V_{DS}$ (V)
3
2
1
0
typ
max
10
30
50
70
90
$-I_{DS}$ (mA)


7Z67449
$-I_D = 10$ mA
$-V_{DS} = 10$ V
typ. values
$-V_{GS}$ (V)
12
11
10
9
−50
0
50
100
150
$T_{amb}$ (°C)


7Z67451
1 kΩ
G
D
S
20 V
$-V_{DS}$ (V)
20
15
10
5
0
$T_{amb} = 25\ ^oC$
typ. values
7,5
10
12,5
15
$-V_{GS}$ (V)


7Z67495
typ. values
$T_{amb}$ = 25 °C
$-I_D$ (mA)
100
50
max
$-V_{DS}$ = 10 V
min
$-V_{GS}$ = 20 V
15
14
13
12
$-V_{GS}$ =
11,65 V
11,60
11,55
11,50
11,45
11,40
11,35
11,30
15
10
5
0
5
10
15
$-V_{GS}$ (V)
$-V_{DS}$ (V)

# HI-FI F.M./I.F. AMPLIFIER

The TCA420A is a monolithic integrated f.m./i.f. amplifier for car and hi-fi equipment provided with the following functions:

- limiter amplifier
- symmetrical quadrature detector
- symmetrical a.f.c. output
- field-strength indication output
- stereo decoder switching voltage
- adjustable side response suppression
- muting

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_P$ | typ. | 15 | V |
| Supply current (pin 11) | $I_P$ | typ. | 26 | mA |
| Input limiting voltage (−3 dB); $f_o$ = 10,7 MHz | $V_{i\,lim}$ | typ. | 20 | $\mu$V |
| A.F. output voltage (pin 5); $\Delta f = \pm 15$ kHz; r.m.s. value | $V_{o(rms)}$ | typ. | 115 | mV |
| Signal plus noise-to-noise ratio; $V_i > 1$ mV; $\Delta f = \pm 15$ kHz | S+N/N | typ. | 72 | dB |
| I.F. input voltage; $\Delta f = \pm 15$ kHz | | | | |
| S + N/N = 26 dB | $V_i$ | typ. | 15 | $\mu$V |
| S + N/N = 46 dB | $V_i$ | typ. | 45 | $\mu$V |
| A.M. rejection; $V_i$ = 10 mV; $f_m$ = 1 kHz (f.m.); $\Delta f = \pm 15$ kHz | $\alpha$ | typ. | 50 | dB |
| Total distortion (single tuned circuit); $\Delta f = \pm 15$ kHz | $d_{tot}$ | typ. | 0,1 | % |
| Centre shift of f.m. detector curve | $\Delta f = \lvert f_{o1} - f_{o2} \rvert$ | typ. | 7 | kHz |
| Field-strength indication range | $\Delta V_i$ | typ. | 70 | dB |
| Supply voltage range (pin 11) | $V_P$ | | 6 to 18 | V |
| Ambient temperature range | $T_{amb}$ | | −30 to +80 | °C |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

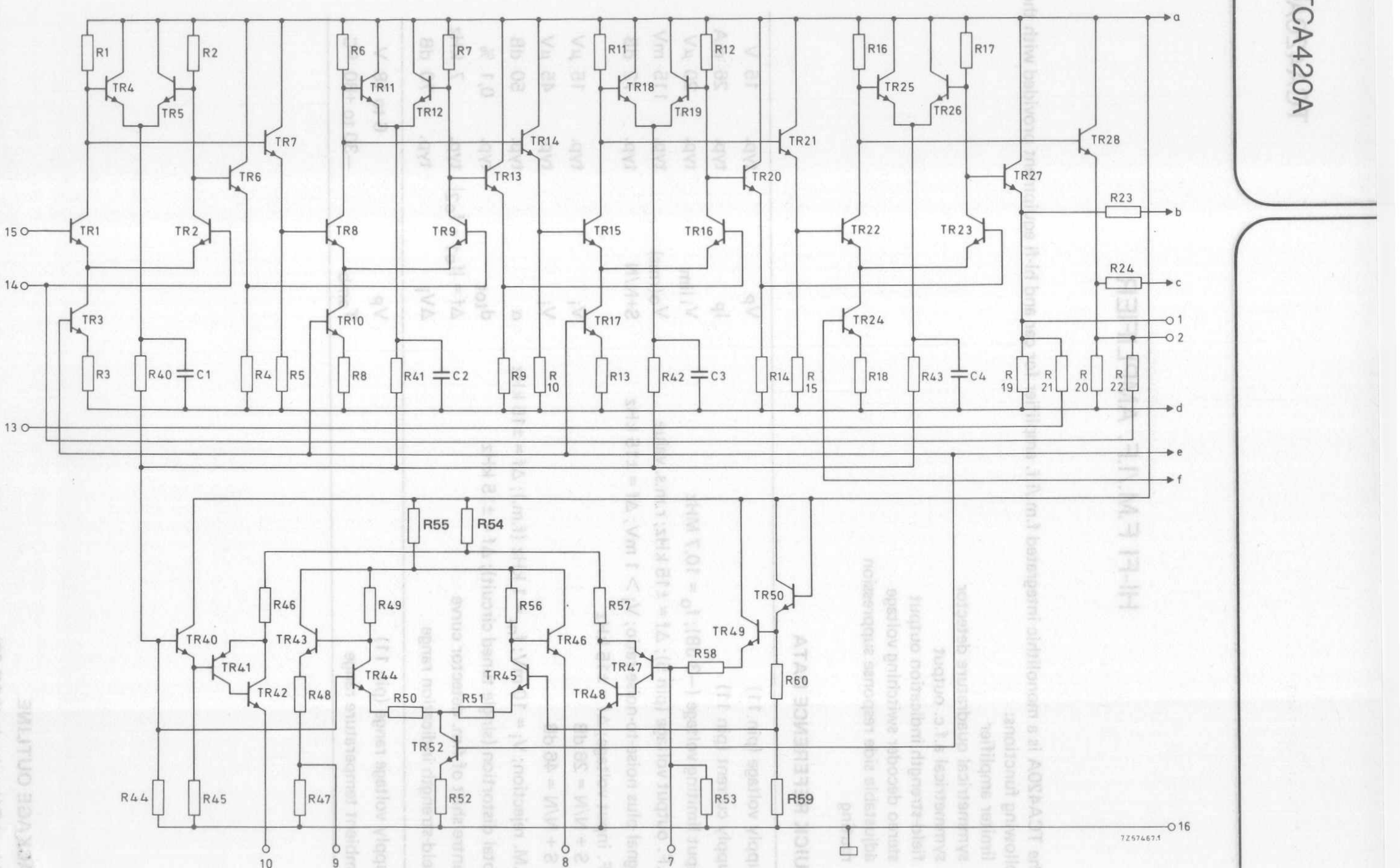



Fig. 1a Part of circuit diagram; other part continued in Fig. 1b.

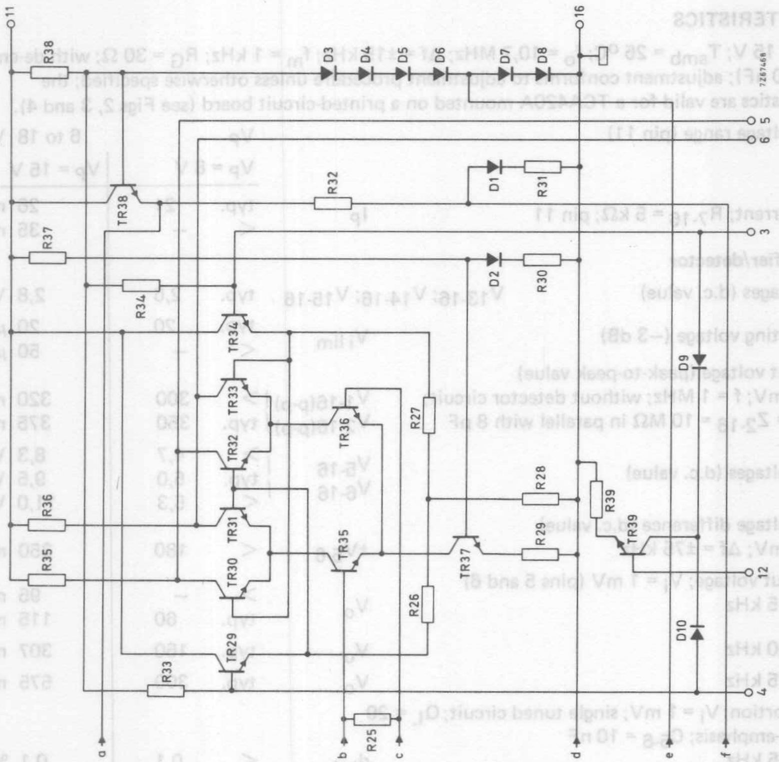



Fig. 1b Part of circuit diagram; continued from Fig. 1a.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_P = V_{11\text{-}16}$ | max. | 18 | V |
| Total power dissipation | $P_{tot}$ | max. | 720 | mW |
| Storage temperature | $T_{stg}$ | | −55 to +150 | °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to +80 | °C |

## CHARACTERISTICS

$V_P$ = 8 or 15 V; $T_{amb}$ = 25 °C; $f_o$ = 10,7 MHz; $\Delta f$ = ±15 kHz; $f_m$ = 1 kHz; $R_G$ = 30 Ω; with de-emphasis ($C_{5\text{-}6}$ = 10 nF); adjustment conforms to adjustment procedure unless otherwise specified; the characteristics are valid for a TCA420A mounted on a printed-circuit board (see Figs 2, 3 and 4).

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range (pin 11) | $V_P$ | | | 6 to 18 | V |
| | | | $V_P$ = 8 V | $V_P$ = 15 V | |
| Supply current; $R_{7\text{-}16}$ = 5 kΩ; pin 11 | $I_P$ | typ. | 21 | 26 | mA |
| | | < | – | 35 | mA |
| **I.F. amplifier/detector** | | | | | |
| Input voltages (d.c. value) | $V_{13\text{-}16}$; $V_{14\text{-}16}$; $V_{15\text{-}16}$ | typ. | 2,6 | 2,8 | V |
| Input limiting voltage (−3 dB) | $V_{i\,lim}$ | typ. | 20 | 20 | μV |
| | | < | – | 50 | μV |
| I.F. output voltage (peak-to-peak value) | | | | | |
| $V_i$ = 5 mV; f = 1 MHz; without detector circuit; | $V_{1\text{-}16(p\text{-}p)}$ | > | 300 | 320 | mV |
| $Z_{1\text{-}16} = Z_{2\text{-}16}$ = 10 MΩ in parallel with 8 pF | $V_{2\text{-}16(p\text{-}p)}$ | typ. | 350 | 375 | mV |
| Output voltages (d.c. value) | $V_{5\text{-}16}$, $V_{6\text{-}16}$ | > | 4,7 | 8,3 | V |
| | | typ. | 5,0 | 9,5 | V |
| | | < | 5,3 | 11,0 | V |
| Output voltage difference (d.c. value) | | | | | |
| $V_i$ = 1 mV; $\Delta f$ = ±75 kHz | $\pm V_{5\text{-}6}$ | < | 180 | 350 | mV |
| A.F. output voltage; $V_i$ = 1 mV (pins 5 and 6) | | | | | |
| $\Delta f$ = ±15 kHz | $V_o$ | > | – | 95 | mV |
| | | typ. | 60 | 115 | mV |
| $\Delta f$ = ±40 kHz | $V_o$ | typ. | 160 | 307 | mV |
| $\Delta f$ = ±75 kHz | $V_o$ | typ. | 300 | 575 | mV |
| Total distortion; $V_i$ = 1 mV; single tuned circuit; $Q_L$ = 20 | | | | | |
| with de-emphasis; $C_{5\text{-}6}$ = 10 nF | | | | | |
| $\Delta f$ = ±15 kHz | $d_{tot}$ | < | 0,1 | 0,1 | % |
| $\Delta f$ = ±40 kHz | $d_{tot}$ | typ. | 0,18 | 0,18 | % |
| $\Delta f$ = ±75 kHz | $d_{tot}$ | typ. | 0,45 | 0,45 | % |
| without de-emphasis; $C_{5\text{-}6}$ = 220 pF | | | | | |
| $\Delta f$ = ±15 kHz | $d_{tot}$ | < | 0,1 | 0,1 | % |
| $\Delta f$ = ±40 kHz | $d_{tot}$ | typ. | 0,22 | 0,22 | % |
| $\Delta f$ = ±75 kHz | $d_{tot}$ | typ. | 0,65 | 0,65 | % |
| | | < | 1 | 1 | % |

| | | | $V_P = 8$ V | $V_P = 15$ V | |
|---|---|---|---|---|---|
| I.F. input voltage; with filter: B = 250 Hz to 16 kHz | | | | | |
| S+N/N = 26 dB; with de-emphasis; $C_{5\text{-}6}$ = 10 nF | | | | | |
| Δf = ±15 kHz | $V_i$ | typ. | 15 | 15 | μV |
| Δf = ±75 kHz | $V_i$ | typ. | 5 | 5 | μV |
| S+N/N = 26 dB; without de-emphasis; $C_{5\text{-}6}$ = 220 pF | | | | | |
| Δf = ±15 kHz | $V_i$ | typ. | 20 | 20 | μV |
| Δf = ±75 kHz | $V_i$ | typ. | 8 | 8 | μV |
| S+N/N = 46 dB; with de-emphasis; $C_{5\text{-}6}$ = 10 nF | | | | | |
| Δf = ±15 kHz | $V_i$ | typ. | 45 | 45 | μV |
| Δf = ±75 kHz | $V_i$ | typ. | 20 | 20 | μV |
| S+N/N = 46 dB; without de-emphasis; $C_{5\text{-}6}$ = 220 pF | | | | | |
| Δf = ±15 kHz | $V_i$ | typ. | 65 | 65 | μV |
| Δf = ±75 kHz | $V_i$ | typ. | 30 | 30 | μV |
| Signal plus noise-to-noise ratio; with filter: | | | | | |
| B = 250 Hz to 16 kHz; $V_i$ = 1 mV | | | | | |
| with de-emphasis | | | | | |
| Δf = ±15 kHz | S+N/N | typ. | 74 | 76 | dB |
| Δf = ±75 kHz | S+N/N | typ. | 88 | 90 | dB |
| without de-emphasis | | | | | |
| Δf = ±15 kHz | S+N/N | typ. | 68 | 70 | dB |
| Δf = ±75 kHz | S+N/N | typ. | 82 | 84 | dB |
| Noise output voltage; weighted conform DIN45405 | | | | | |
| with de-emphasis | | | | | |
| $V_i$ = 0 | $V_{no}$ | typ. | 7 | 12 | mV |
| $V_i$ = 1 mV | $V_{no}$ | typ. | 30 | 50 | μV |
| A.M. rejection; with filter: B = 700 Hz to 5 kHz | | | | | |
| $f_m$ = 70 Hz; Δf = ±15 kHz (for f.m.); | | | | | |
| $f_m$ = 1 kHz; m = 0,3 (for a.m.); simultaneously modulated | | | | | |
| $V_i$ = 0,3 mV | α | typ. | 52 | 52 | dB |
| $V_i$ = 1 mV | α | typ. | 40 | 40 | dB |
| $V_i$ = 10 mV | α | typ. | 52 | 52 | dB |
| $V_i$ = 100 mV | α | typ. | 43 | 43 | dB |
| Zero crossing shift of f.m. detector curve (see note) | | | | | |
| $f_m$ = 70 Hz; Δf = ±75 kHz (for f.m.); | | typ. | 4 | 7 | kHz |
| $f_m$ = 1 kHz; m = 85% (for a.m.) | $\Delta f = \lvert f_{o1} - f_{o2} \rvert$ | < | 9 | 15 | kHz |
| Detector input impedance | $Z_{3\text{-}4}$ | | 4,4 kΩ//2,25 pF | | |
| Output resistance | $R_{5\text{-}11}; R_{6\text{-}11}$ | typ. | 3,3 | 3,3 | kΩ |

**Note**

Zero crossing shift is defined as the difference between frequencies $f_{o1}$ at $V_i$ = 1 mV and $f_{o2}$ at $V_i$ = 30 μV.

## CHARACTERISTICS (continued)

| Parameter | Symbol | | Vp = 8 V | Vp = 15 V |
|---|---|---|---|---|
| **Side response suppression** | | | | |
| Input voltage for 10 dB side response suppression at S1 = 'on' adjust R1, so $V_{10\text{-}16} = 1,3$ V at $V_i = 0$; S1 = 'off'; R4 = 3,9 kΩ | $V_{i(rms)}$ | typ. | 35 | 30 μV |
| Side response suppression level $\Delta f = \pm 15$ kHz; $V_{i(rms)} = 1$ mV | | | | |
| control voltage for $\Delta V_o = -1$ dB | $V_{12\text{-}16}$ | typ. | 0,7 | 0,7 V |
| control voltage for $\Delta V_o = -10$ dB | $V_{12\text{-}16}$ | typ. | 1,1 | 1,1 V |
| **Muting** | | | | |
| Output signal muting at S2 = 'on'; reference signal at S2 = 'off'; $V_{i(rms)} = 1$ mV; $\Delta f = \pm 75$ kHz; R4 = 3,9 kΩ | $\Delta V_o$ | typ. | −80 | −80 dB |
| **Field-strength indication** | | | | |
| Output voltages (d.c. value) $V_i = 0$; $I_{8\text{-}9} = 0$; $R_{8\text{-}16} = 4,3$ kΩ | $V_{9\text{-}16}$ | typ. | 1,75 | 1,85 V |
| | $V_{8\text{-}16}$ | typ. | 1,90 | 2,00 V |
| Field-strength indicator current $R_{indicator} = 2$ kΩ; adjust R2 so $I_{8\text{-}9} = 0$ at $V_i = 0$ and R3 = 0 measured at $V_{i(rms)} = 120$ mV | $I_{8\text{-}9}$ | > | 130 | 140 μA |
| | | typ. | 190 | 210 μA |
| Output resistance | $R_o$ | typ. | 810 | 850 Ω |
| | $R_{9\text{-}16}$ | typ. | 3,7 | 3,7 kΩ |
| **Stereo decoder switching voltage** | | | | |
| Reference voltage; without load: $I_7 = 0$ | $V_{7\text{-}16}$ | typ. | 2,05 | 2,25 V |
| Output voltage; $I_{10} = I_{10max}$ | $V_{10\text{-}16}$ | typ. | 1,70 | 1,90 V |
| Available output current | $-I_{10\,max}$ | typ. | 0,45 | 0,85 mA |
| Output voltage as a function of the i.f. input voltage $R_{10\text{-}16} = 3,9$ kΩ; R1 = 5 kΩ | $\dfrac{\Delta V_{10\text{-}16}}{20 \log \frac{V_{i1}}{V_{i2}}}$ | typ. | −0,9 | −1,2 V/20 dB |
| Input voltage for $V_{10\text{-}16} = 0,8$ V adjust R1 so $V_{10\text{-}16} = 1,3$ V at $V_{i(rms)} = 0$ | $V_{i(rms)}$ | typ. | 98 | 100 μV |
| | | < | 150 | 200 μV |
| Input voltage for $V_{10\text{-}16} = 1,3$ V adjust R1 so $V_{10\text{-}16} = 0,8$ V at $V_{i(rms)} = 3$ mV | $V_{i(rms)}$ | > | – | 0,5 mV |
| | | typ. | 1,3 | 1,3 mV |
| | | < | – | 1,75 mV |
| Input resistance (pin 7) | $R_{7\text{-}16}$ | typ. | 4 | 4,7 kΩ |

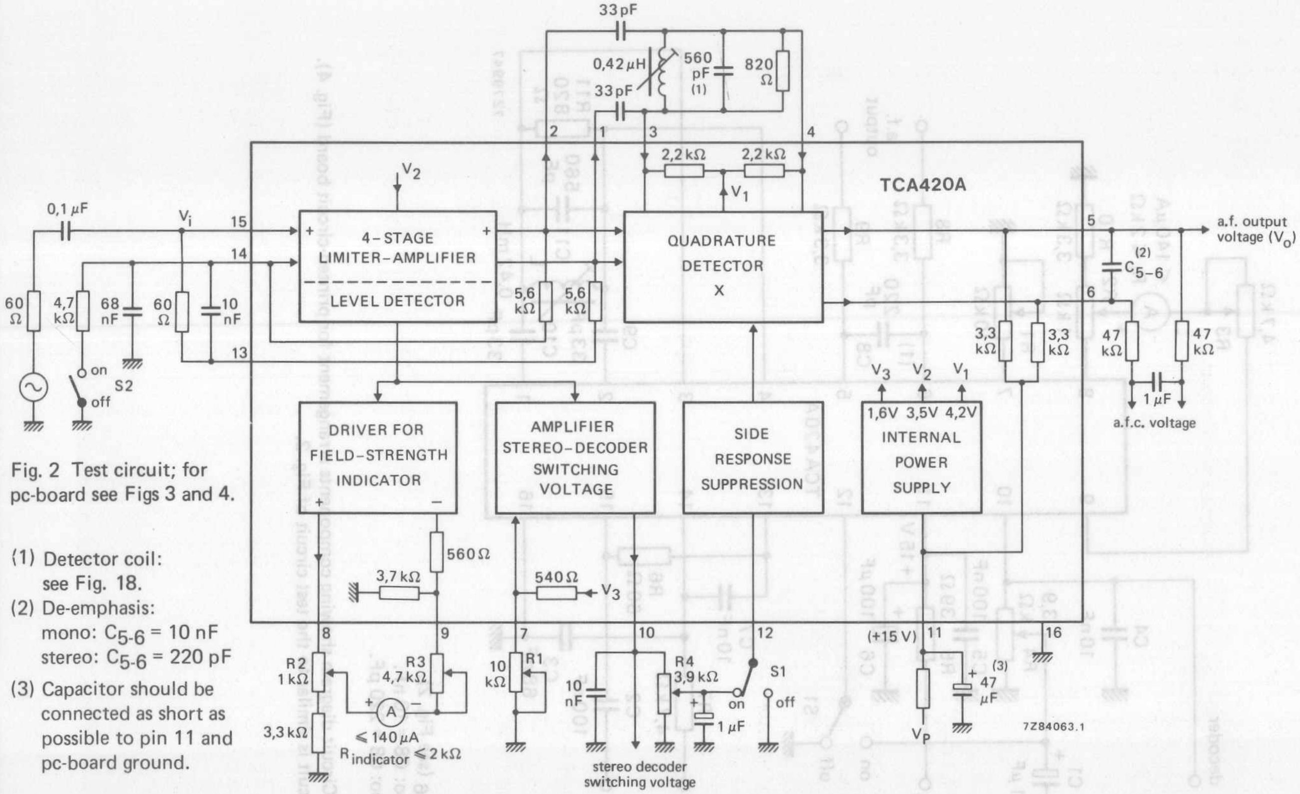
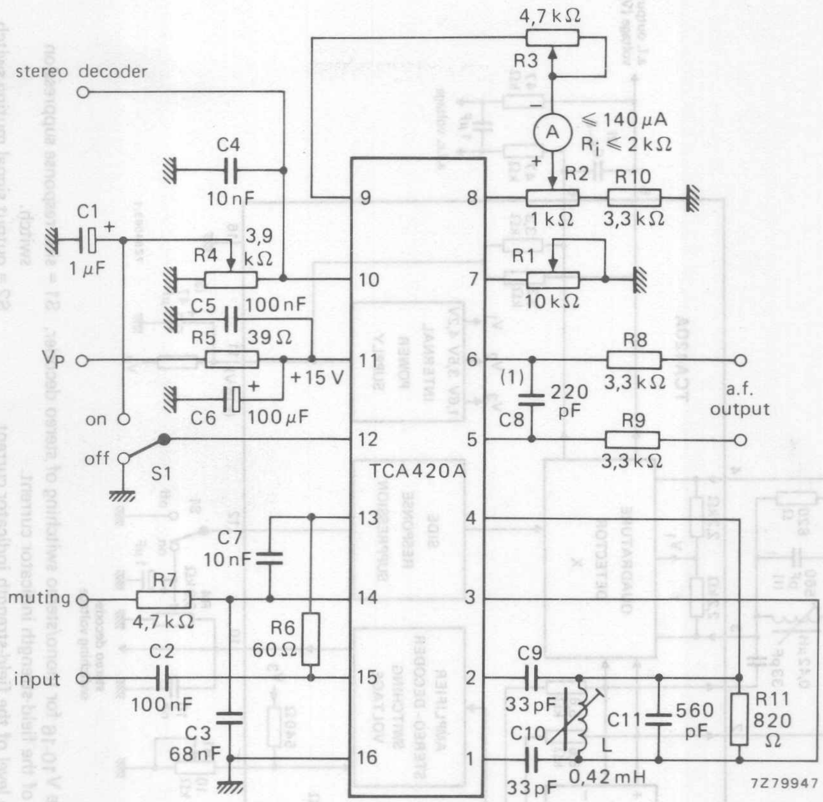



Fig. 2 Test circuit; for pc-board see Figs 3 and 4.

(1) Detector coil: see Fig. 18.
(2) De-emphasis:
mono: $C_{5\text{-}6}$ = 10 nF
stereo: $C_{5\text{-}6}$ = 220 pF
(3) Capacitor should be connected as short as possible to pin 11 and pc-board ground.

R1 = preset potentiometer for adjusting output voltage $V_{10\text{-}16}$ for mono/stereo switching of stereo decoder.
R2 = preset potentiometer for adjusting the zero level of the field-strength indicator current.
R3 = preset potentiometer for adjusting the maximum level of the field-strength indicator current.
R4 = preset potentiometer for adjusting the side response suppression.

S1 = side response suppression switch.
S2 = output signal muting switch.




(1) $C_8 = C_{5\text{-}6}$ (see Fig. 2).
For mono: C8 = 10 nF.
For stereo: C8 = 220 pF.

Fig. 3 Circuit diagram showing components arrangement for printed-circuit board (Fig. 4).
The circuit is similar to the test circuit of Fig. 2.

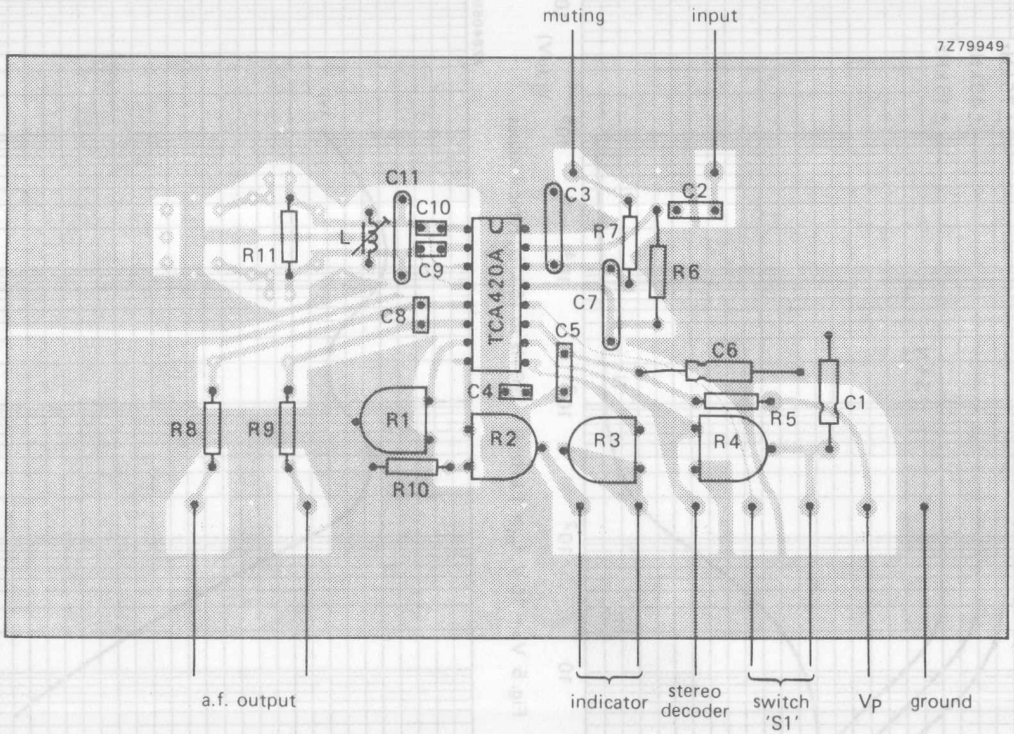



Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

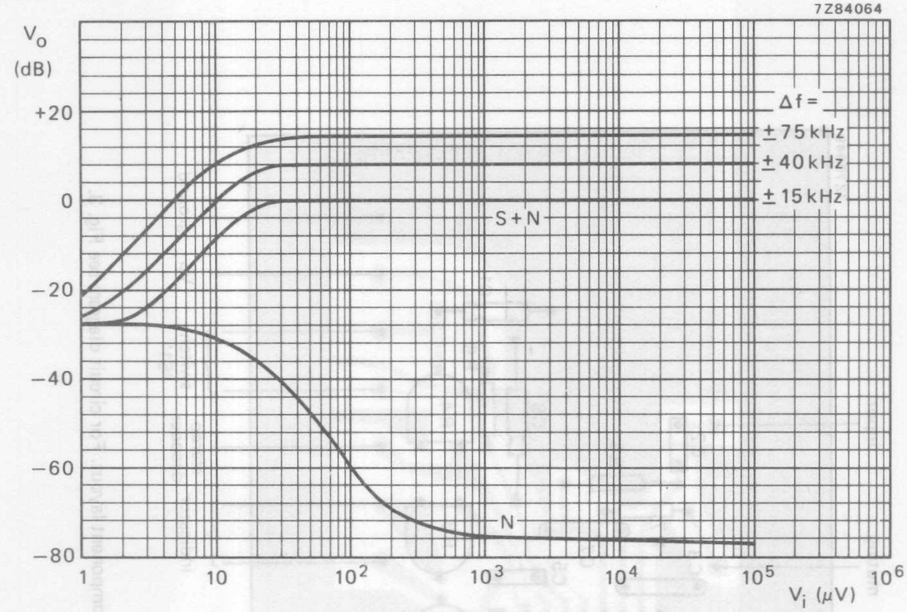



Fig. 5 $V_P$ = 15 V; $f_m$ = 1 kHz; B = 250 Hz to 16 kHz; typical values.

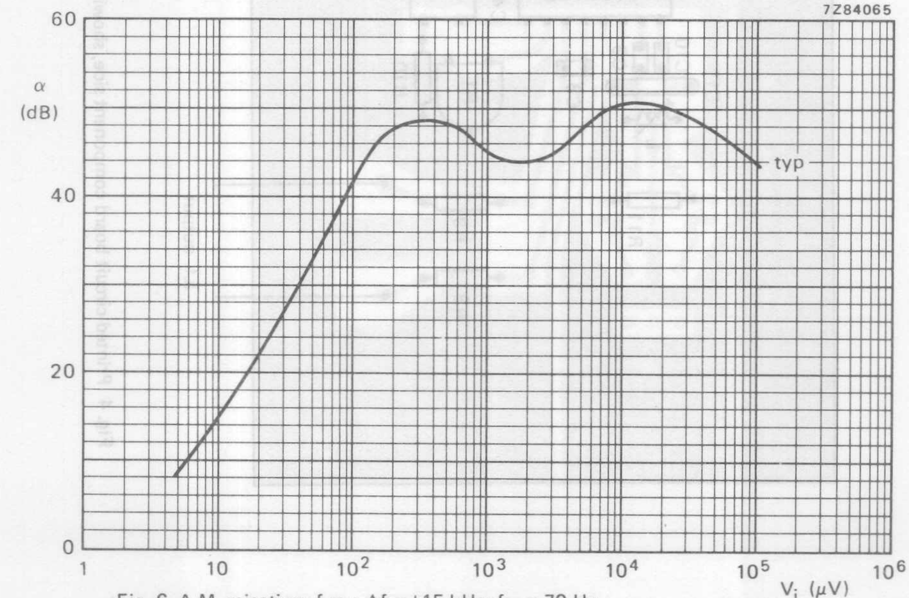



Fig. 6 A.M. rejection; f.m.: $\Delta f$ = ±15 kHz; $f_m$ = 70 Hz.
a.m.: m = 30%; $f_m$ = 1 kHz; simultaneously modulated.

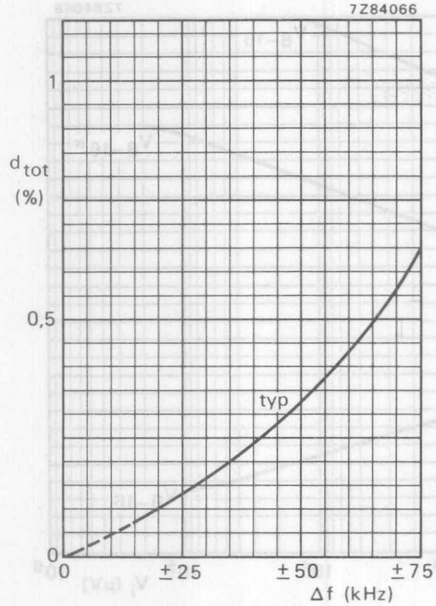



Fig. 7 Total distortion as a function of frequency deviation; single tuned circuit with $Q_L$ = 20; $f_m$ = 1 kHz; $C_{5\text{-}6}$ = 220 pF.

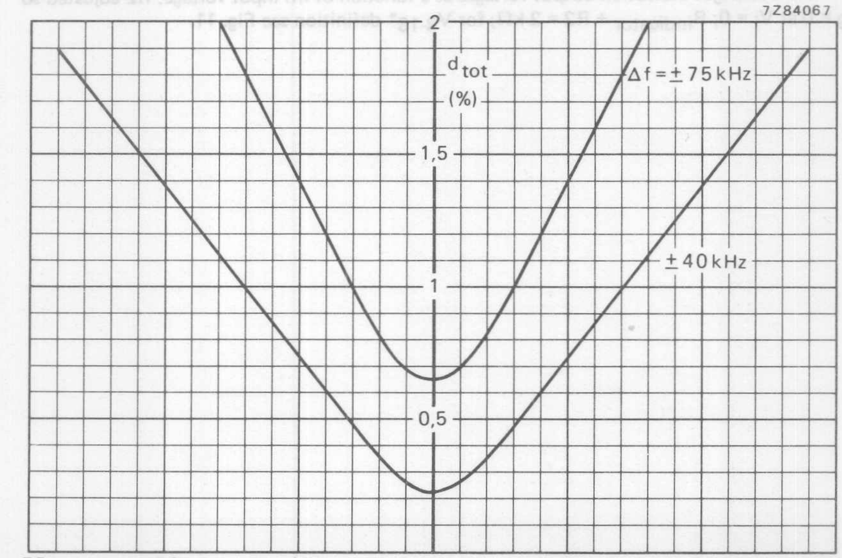



Fig. 8 Total distortion as a function of detuning; single tuned circuit with $Q_L$ = 20; $f_m$ = 1 kHz; $C_{5\text{-}6}$ = 220 pF.

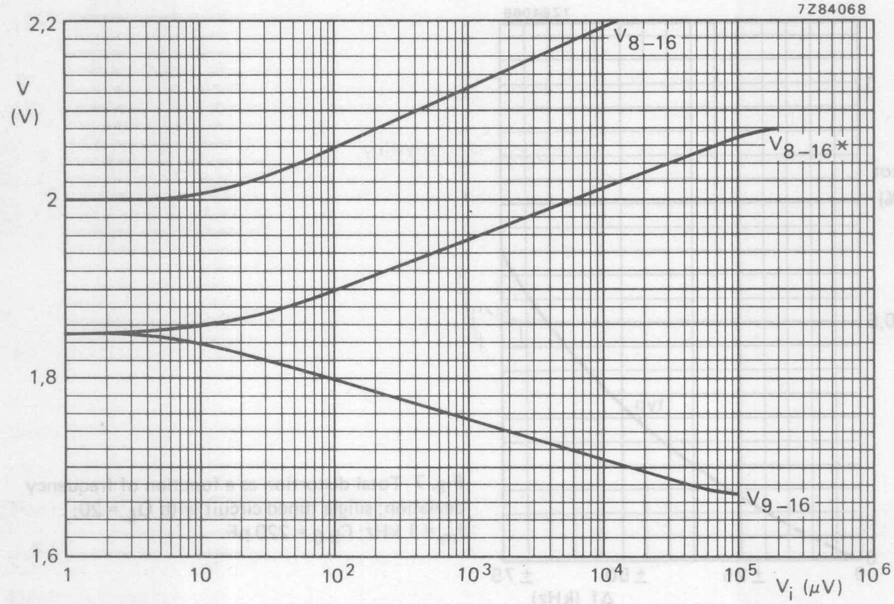



Fig. 9 Field-strength indication output voltages as a function of i.f. input voltage; R2 adjusted so $V_{8\text{-}9} = 0$ at $V_i = 0$; $R_{indicator} + R2 = 2\ k\Omega$; for $V_{8\text{-}16}$* definition see Fig. 11.

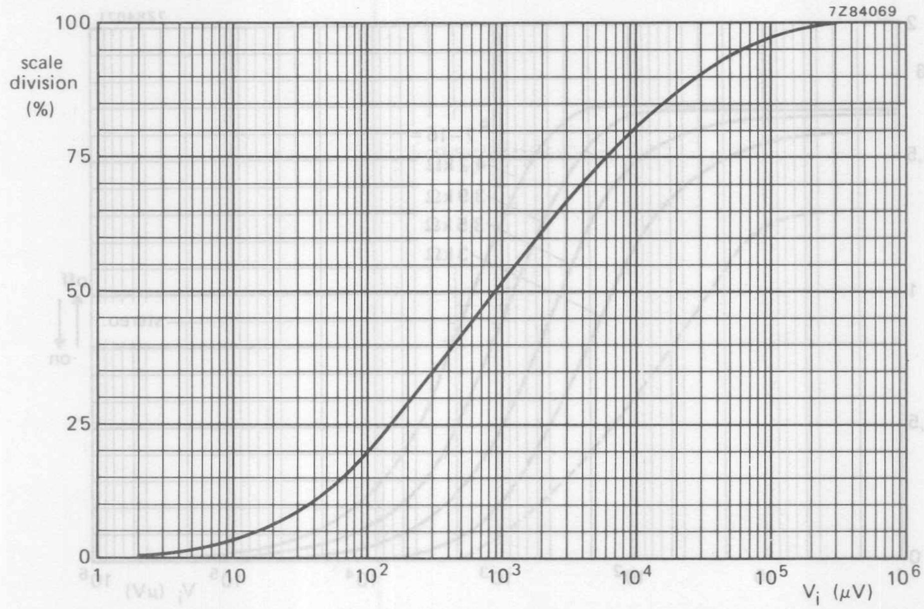



Fig. 9 Scale division of indicator as a function of i.f. input voltage; R2 adjusted so $V_{8\text{-}9} = 0$ at $V_i = 0$; $R_{indicator} = 2\ k\Omega$; R3 adjusted at indication 100%; indicator current = 140 $\mu$A; see Fig. 11.

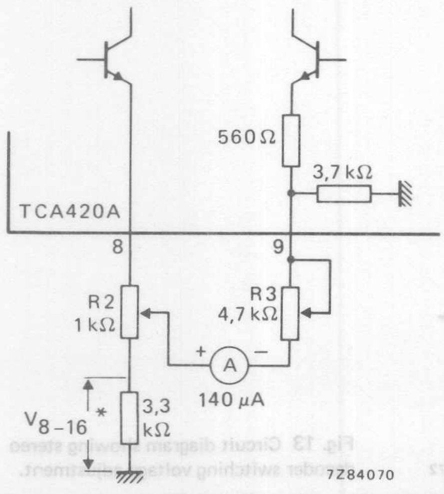



Fig. 11 Circuit diagram showing field-strength indicator adjustment components.

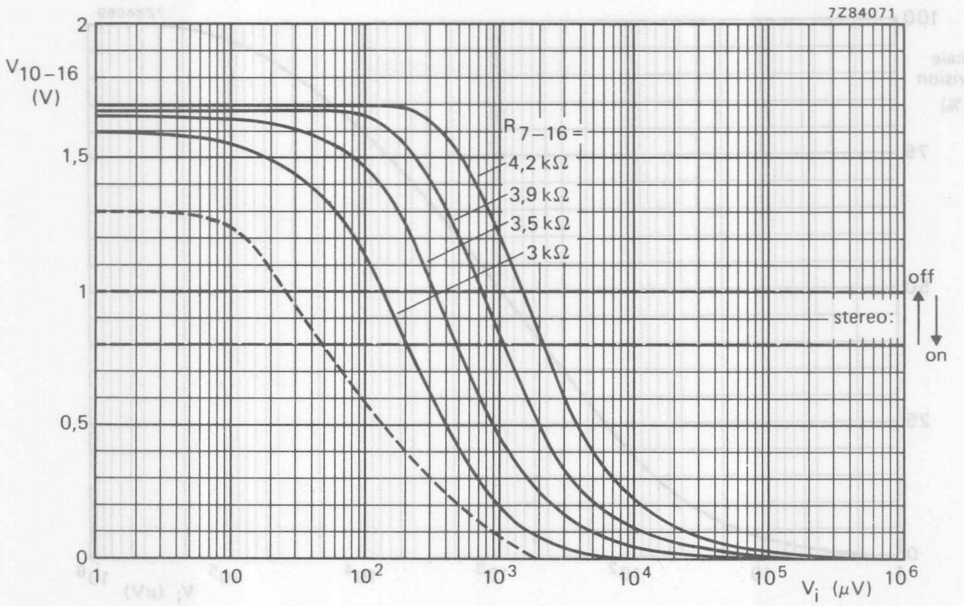



Fig. 12 Stereo decoder switching voltage as a function of i.f. input voltage; R4 = 3,9 kΩ; – – – R1 adjusted so $V_{10\text{-}16}$ = 0 at $V_i$ = 0; see Fig. 13.

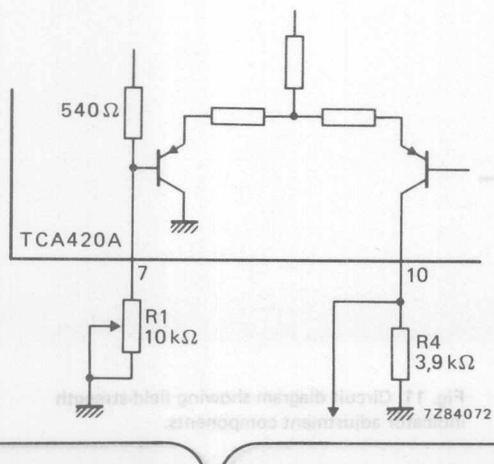



Fig. 13 Circuit diagram showing stereo decoder switching voltage adjustment.

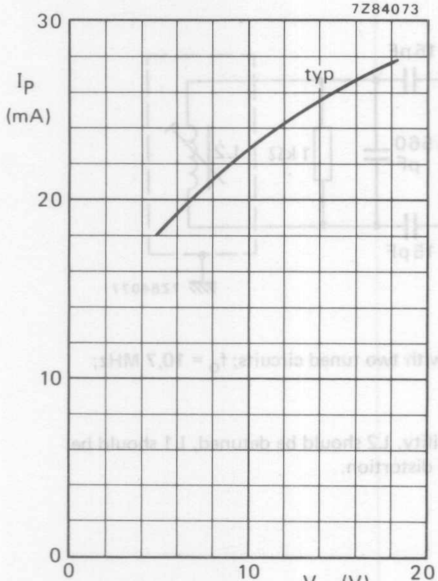



Fig. 14 Supply current consumption.

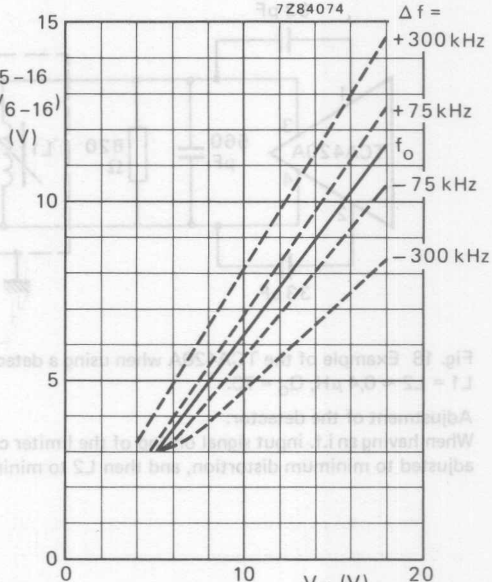



Fig. 15 Output voltage range.

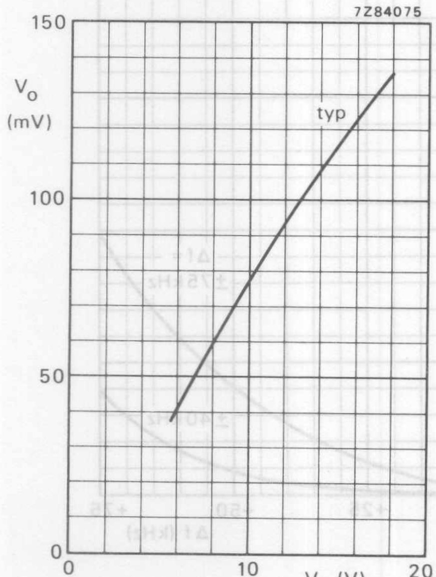



Fig. 16 A.F. output voltage; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz; $V_i = 1$ mV.

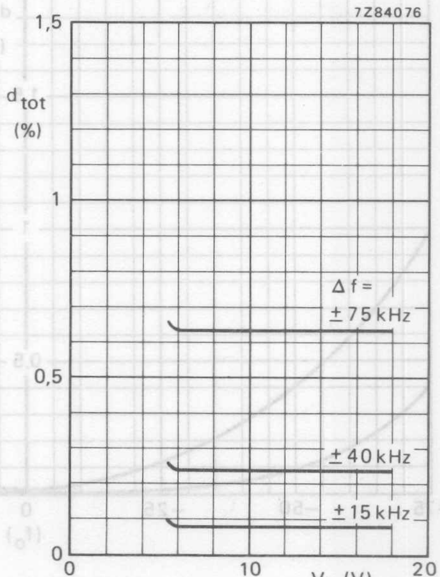



Fig. 17 Total distortion; $f_m = 1$ kHz; $V_i = 1$ mV; $C_{5-6} = 220$ pF.

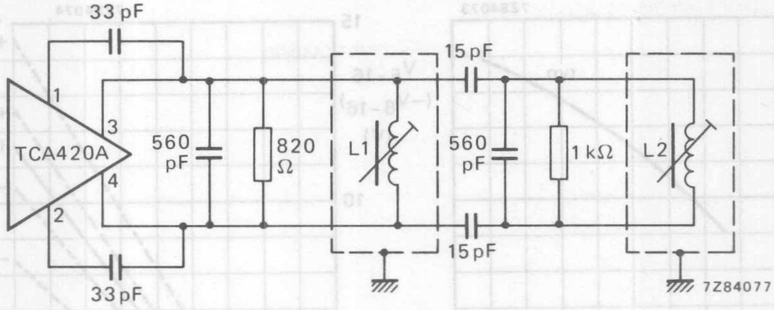



Fig. 18 Example of the TCA420A when using a detector with two tuned circuits; $f_o$ = 10,7 MHz; L1 = L2 ≈ 0,4 μH; $Q_o$ = 70.

Adjustment of the detector:
When having an i.f. input signal on top of the limiter capability, L2 should be detuned, L1 should be adjusted to minimum distortion, and then L2 to minimum distortion.

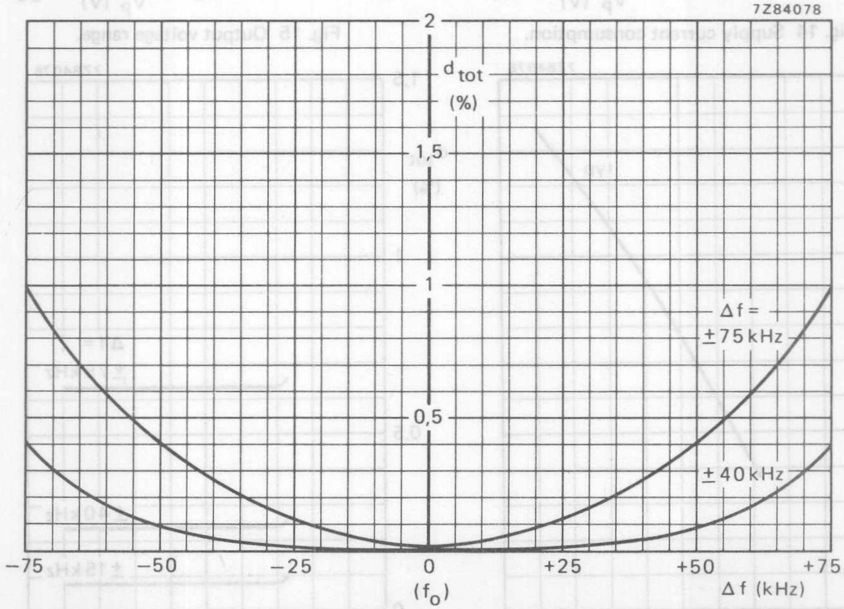



Fig. 19 Total distortion as a function of detuning; circuit as Fig. 18; $f_m$ = 1 kHz; $C_{5\text{-}6}$ = 220 pF. $V_o$ = 500 mV for a frequency deviation Δf = ±75 kHz and $d_{tot}$ < 0,1%.

## APPLICATION INFORMATION

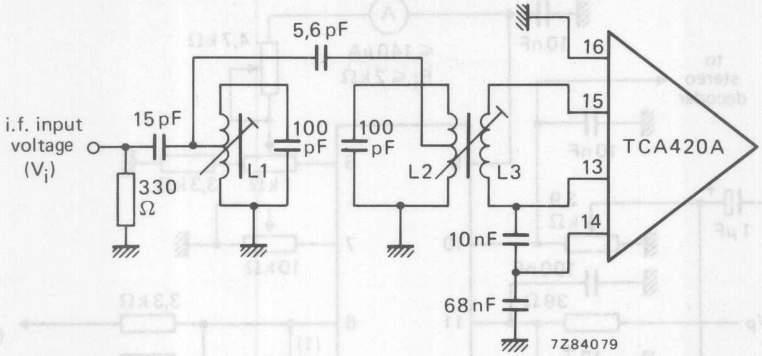



Fig. 20 I.F. coupling circuit, using LC filter; L1 = L2 = 7 + 7 turns h.f. litz wire (5 x 0,04); L3 = 3 turns h.f. litz wire wound on L2 (5 x 0,04).

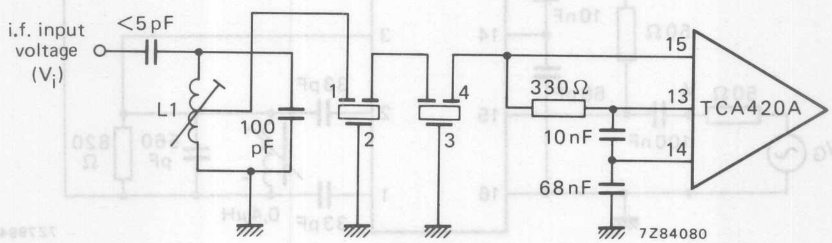
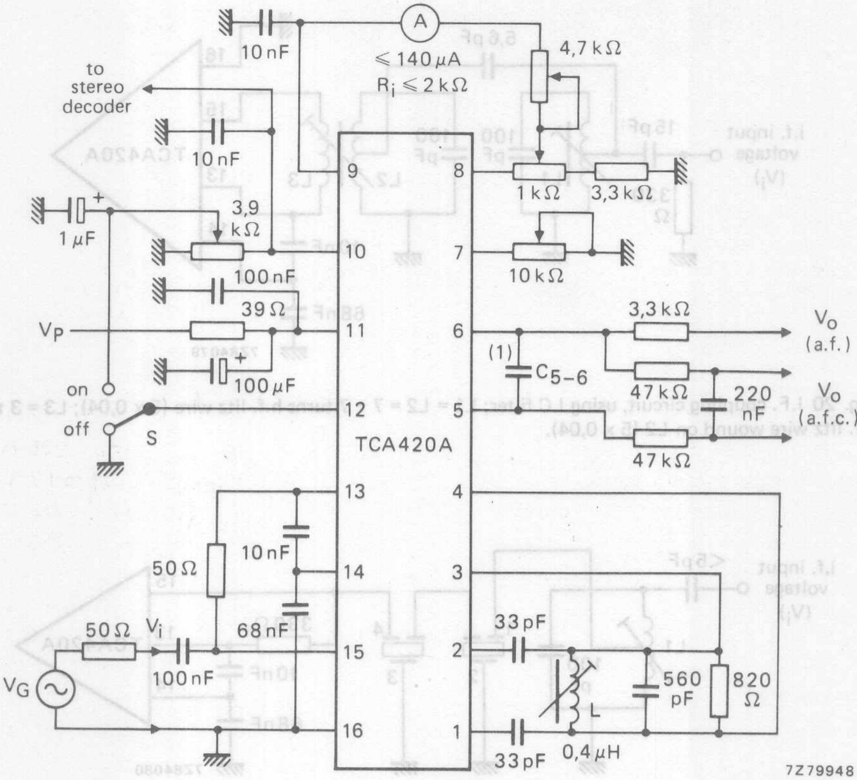



Fig. 21 I.F. coupling circuit, using ceramic filter; L1 = 14 turns h.f. litz wire (5 x 0,04), tab at 3 turns.

APPLICATION INFORMATION (continued)




(1) For mono: $C_{5\text{-}6}$ = 10 nF.
For stereo: $C_{5\text{-}6}$ = 220 pF.

Fig. 22 Application example of using TCA420A.

# D.C. VOLUME AND BALANCE STEREO CONTROL CIRCUIT

The TCA730A is a monolithic integrated circuit for controlling volume and balance in stereo amplifiers by means of a d.c. voltage.

Features:

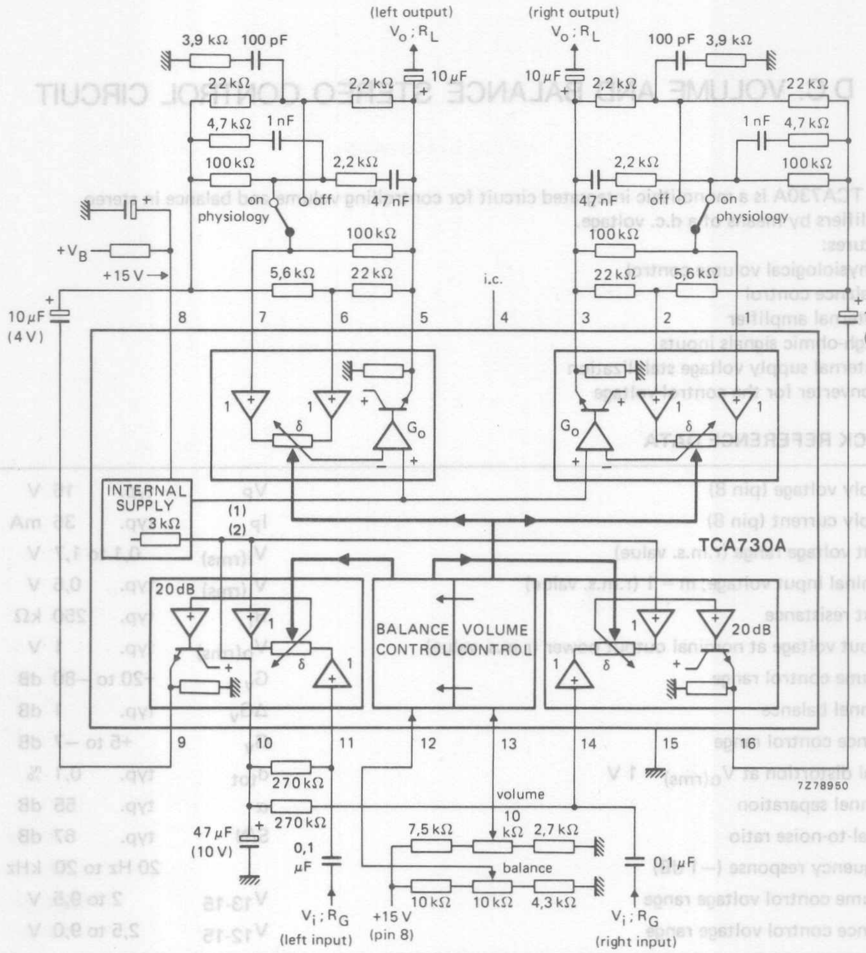
- physiological volume control
- balance control
- internal amplifier
- high-ohmic signals inputs
- internal supply voltage stabilization
- converter for the control voltage

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 8) | $V_P$ | typ. | 15 | V |
| Supply current (pin 8) | $I_P$ | typ. | 35 | mA |
| Input voltage range (r.m.s. value) | $V_{i(rms)}$ | | 0,1 to 1,7 | V |
| Nominal input voltage; m = 1 (r.m.s. value) | $V_{i(rms)}$ | typ. | 0,5 | V |
| Input resistance | $R_i$ | typ. | 250 | kΩ |
| Output voltage at nominal output power (r.m.s. value) | $V_{o(rms)}$ | typ. | 1 | V |
| Volume control range | $G_v$ | | +20 to −80 | dB |
| Channel balance | $\Delta G_v$ | typ. | 1 | dB |
| Balance control range | $G_v$ | | +5 to −7 | dB |
| Total distortion at $V_{o(rms)}$ = 1 V | $d_{tot}$ | typ. | 0,1 | % |
| Channel separation | $\alpha$ | typ. | 55 | dB |
| Signal-to-noise ratio | S/N | typ. | 67 | dB |
| Frequency response (−1 dB) | | | 20 Hz to 20 | kHz |
| Volume control voltage range | $V_{13\text{-}15}$ | | 2 to 9,5 | V |
| Balance control voltage range | $V_{12\text{-}15}$ | | 2,5 to 9,0 | V |
| Supply voltage range (pin 8) | $V_P$ | | 13,5 to 16,5 | V |
| Ambient temperature range | $T_{amb}$ | | −30 to +80 | °C |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).




(1) 6,6 $V_{BE}$; $V_1$ = 4,6 V
(2) 0,35 $V_P$ + 0,65 $V_{BE}$; $V_2$ = 5,7 V.

Fig. 1 Block diagram with external circuitry.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 8) | $V_P$ | max. | 18 V |
| Input voltages | $V_{11\text{-}15}$; $V_{14\text{-}15}$ | min. | 0 V |
| | | max. | $V_P$ V |
| Control voltages | $V_{12\text{-}15}$; $V_{13\text{-}15}$ | min. | −5 V |
| | | max. | 12 V |
| Total power dissipation | $P_{tot}$ | max. | 900 mW |
| Storage temperature range | $T_{stg}$ | | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +80 °C |

## CHARACTERISTICS

$V_P$ = 15 V; $T_{amb}$ = 25 °C; measured in Fig. 1; balance control in mid-position ($V_{12\text{-}10}$ = 0); physiology switch off; f = 1 kHz; $R_G$ = 22 kΩ; $R_L$ = 5,6 kΩ; unless otherwise specified.

| | | | |
|---|---|---|---|
| Supply voltage range (pin 8) | $V_P$ | | 13,5 to 16,5 V |
| Supply current | $I_P$ | typ. | 35 mA |
| | | | 25 to 43 mA |
| **Control range** | | | |
| Voltage gain range | $G_v$ | | 0 to 20 dB |
| Voltage gain at $V_{13\text{-}15}$ = 9,5 V (0,63 $V_P$) | $G_v$ | typ. | 20 dB |
| | | | 18 to 22 dB |
| Voltage attenuation range | $G_v$ | | 0 to −80 dB |
| Voltage attenuation at $V_{13\text{-}15}$ = 3 V (0,2 $V_P$) | $G_v$ | > | −75 dB |
| | | typ. | −80 dB |
| Balance control range at $G_v$ = −10 dB | | | +5 to −7 dB |
| **Control inputs** | | | |
| Recommended control voltage range | | | |
| volume | $V_{13\text{-}15}$ | | 2 to 9,5 V |
| balance | $V_{12\text{-}15}$ | | 2,5 to 9,0 V |
| Control voltage for $G_v$ = −10 dB; $V_{12\text{-}10}$ = 0 | $V_{13\text{-}15}$ | | 6,7 to 7,1 V* |
| Control voltage for balance 0 dB; $V_{13\text{-}15}$ = 6,9 V | $V_{12\text{-}10}$ | typ. | 0 ± 0,2 V |
| Internal supply voltage (0,35 $V_P$ + 0,65 $V_{BE}$) | $V_{10\text{-}15}$ | typ. | 5,9 V |
| | | | 5,7 to 6,1 V |
| Output resistance (pin 10) | $R_{o10}$ | typ. | 3 kΩ |
| Control current | | | |
| volume ($V_{13\text{-}15}$ = 6,9 V) | $I_{13}$ | typ. | 15 µA |
| | | < | 50 µA |
| balance ($V_{12\text{-}15}$ = 5,9 V) | $I_{12}$ | typ. | 8 µA |
| | | < | 25 µA |
| Input resistance | | | |
| pin 13 (volume) | $R_{i13}$ | typ. | 500 kΩ |
| pin 12 (balance) | $R_{i12}$ | typ. | 600 kΩ |

* Typical value 6,9 V.

**CHARACTERISTICS** (continued)

**Signal processing**

| | | | |
|---|---|---|---|
| Frequency response (−1 dB) | f | | 20 Hz to 20 kHz |
| Input resistance; $R_{11\text{-}10} = R_{14\text{-}10} = 270\ k\Omega$ (pins 11; 14) | $R_{i11;14}$ | typ. | 250 kΩ |
| Output resistance (pins 3; 5) | $R_{o3;5}$ | typ. | 10 Ω |
| Maximum input voltage; $V_{o(rms)} < 1$ V; $d_{tot} = 0{,}7$ % (r.m.s. value) | $V_{i(rms)}$ | > <br> typ. | 1,3 V <br> 1,7 V |
| Maximum output voltage; $V_{i(rms)} < 1$ V; $d_{tot} = 0{,}7$% (r.m.s. value) | $V_{o(rms)}$ | > <br> typ. | 1,8 V <br> 2,0 V |
| Nominal input voltage; m = 1 (r.m.s. value) | $V_{i(rms)}$ | typ. | 0,5 V |
| Nominal output voltage at nominal output power (r.m.s. value) | $V_{o(rms)}$ | typ. | 1 V |
| Total distortion | | | |
| $V_{o(rms)} = 1$ V; $G_v$ = maximum | $d_{tot}$ | typ. <br> < | 0,07 % <br> 0,2 % |
| $V_{o(rms)} = 1$ V; $V_{i\ (rms)} = 1$ V | $d_{tot}$ | typ. | 0,2 % |
| $V_{o(rms)} = 50$ mV; $V_{i(rms)} = 150$ mV | $d_{tot}$ | typ. <br> < | 0,03 % <br> 0,1 % |
| $V_{o(rms)} = 50$ mV; $V_{i(rms)} = 1$ V | $d_{tot}$ | typ. | 0,2 % |
| Output noise voltage; f = 20 Hz to 20 kHz | | | |
| signal plus noise voltage (r.m.s. value) | | | |
| $G_v = -60$ dB | $V_{no(rms)}$ | typ. | 6 μV |
| $G_v = -10$ dB | $V_{no(rms)}$ | typ. | 15 μV |
| $G_v$ = maximum (+20 dB) | $V_{no(rms)}$ | typ. | 100 μV |
| noise voltage; weighted conform DIN45405 (peak value) | | | |
| $G_v = -60$ dB | $V_{no(m)}$ | typ. | 15 μV |
| $G_v = -10$ dB | $V_{no(m)}$ | typ. <br> < | 35 μV <br> 80 μV |
| $G_v$ = maximum (+20 dB) | $V_{no(m)}$ | typ. <br> < | 230 μV <br> 350 μV |
| Channel separation; $G_v = \pm 20$ dB; $V_i = V_o < 1$ V | | | |
| f = 250 Hz to 12,5 kHz | α | > <br> typ. | 52 dB <br> 53 dB |
| f = 40 Hz to 16 kHz | α | > <br> typ. | 46 dB <br> 50 dB |
| Channel balance | | | |
| $G_v = +15$ to $-50$ dB | $\Delta G_v$ | typ. <br> < | 1 dB <br> 2 dB |
| $G_v < 50$ dB | $\Delta G_v$ | typ. | 2 dB |

**Amplifier characteristics**

| | | | | |
|---|---|---|---|---|
| Input resistance (pins 11 and 14) | $R_{i11;14}$ | > | 3 | MΩ |
| D.C. output voltages | | | | |
| $(0,35\ V_P - 1,35\ V_{BE})$ | $V_{3\text{-}15}$; $V_{16\text{-}15}$ | typ. | 4,2 | V |
| $(6,6\ V_{BE})$ | $V_{3\text{-}15}$; $V_{16\text{-}15}$ | typ. | 4,6 | V |
| Quiescent input currents (pins 1,2,6,7,11,14) | $I_1$; $I_2$; $I_6$; $I_7$; $I_{11}$; $I_{14}$ | typ. | 0,5 | μA |
| | | < | 2 | μA |
| Input resistance (pins 1,2,6 and 7) of physiology; without external circuitry | $R_{i1;2;6;7}$ | > | 1 | MΩ |
| Internal load resistance at outputs (pins 3,5,9,16) | $R_{3\text{-}15}$; $R_{5\text{-}15}$; $R_{9\text{-}15}$; $R_{10\text{-}15}$ | typ. | 2 | kΩ |
| Maximum gain; no load | $G_{3\text{-}1}$; $G_{3\text{-}2}$; $G_{5\text{-}6}$; $G_{5\text{-}7}$ | > | 40 | dB |
| | | typ. | 43 | dB |

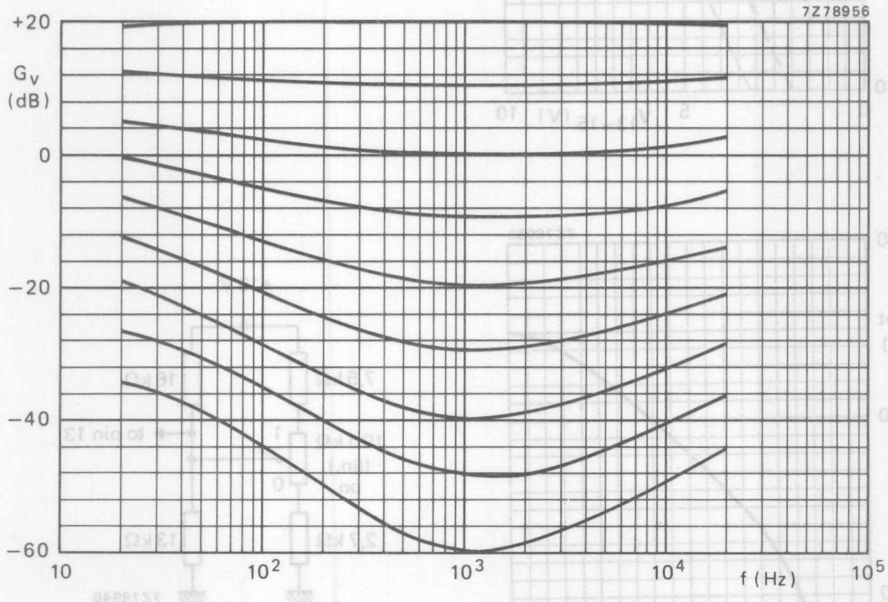



Fig. 2 Frequency response volume control with physiology.

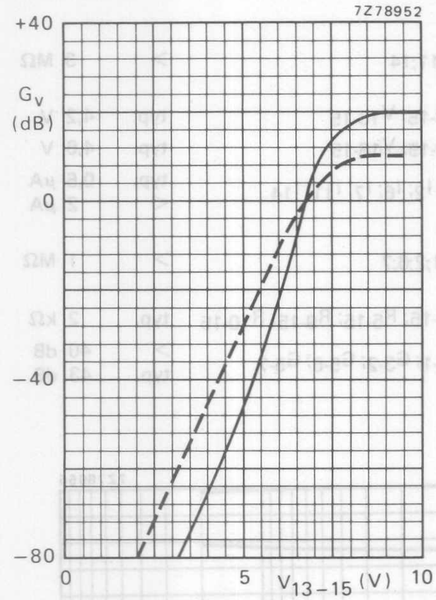
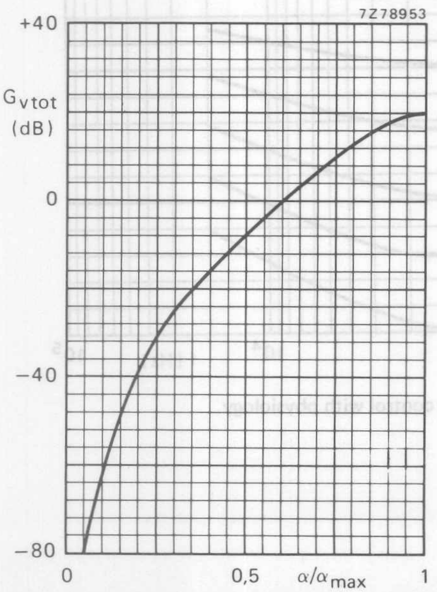



Fig. 3 Volume control curves; without physiology; balance = 0; $V_{12\text{-}10} = 0$.

—— $G_{v\ tot}$; $G_{v\ 5\text{-}11}$; $G_{v\ 3\text{-}14}$

– – – $G_{v\ 9\text{-}11}$; $G_{v\ 16\text{-}14}$



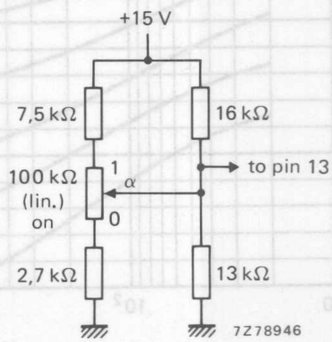




Fig. 4 Volume adjustment curve; balance = 0; $V_{12\text{-}10} = 0$.

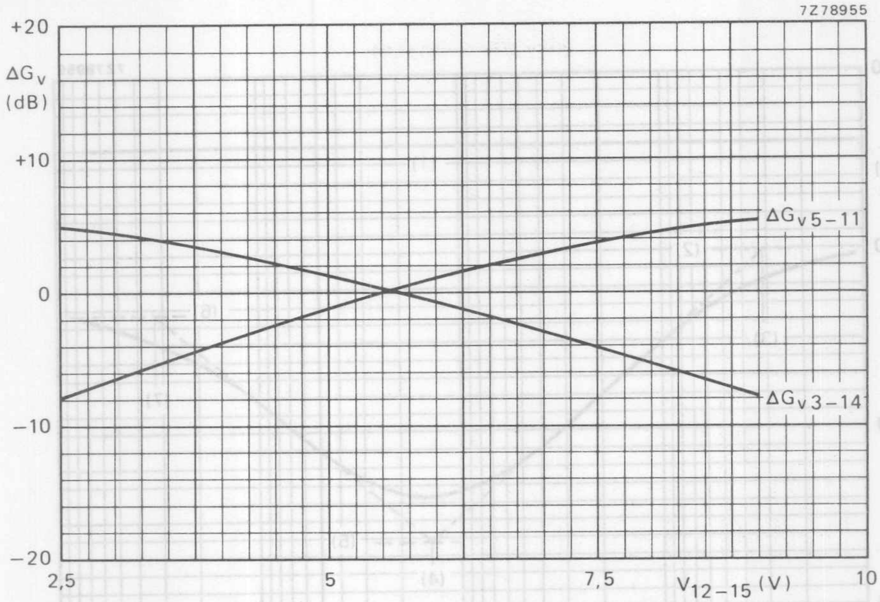



Fig. 5 Balance control curves; $G_{v\,tot} = -10$ dB ($V_{13\text{-}15} = 6{,}9$ V); for balance = 0.

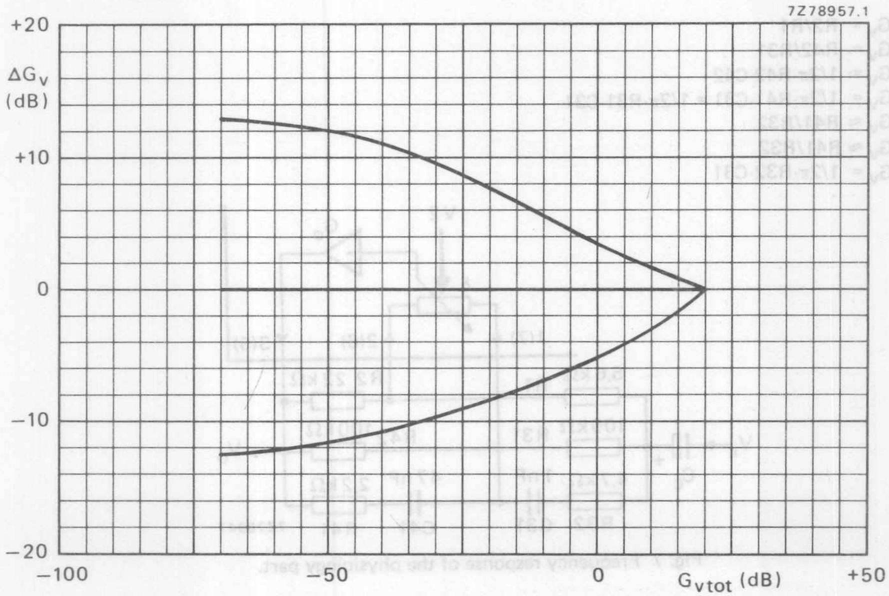
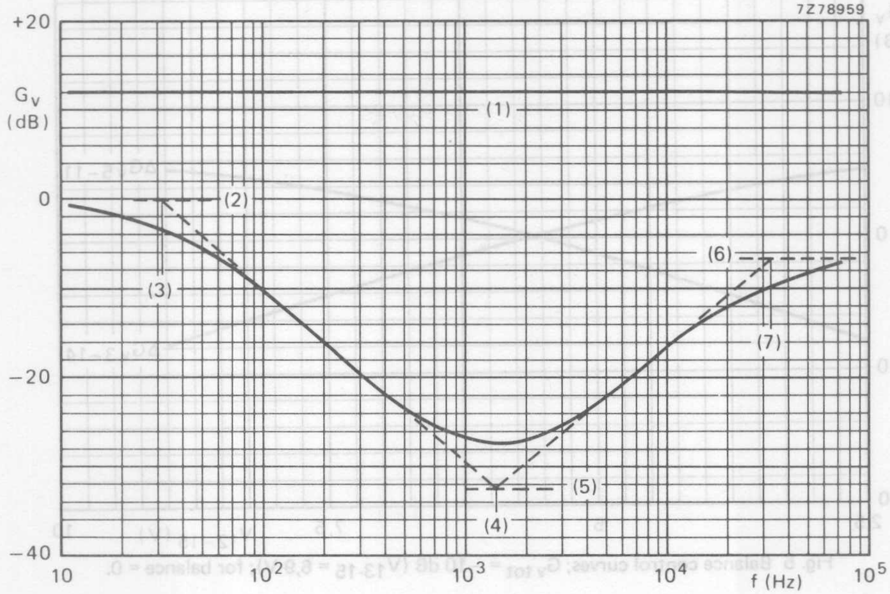



Fig. 6 Balance control range; $V_{12\text{-}15} = 2{,}5$ to $9{,}0$ V.




(1) $G_v$ = R2/R1
(2) $G_v$ = R42/R31
(3) $G_v$ = $1/2\pi \cdot R42 \cdot C42$
(4) $G_v$ = $1/2\pi \cdot R41 \cdot C31 = 1/2\pi \cdot R31 \cdot C31$
(5) $G_v \approx$ R41/R32
(6) $G_v \approx$ R41/R32
(7) $G_v$ = $1/2\pi \cdot R32 \cdot C31$

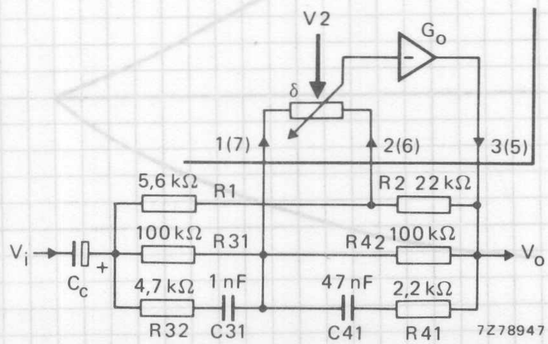



Fig. 7 Frequency response of the physiology part.

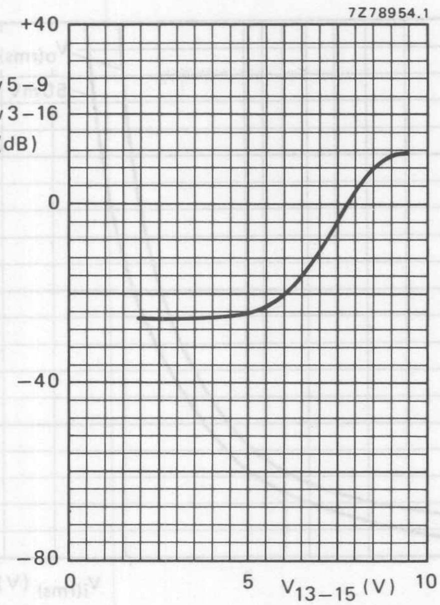



Fig. 8 Physiology control curve; f = 1 kHz; balance = 0; $V_{12\text{-}15}$ = 0.

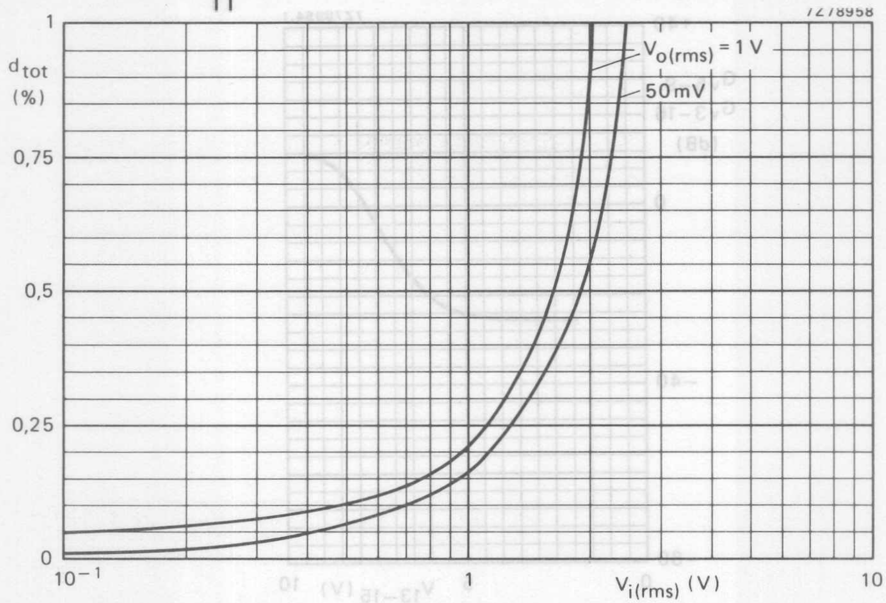



Fig. 9 Total distortion as a function of r.m.s. input voltage; f = 1 kHz; $R_L$ = 5,6 kΩ.

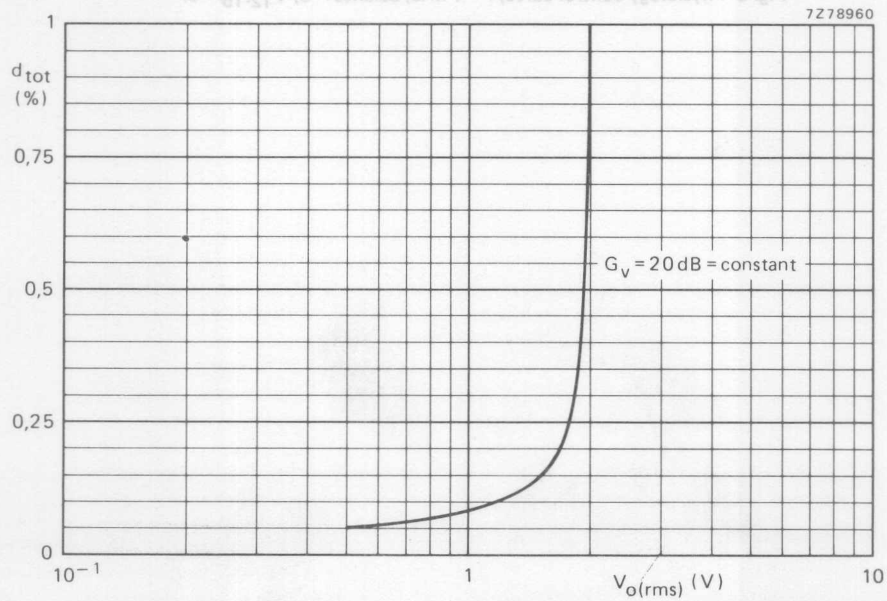



Fig. 10 Total distortion as a function of r.m.s. output voltage; f = 1 kHz; $R_L$ = 5,6 kΩ.

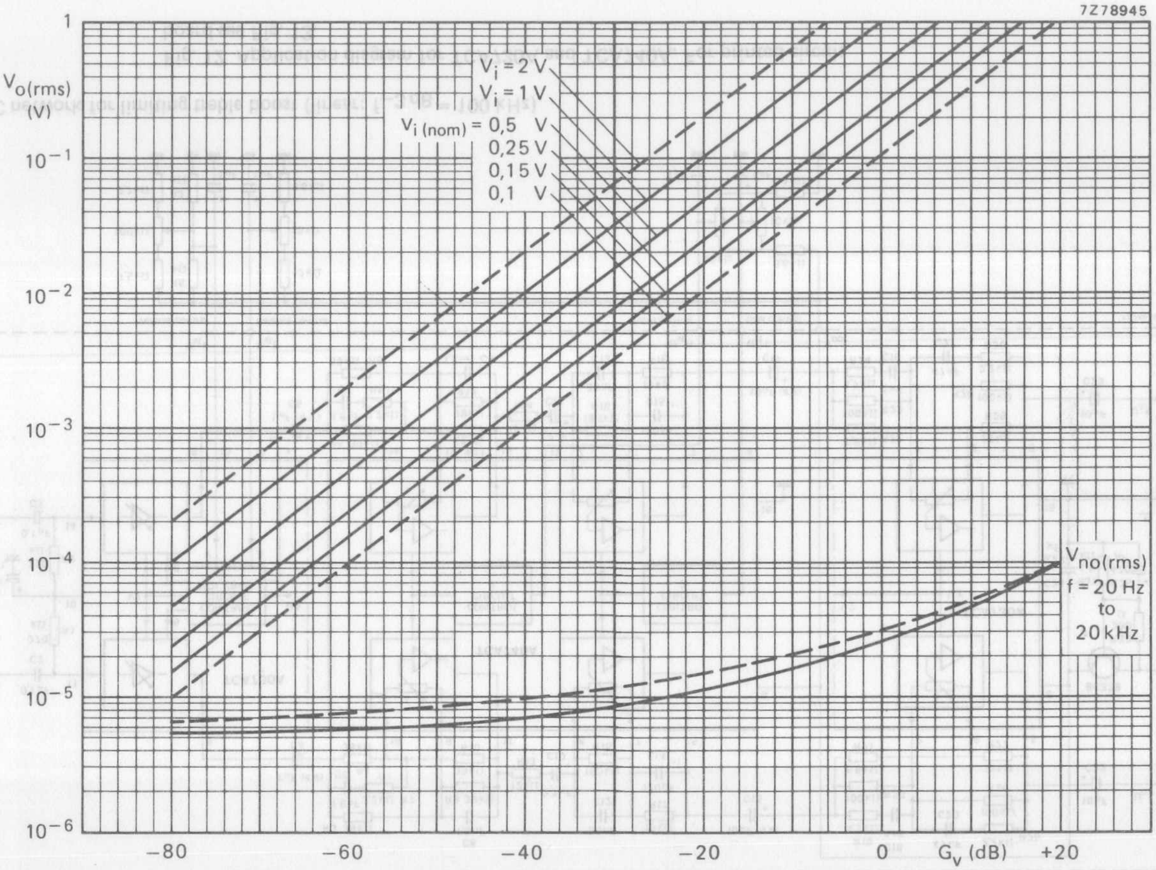
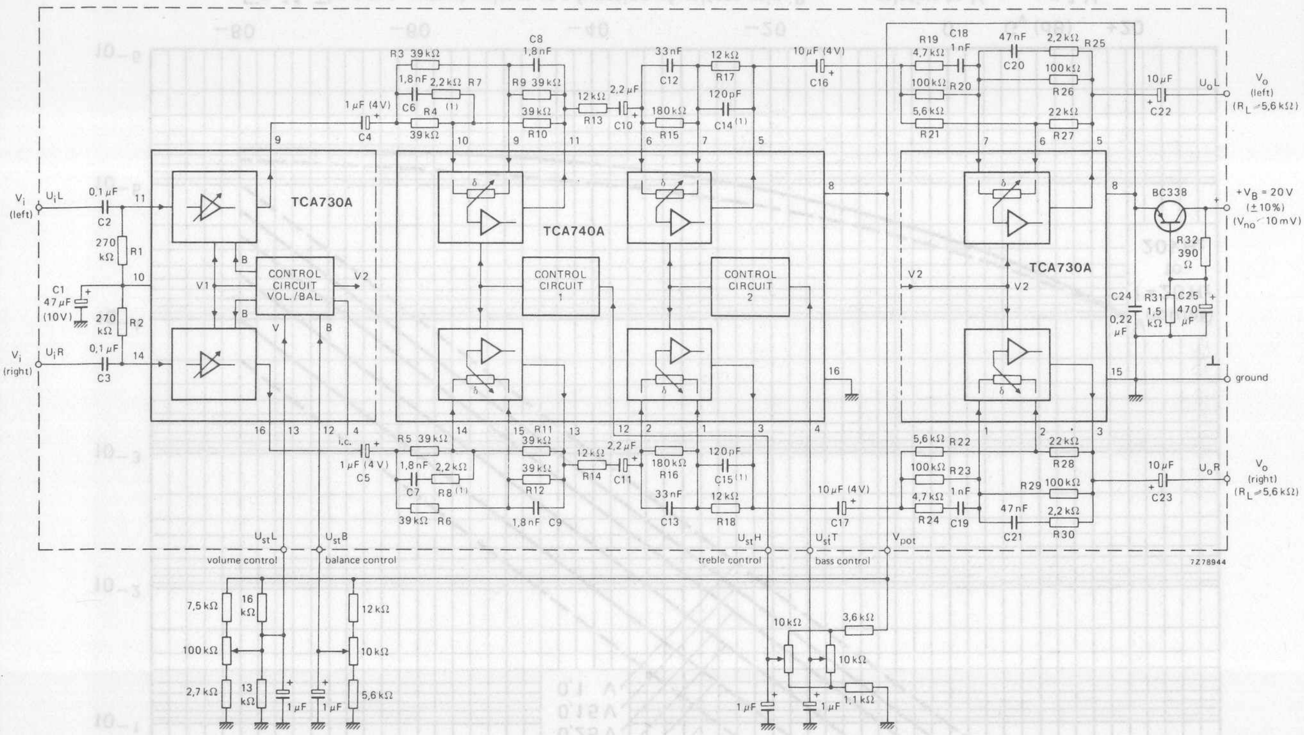



Fig. 11 The r.m.s. output voltage as a function of voltage gain; $P_{o(nom)}$ relative to $V_{o(rms)}$ = 1 V.
—— without physiological volume control; – – – with physiological volume control.

## APPLICATION INFORMATION




(1) RC network for limiting treble boost (linear: $f_{-3\,dB}$ = 100 kHz).

Fig. 12 Application diagram for TCA730A and TCA740A. For printed-circuit board see Fig. 13.

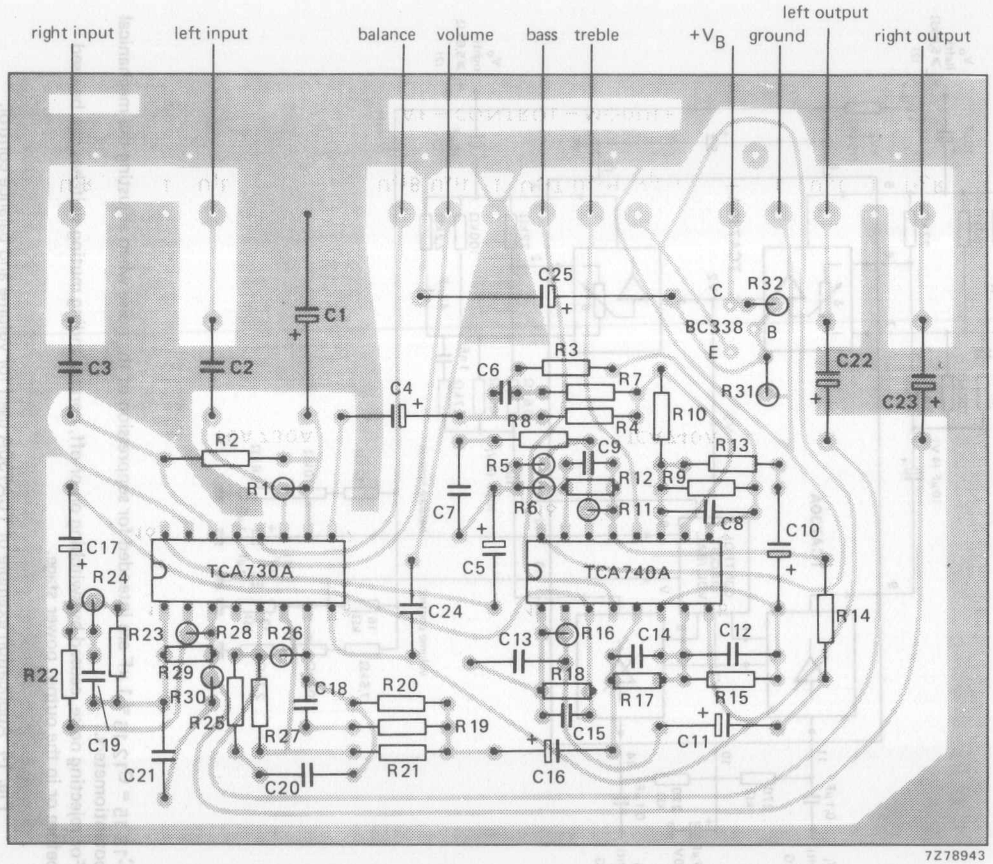
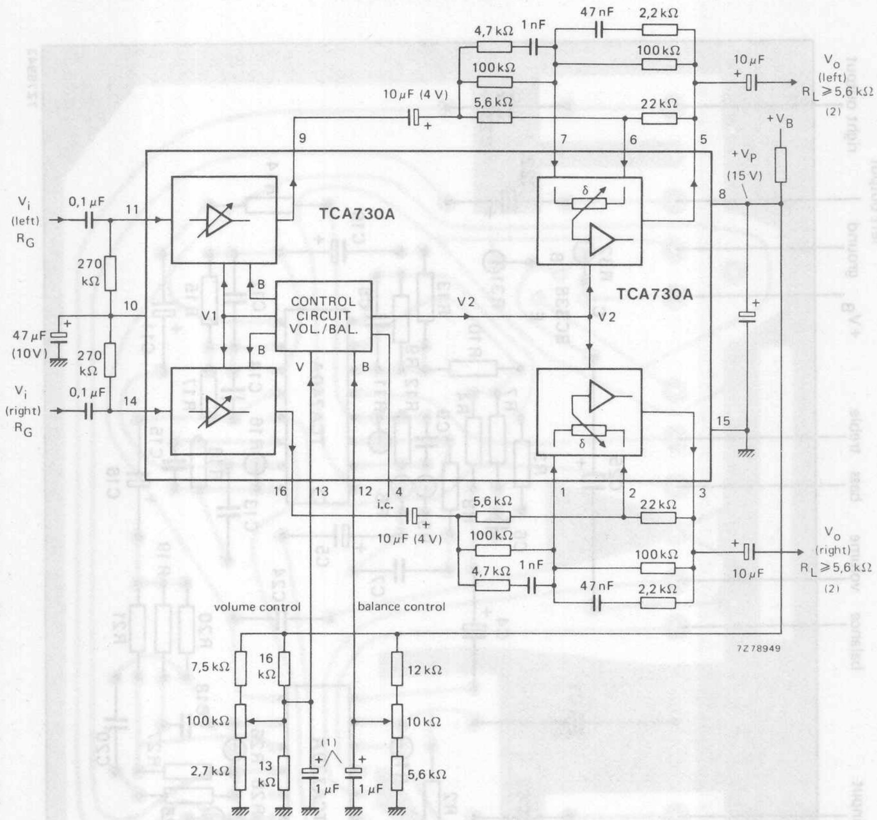



Fig. 13 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 12.

APPLICATION INFORMATION (continued)




(1) $C_{13\text{-}15} = C_{12\text{-}15} = 1\ \mu F$ are intended for suppression of the noise when adjusting the mechanical potentiometers.

(2) For rejecting noise, caused by switching on or off, corresponding muting switches can be used before or in the output power stage.

Fig. 14 Application example of TCA730A used for volume and balance control.

# D.C. TREBLE AND BASS STEREO CONTROL CIRCUIT

The TCA740A is a monolithic integrated circuit for controlling treble and bass in stereo amplifiers by means of a d.c. voltage.

Features:

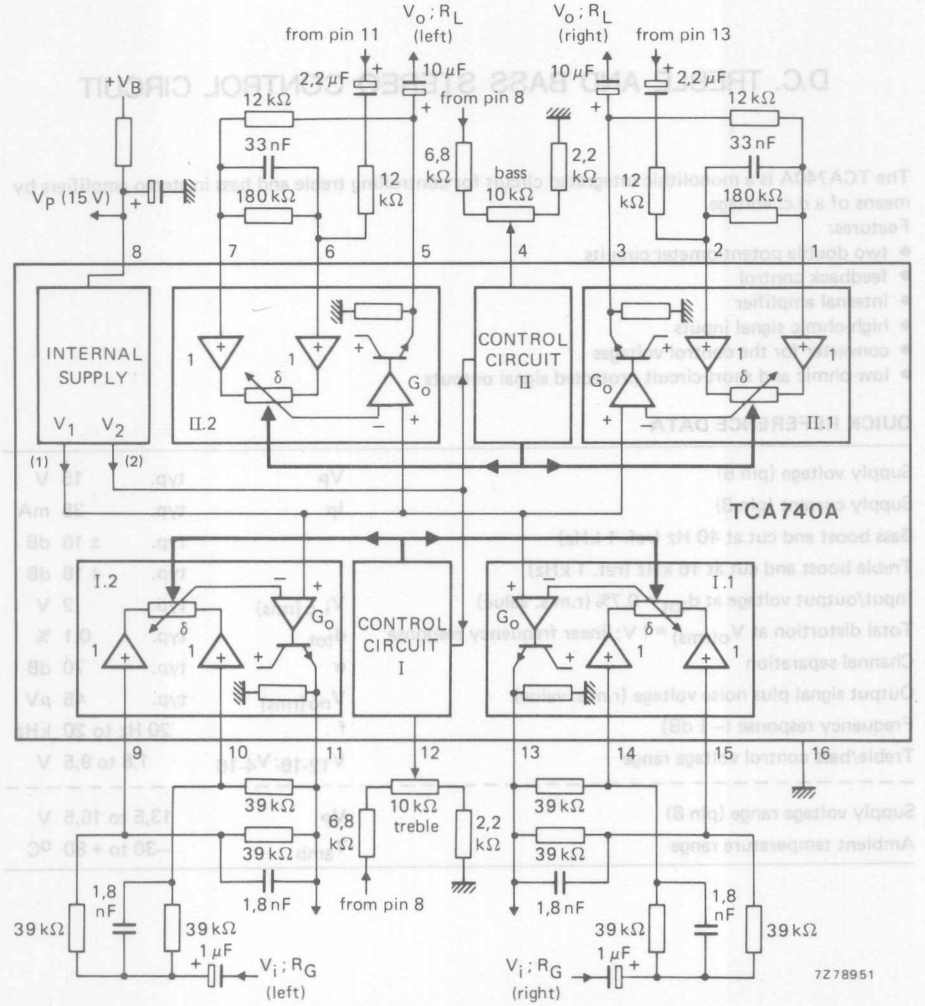
- two double potentiometer circuits
- feedback control
- internal amplifier
- high-ohmic signal inputs
- converter for the control voltages
- low-ohmic and short-circuit protected signal outputs

**QUICK REFERENCE DATA**

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 8) | $V_P$ | typ. | 15 | V |
| Supply current (pin 8) | $I_P$ | typ. | 35 | mA |
| Bass boost and cut at 40 Hz (ref. 1 kHz) | | typ. | ± 16 | dB |
| Treble boost and cut at 16 kHz (ref. 1 kHz) | | typ. | ± 16 | dB |
| Input/output voltage at $d_{tot}$ = 0,7% (r.m.s. value) | $V_{i,o(rms)}$ | typ. | 2 | V |
| Total distortion at $V_{o(rms)}$ = 1 V; linear frequency response | $d_{tot}$ | typ. | 0,1 | % |
| Channel separation | $\alpha$ | typ. | 70 | dB |
| Output signal plus noise voltage (r.m.s. value) | $V_{no(rms)}$ | typ. | 45 | $\mu$V |
| Frequency response (−1 dB) | f | | 20 Hz to 20 | kHz |
| Treble/bass control voltage range | $V_{12\text{-}16}$; $V_{4\text{-}16}$ | | 1,8 to 9,5 | V |
| Supply voltage range (pin 8) | $V_P$ | | 13,5 to 16,5 | V |
| Ambient temperature range | $T_{amb}$ | | −30 to + 80 | °C |

**PACKAGE OUTLINE**

16-lead DIL; plastic (SOT-38).




(1) 6,6 $V_{BE}$; $V_1$ = 4,6 V

(2) 0,31 $V_P$ + 1,4 $V_{BE}$; $V_2$ = 5,6 V

Fig. 1 Block diagram with external circuitry.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 8) | $V_P$ | max. | 18 V |
| Control voltages (pins 4 and 12) | $V_{4\text{-}16}$ | max. | 12 V |
| | $-V_{4\text{-}16}$ | max. | 5 V |
| | $V_{12\text{-}16}$ | max. | 12 V |
| | $-V_{12\text{-}16}$ | max. | 5 V |
| Total power dissipation | $P_{tot}$ | max. | 900 mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 °C |

## CHARACTERISTICS

$V_P$ = 15 V; $T_{amb}$ = 25 °C; measured in Fig.1; in position 'linear' ($V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V);
$R_G$ = 60 Ω; $R_L$ = 5,6 kΩ; f = 1 kHz; unless otherwise specified

| | | | |
|---|---|---|---|
| Supply voltage range (pin 8) | $V_P$ | | 13,5 to 16,5 V |
| Supply current (pin 8) | $I_P$ | typ. | 34 mA |
| | | | 25 to 45 mA |

**Signal processing**

| | | | |
|---|---|---|---|
| Voltage gain at linear frequency response | $G_v$ | typ. | 0 dB |
| Frequency response (−1 dB) | f | | 20 Hz to 20 kHz |
| Maximum gain variation at f = 1 kHz at maximum bass/treble boost or cut | $\Delta G_v$ | < | ±1,5 dB |
| Bass boost at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 9,2 V | | > | 15 dB |
| | | typ. | 16 dB |
| Bass cut at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 2 V | | > | 15 dB |
| | | typ. | 16 dB |
| Treble boost at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 9,2 V | | > | 15 dB |
| | | typ. | 16 dB |
| Treble cut at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 2 V | | > | 15 dB |
| | | typ. | 16 dB |
| Total distortion | | | |
| $V_{o(rms)}$ = 100 mV; f = 1 kHz | $d_{tot}$ | typ. | 0,03 % |
| $V_{o(rms)}$ = 100 mV; f = 40 Hz to 16 kHz | $d_{tot}$ | typ. | 0,1 % |
| $V_{o(rms)}$ = 1 V; f = 1 kHz | $d_{tot}$ | typ. | 0,07 % |
| | | < | 0,2 % |
| $V_{o(rms)}$ = 1 V; f = 40 Hz to 16 kHz | $d_{tot}$ | typ. | 0,2 % |
| Input/output voltage at $d_{tot}$ = 0,7 % (r.m.s. value) | $V_{i(rms)} = V_{o(rms)}$ | > | 1,6 V |
| | | typ. | 2 V |
| Output signal plus noise voltage (r.m.s. value) f = 20 Hz to 20 kHz | $V_{no(rms)}$ | typ. | 40 μV |
| Output noise voltage; weighted conform DIN45405; peak value | $V_{no(m)}$ | typ. | 90 μV |
| | | < | 160 μV |

**CHARACTERISTICS** (continued)

| | | | | |
|---|---|---|---|---|
| Channel separation | | | | |
| f = 1 kHz | $\alpha$ | typ. | 72 | dB |
| f = 250 Hz to 12,5 kHz | $\alpha$ | typ. | 68 | dB |
| f = 40 Hz to 16 kHz | $\alpha$ | > | 50 | dB |
| | | typ. | 58 | dB |
| **Control voltages** | | | | |
| Recommended control voltage range | | > | 0 | V |
| treble/bass | $V_{4\text{-}16} = V_{12\text{-}16}$ | | 2 to 9,2 | V |
| | | < | 0,66 $V_P$ | V |
| | | typ. | 5,6 | V |
| Control voltage at linear frequency response | $V_{4\text{-}16} = V_{12\text{-}16}$ | | 5,4 to 5,8 | V |
| | | | (0,31 $V_P$ to 1,4 $V_{BE}$) | V |
| Quiescent input current | | | | |
| $V_{4\text{-}16} = V_{12\text{-}16}$ = 2 to 9,2 V | $I_4 = I_{12}$ | typ. | 6 | $\mu$A |
| | | < | 25 | $\mu$A |
| Input resistance (pins 4 and 12) | | | | |
| $V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V | $R_{i4;12}$ | typ. | 800 | k$\Omega$ |
| **Amplifier characteristics** | | | | |
| Quiescent input currents; $V_i$ = 4,6 V | | typ. | 0,6 | $\mu$A |
| (pins 1, 2, 6, 7, 9, 10, 14 and 15) | $I_1;I_2;I_6;I_7;I_9;I_{10};I_{14};I_{15}$ | < | 2 | $\mu$A |
| Input resistance (pins 1,2,6,7,9,10,14 and 15) | $R_{i\,1;2;6;7;9;10;14;15}$ | > | 1 | M$\Omega$ |
| Internal emitter resistance at outputs | $R_{3\text{-}16}$; $R_{5\text{-}16}$; $R_{11\text{-}16}$; $R_{13\text{-}16}$ | typ. | 2 | k$\Omega$ |
| Output resistance (pins 3,5,11 and 13) | $R_{o\,3;5;11;13\text{-}16}$ | typ. | 10 | $\Omega$ |
| Maximum gain; no load | $G_v$ | > | 40 | dB |
| | | typ. | 43 | dB |
| D.C. output voltages | | typ. | 4,6 | V |
| $V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V (pins 3,5,11 and 13) | $V_{3\text{-}16}$; $V_{5\text{-}16}$; $V_{11\text{-}16}$; $V_{13\text{-}16}$ | | 4,3 to 4,9 | V |
| | | | (6,6 $V_{BE}$) | V |

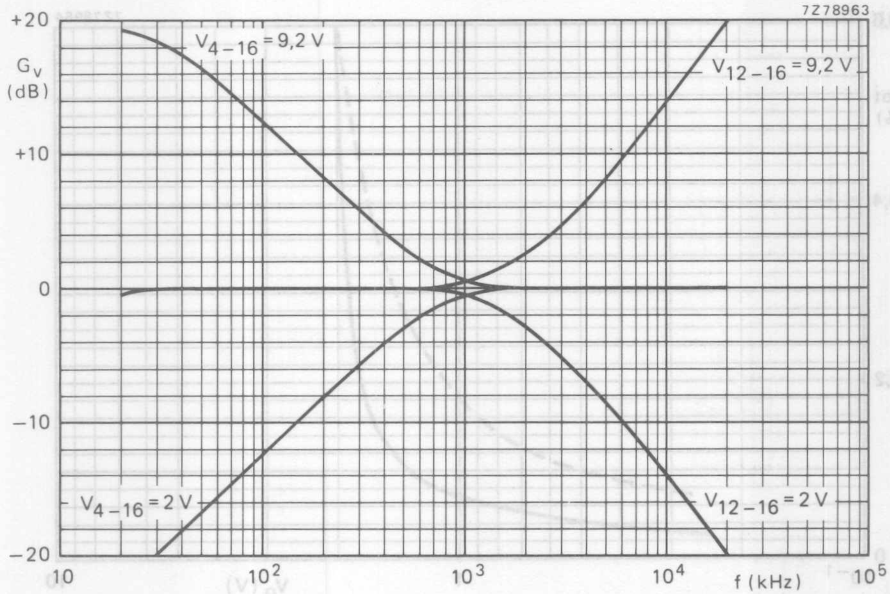



Fig. 2 Frequency response.

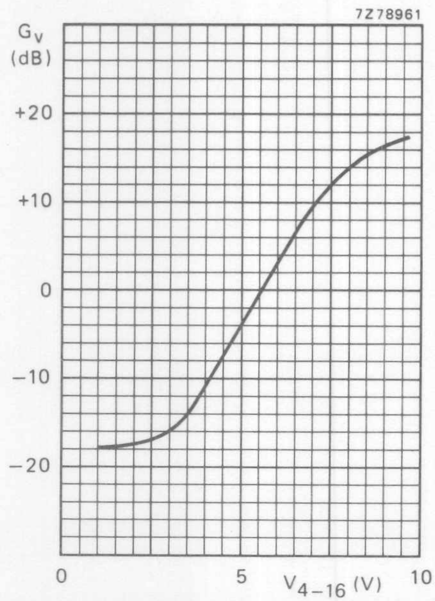



Fig. 3 Bass control curve at f = 40 Hz.

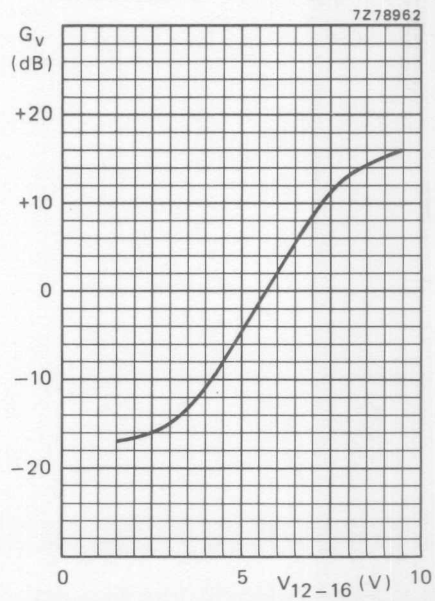



Fig. 4 Treble control curve at f = 16 kHz.

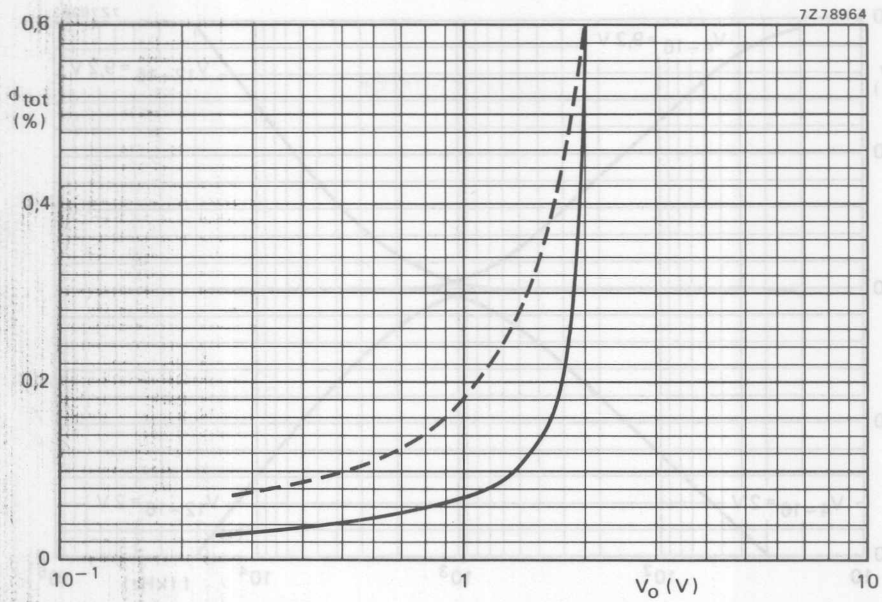
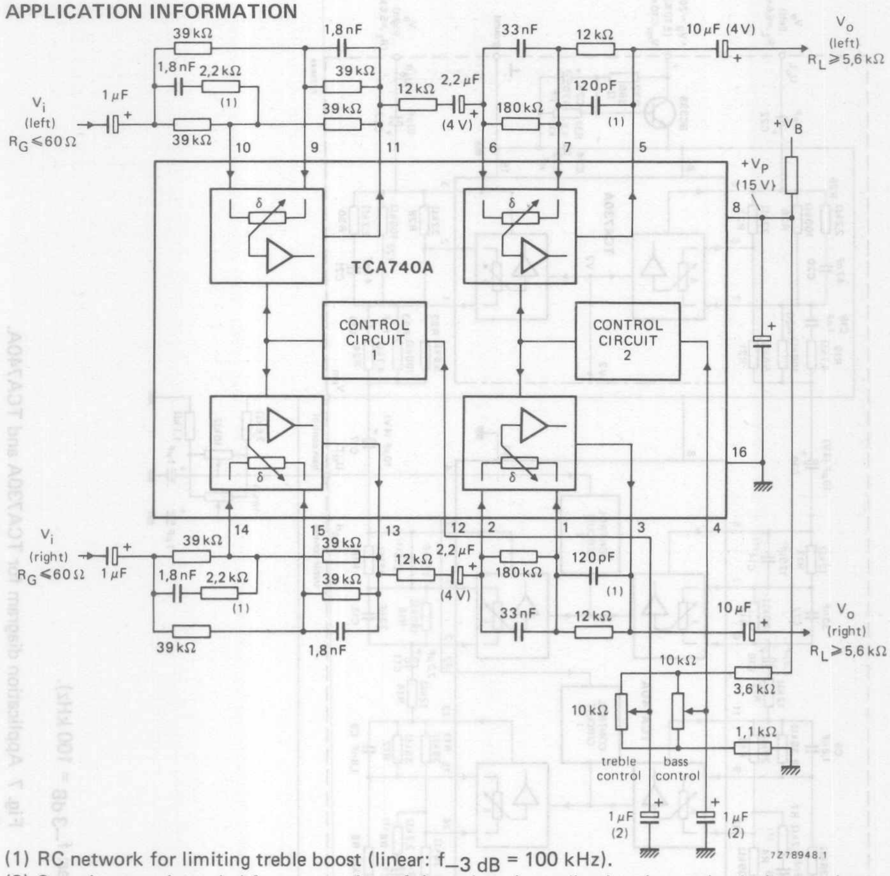



Fig. 5 Total distortion as a function of output voltage; $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V (linear, $G_{v\,tot} = 1$); ——— f = 1 kHz; – – – f = 40 Hz to 16 kHz.

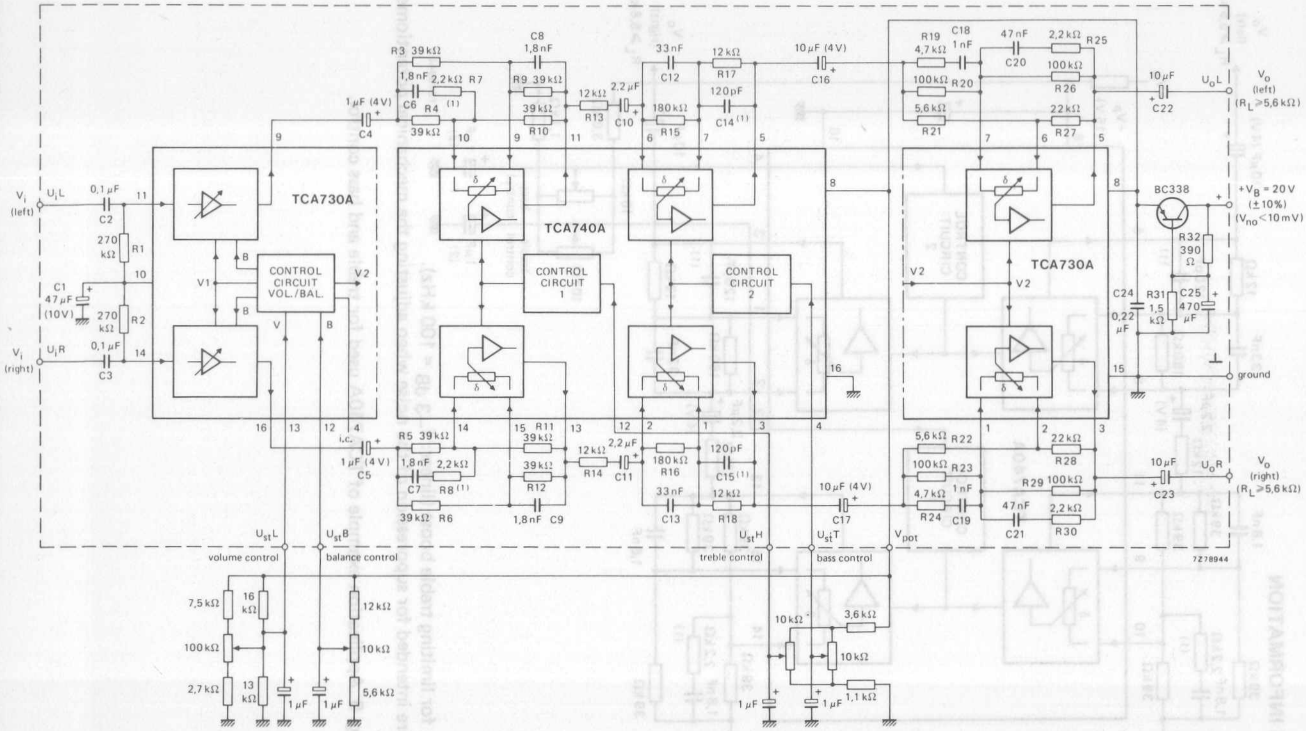
## APPLICATION INFORMATION




(1) RC network for limiting treble boost (linear: $f_{-3\text{ dB}} = 100$ kHz).

(2) Capacitors are intended for suppression of the noise when adjusting the mechanical potentiometers.

Fig. 6 Application example of TCA740A used for treble and bass control.




(1) RC network for limiting treble boost (linear: $f_{-3\,dB} = 100$ kHz).

Fig. 7 Application diagram for TCA730A and TCA740A.
For printed-circuit board see Fig. 8.

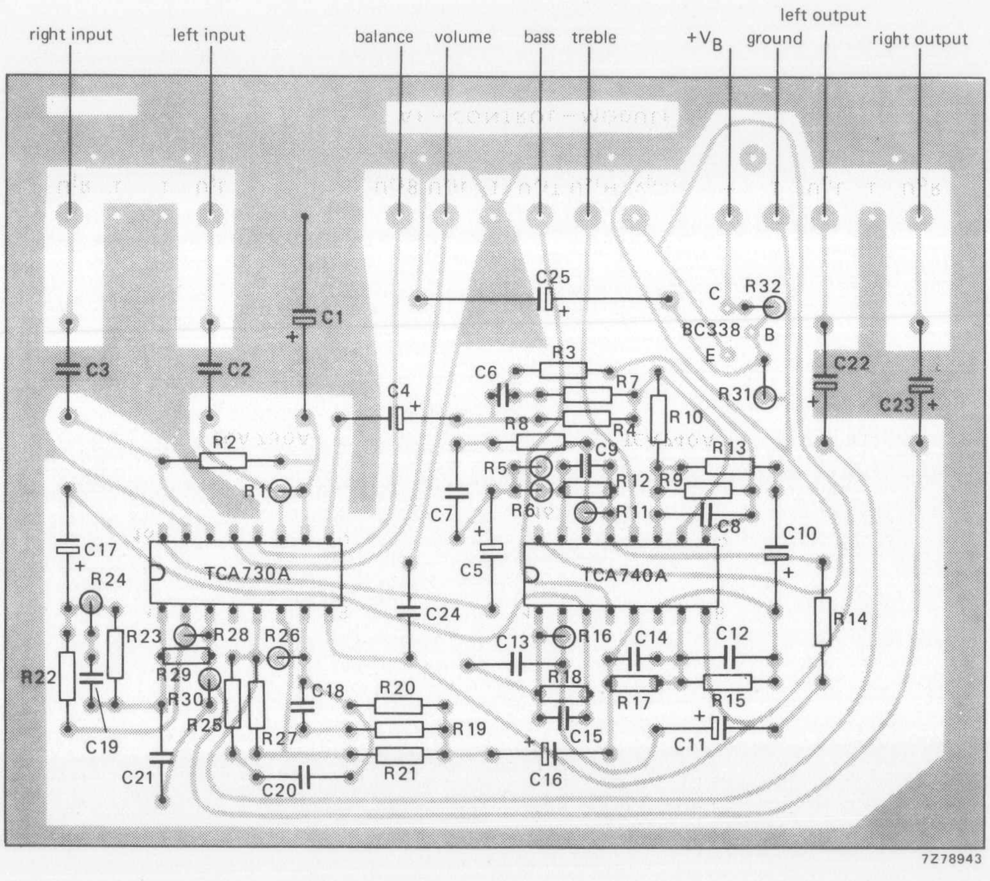



Fig. 8 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 7.

# INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

## GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

### Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ | typ. | 12 | V |
| Supply current (pin 9) | $I_P$ | typ. | 14 | mA |
| A.F. input signal handling (pin 1) (peak-to-peak value) | $V_{i(p\text{-}p)}$ | typ. | 1 | V |
| Input resistance (pin 1) | $R_i$ | min. | 35 | kΩ |
| Voltage gain ($V_{1\text{-}16}/V_{6\text{-}16}$) | $G_v$ | typ. | 0,5 | dB |
| Total harmonic distortion | THD | typ. | 0,25 | % |
| Bandwidth | B | typ. | 70 | kHz |
| Suppression pulse threshold voltage (peak value); $R_{13} = 0$ | $V_{i(tr)OM}$ | typ. | 19 | mV |
| Suppression pulse duration | $t_s$ | typ. | 27 | μs |
| Supply voltage range (pin 9) | $V_P$ | | 7,5 to 16 | V |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +80 | °C |

## PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT-38).
TDA1001BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

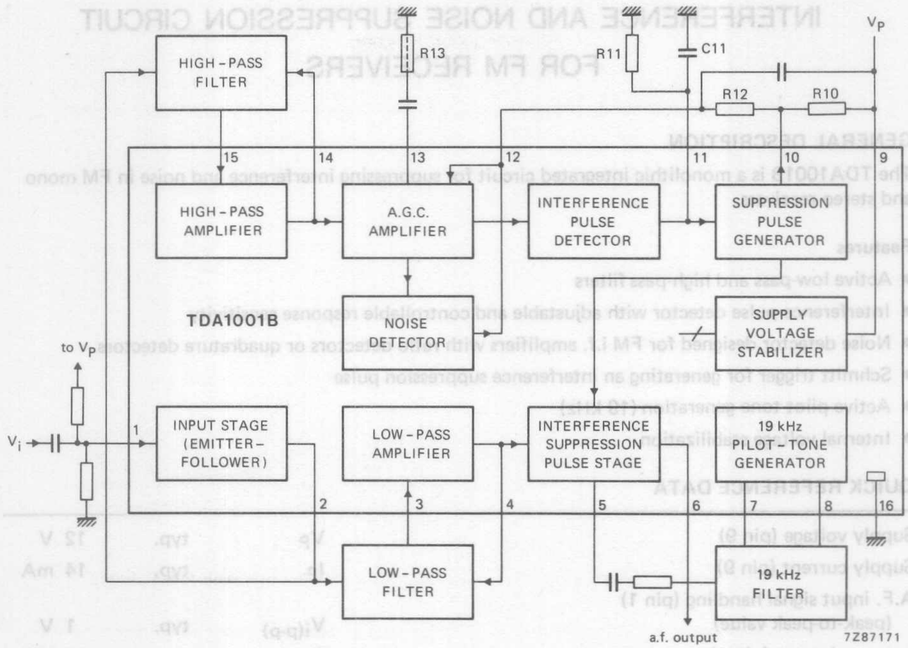



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ | max. | 18 V |
| Input voltage (pin 1) | $V_{1\text{-}16}$ | max. | $V_P$ V |
| Output current (pin 6) | $I_6$ | max. | 1 mA |
| | $-I_6$ | max. | 15 mA |
| Total power dissipation | see derating curves Fig. 2 | | |
| Storage temperature range | $T_{stg}$ | | −65 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +80 °C |

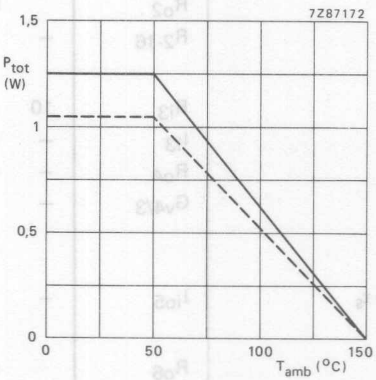



Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Input stage** | | | | | |
| Input impedance (pin 1)<br>f = 40 kHz | $\lvert Z_{i1} \rvert$ | – | 45 | – | kΩ |
| Input resistance (pin 1)<br>with pin 2 not connected | $R_{i1}$ | – | 600 | – | kΩ |
| Input bias current (pin 1)<br>$V_{1\text{-}16} = 4{,}8$ V | $I_{i1}$ | – | 6 | 15 | μA |
| Output resistance (pin 2)<br>unloaded | $R_{o2}$ | | low-ohmic | | |
| Internal emitter resistance | $R_{2\text{-}16}$ | – | 5,6 | – | kΩ |
| **Low-pass amplifier** | | | | | |
| Input resistance (pin 3) | $R_{i3}$ | 10 | – | – | MΩ |
| Input bias current (pin 3) | $I_{i3}$ | – | – | 7 | μA |
| Output resistance (pin 4) | $R_{o4}$ | – | – | 5 | Ω |
| Voltage gain ($V_4/V_3$) | $G_{v4/3}$ | – | 1,1 | – | |
| **Suppression pulse stage** | | | | | |
| Input offset current at pin 5<br>during the suppression time $t_s$ | $I_{io5}$ | – | 50 | 200 | nA |
| **Output stage** | | | | | |
| Output resistance (pin 6) | $R_{o6}$ | | low-ohmic | | |
| Internal emitter resistance | $R_{6\text{-}16}$ | – | 6 | – | kΩ |
| Current gain ($I_5/I_6$) | $G_{i5/6}$ | – | 85 | – | dB |
| **Pilot tone generation (19 kHz)** | | | | | |
| Input impedance (pin 8) | $\lvert Z_{i8} \rvert$ | – | – | 1 | Ω |
| Output impedance (pin 7)<br>pin 8 open | $\lvert Z_{o7} \rvert$ | 150 | – | – | kΩ |
| Output bias current (pin 7) | $I_{o7}$ | 0,7 | 1 | 1,3 | mA |
| Current gain ($I_7/I_8$) | $G_{i7/8}$ | – | 3 | – | |
| **High-pass amplifier** | | | | | |
| Input resistance (pin 15) | $R_{i15}$ | 10 | – | – | MΩ |
| Input bias current (pin 15) | $I_{i15}$ | – | – | 7 | μA |
| Output resistance (pin 14) | $R_{o14}$ | – | – | 5 | Ω |
| Voltage gain ($V_{14/15}$) | $G_{v14/15}$ | – | 1,4 | – | |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **A.G.C. amplifier; interference and noise detectors** | | | | | |
| Internal resistance (pins 13 and 14) | $R_{13\text{-}14}$ | 1,5 | 2,0 | 2,5 | kΩ |
| Operational threshold voltage (uncontrolled); peak value (pin 14) | | | | | |
| of the interference pulse detector | $\pm V_{14int\,m}$ | – | 15 | – | mV |
| of the noise detector | $\pm V_{14n\,m}$ | – | 6,5 | – | mV |
| Output voltage (peak value; pin 11) | $V_{11\text{-}16M}$ | 5,2 | 5,8 | 6,4 | V |
| Output control current (pin 12) (peak value) | $I_{12M}$ | 150 | 200 | 250 | μA |
| Output bias current (pin 12) | $I_{o12}$ | – | 2,5 | 6 | μA |
| Input threshold voltage for onset of control (pin 12) | $V_{12\text{-}9}$ | 360 | 425 | 500 | mV |
| ($V_{i(tr)O}$ + 3 dB) | or: | – | $0{,}66V_{BE}$ | – | mV |
| **Suppression pulse generation (Schmitt trigger)** | | | | | |
| Switching threshold (pin 11) | | | | | |
| 1: gate disabled | $V_{11\text{-}16}$ | – | 3,2 | – | V |
| 2: gate enabled | $V_{11\text{-}16}$ | – | 2,0 | – | V |
| Switching hysteresis | $\Delta V_{11\text{-}16}$ | – | 1,2 | – | V |
| Input offset current (pin 11) | $I_{io11}$ | – | – | 100 | nA |
| Output current (pin 10) gate disabled; peak value | $I_{o10M}$ | 0,6 | 1 | 1,4 | mA |
| Reverse output current (pin 10) | $I_{R10}$ | – | – | 2 | μA |
| Sensitivity (pin 10) | $V_{10\text{-}16}$ | 2,5 | – | – | V |

## APPLICATION INFORMATION

$V_P$ = 12 V; $T_{amb}$ = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage range (pin 9) | $V_P$ | 7,5 | 12 | 16 | V |
| Quiescent supply current (pin 9) | $I_P$ | 10 | 14 | 18 | mA |
| **Signal path** | | | | | |
| D.C. input voltage (pin 1) | $V_{1\text{-}16}$ | — | 4,5 | — | V |
| Input impedance (pin 1); f = 40 kHz | $\lvert Z_{i1} \rvert$ | 35 | — | — | kΩ |
| D.C. output voltage (pin 6) | $V_{6\text{-}16}$ | 2,4 | 2,8 | — | V |
| Output resistance (pin 6) | $R_{o6}$ | | low-ohmic | | |
| Voltage gain ($V_6/V_1$) | $G_{v6/1}$ | 0 | 0,5 | 1 | dB |
| −3 dB point of low-pass filter | $f_{(-3dB)}$ | — | 70 | | kHz |
| Sensitivity for THD < 0,5% (peak-to-peak value) | $V_{i(p\text{-}p)}$ | 1,2 | 1,8 | — | V |
| Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value) | $V_{6\text{-}16(p\text{-}p)}$ | — | — | 3 | mV |
| Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; $f_r$ = 400 Hz | $\alpha_{int}$ | 20 | 30 | — | dB |
| **Interference processing** | | | | | |
| Input signal at pin 1; output signal at pin 10 | | | | | |
| Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1 | | | | | |
| measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9}$ > 1 V | | | | | |
| at R13 = 0 Ω | $V_{i(tr)rms}$ | 8 | 11 | 14 | mV |
| at R13 = 2,7 kΩ | $V_{i(tr)rms}$ | 18 | 28,5 | 40 | mV |
| voltage difference for safe triggering/non-triggering (r.m.s. value) | $\Delta V_{i(rms)}$ | — | 1 | — | mV |
| measured with interference pulses f = 400 Hz (see Fig. 3); peak value | | | | | |
| at R13 = 0 Ω | $V_{i(tr)M}$ | — | 19 | — | mV |
| at R13 = 2,7 kΩ | $V_{i(tr)M}$ | — | 45 | — | mV |
| Suppression pulse duration (note 2) | $t_s$ | 24 | 27 | 30 | μs |

| parameters | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Noise threshold feedback control** (notes 1 and 3) | | | | | |
| Noise input voltage (r.m.s. value) f = 120 kHz sinewave | | | | | |
| for $V_{12\text{-}9}$ = 300 mV | | | | | |
| at R13 = 0 Ω | $V_{ni(rms)}$ | 2,3 | 3,3 | 4,3 | mV |
| at R13 = 2,7 kΩ | $V_{ni(rms)}$ | – | 8,2 | – | mV |
| for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB) | | | | | |
| at R13 = 0 Ω | $V_{ni(rms)}$ | – | 7,3 | – | mV |
| at R13 = 2,7 kΩ | $V_{ni(rms)}$ | – | 16,5 | – | mV |
| for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB) | | | | | |
| at R13 = 0 Ω | $V_{ni(rms)}$ | 33 | 45 | 57 | mV |
| at R13 = 2,7 kΩ | $V_{ni(rms)}$ | – | 107 | | mV |
| Amplification control voltage by interference intensity (note 4) | | | | | |
| $V_{i(rms)}$ = 50 mV; f = 19 kHz; | | | | | |
| $V_{i(tr)M}$ = 300 mV; r.m.s. value | | | | | |
| at repetition frequency $f_r$ = 1 kHz | $V_{o6(rms)}$ | 49 | – | 56 | mV |
| at repetition frequency $f_r$ = 16 kHz | $V_{o6(rms)}$ | 45 | – | 65 | mV |

**Notes to application information**

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a de-emphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

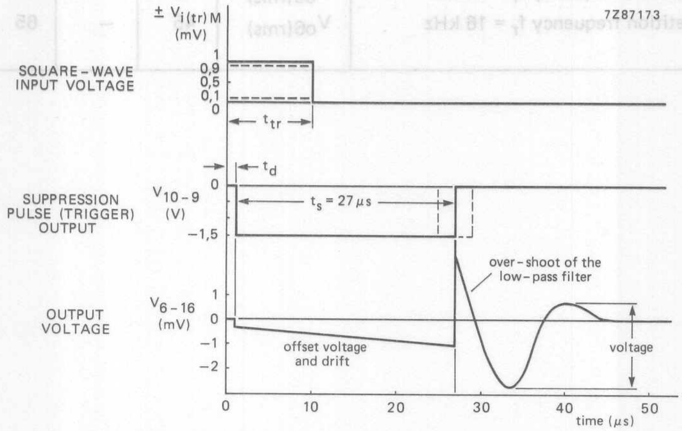



Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of $t_{tr} = 10\ \mu s$ and with rise and fall times $t_r = t_f = 10$ ns.

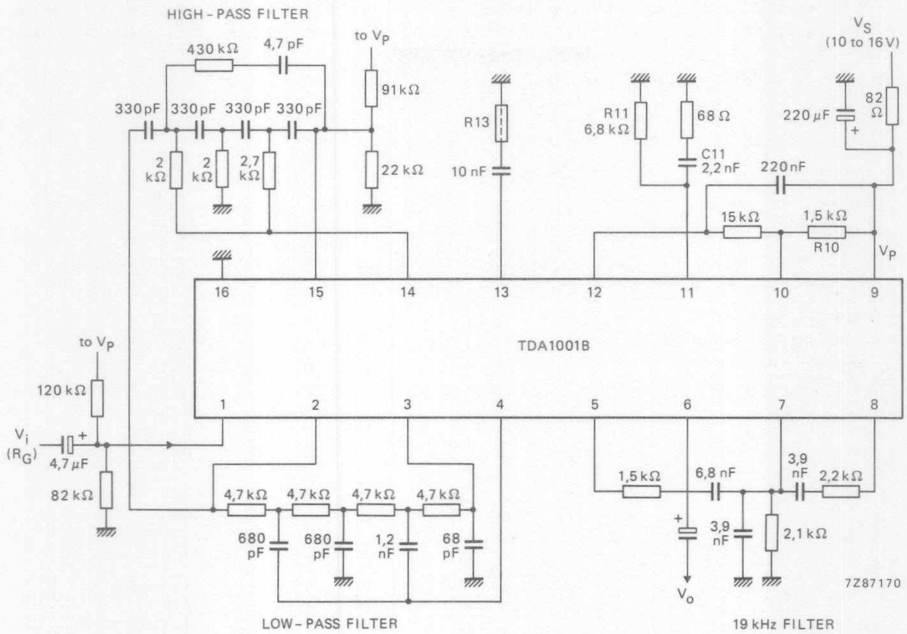



Fig. 4 Application circuit diagram.

# RECORDING AND PLAYBACK AMPLIFIER

This integrated circuit incorporates all amplifier circuits necessary for the record/playback functions, with the exception of the audio power output amplifier. It comprises:
- a preamplifier for microphone or playback,
- a recording amplifier with automatic level control,
- a dynamic limiter with a short limiting time.

Compared to its predecessor TDA1002, this type features an improved automatic level control circuit; the control range has been enlarged from 40 to 55 dB and the spread in control characteristic has been reduced to less than 2 dB.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 4 to 12 | V |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 125 | °C |
| Total quiescent current ($V_P$ = 9 V) | $I_{tot}$ | typ. | 15 | mA |
| **Preamplifier** | | | | |
| Input impedance (pin 1) | $\|Z_i\|$ | typ. | 16 | kΩ |
| Open loop gain | $G_o$ | typ. | 70 | dB |
| Clipping level (pin 4); $V_P$ = 9 V; r.m.s. value | $V_{4\text{-}5(rms)}$ | typ. | 2 | V |
| Equivalent noise input voltage $R_S$ = 500 Ω; B = 300 Hz to 15 kHz | $V_{n(rms)}$ | < | 0,75 | μV |
| **Recording amplifier** | | | | |
| Input impedance (pin 8) | $\|Z_i\|$ | typ. | 40 | kΩ |
| Open loop gain | $G_o$ | typ. | 80 | dB |
| Clipping level (pin 9); $V_P$ = 9 V; r.m.s. value | $V_{9\text{-}10(rms)}$ | typ. | 2 | V |
| **Automatic Level Control (A.L.C.)** | | | | |
| Input impedance (pin 6) | | | | |
| at low signal level at pin 8 | $\|Z_i\|$ | typ. | 250 | kΩ |
| at high signal level pin 8 | $\|Z_i\|$ | typ. | 25 | Ω |
| Control voltage | | | | |
| $V_{4\text{-}5}$ = 10 mV; f = 1 kHz; $V_P$ = 9 V | $V_{9\text{-}10}$ | typ. | 250 | mV |
| $V_{4\text{-}5}$ = 1000 mV; f = 1 kHz; $V_P$ = 9 V | $V_{9\text{-}10}$ | typ. | 750 | mV |
| Limiting time (Fig. 12) | $t_l$ | typ. | 10 | ms |
| Level setting time (Fig. 12) | $t_s$ | typ. | 4 | s |
| Recovery time (Fig. 13) | $t_r$ | typ. | 35 | s |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

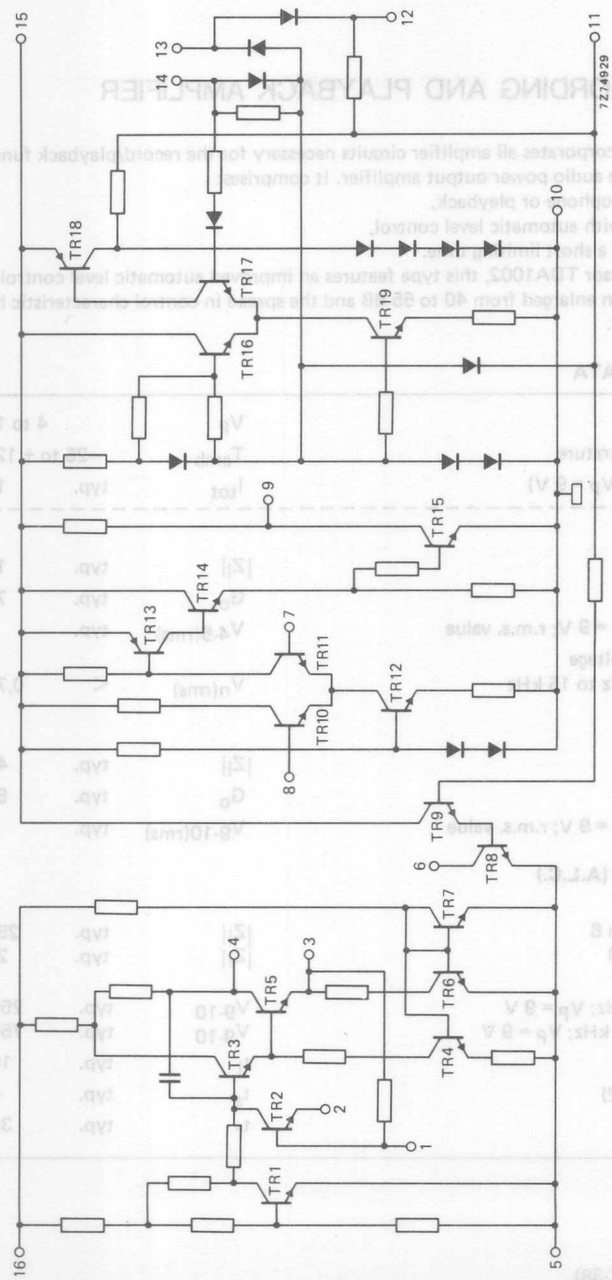



Fig. 1 Circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage preamplifier | $V_{16\text{-}5}$ | max. | 12 V |
| Supply voltage recording amplifier | $V_{15\text{-}10}$ | max. | 12 V |
| Total power dissipation | | see derating curve Fig. 2 | |
| Storage temperature | $T_{stg}$ | | −65 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 125 °C |

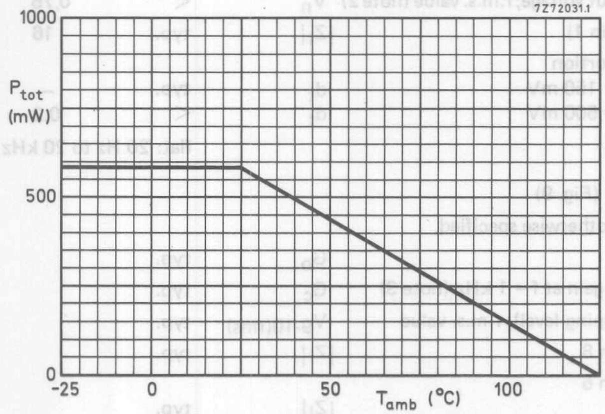



Fig. 2 Power dissipation derating curve.

## D.C. CHARACTERISTICS

$T_{amb}$ = 25 °C unless otherwise specified.

| | | | |
|---|---|---|---|
| Supply voltage recording amplifier | $V_{15\text{-}10}$ | | 4 to 12 V |
| Supply voltage preamplifier | $V_{16\text{-}5}$ | | 4 to 12 V |
| Quiescent current rec. amplifier; $V_P$ = 9 V | $I_{15}$ | typ. | 10 mA |
| Quiescent current preamplifier; $V_P$ = 9 V | $I_{16}$ | typ. | 5 mA |
| Output voltage recording amplifier | $V_{9\text{-}10}$ | typ. | ½ $V_P$ V |
| Output voltage preamplifier | $V_{4\text{-}5}$ | typ. | ½ $V_P$−0,35 V |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 9 V unless otherwise specified.

| **Preamplifier** (note 1) | | | recording | playback |
|---|---|---|---|---|
| Open loop voltage gain | $G_o$ | typ. | 70 | 70 dB |
| Closed loop voltage gain at f = 1 kHz | $G_c$ | typ. | 38 | 45 dB |
| Output voltage (clipping level); r.m.s. value | $V_{4\text{-}5(rms)}$ | typ. | 2 | 2 V |
| Equivalent noise input voltage; r.m.s. value (note 2) | $V_n$ | < | 0,75 | 0,75 μV |
| Input impedance (pin 1) | $\lvert Z_i \rvert$ | typ. | 16 | 16 kΩ |
| Total harmonic distortion | | | | |
| f = 1 kHz; $V_{4\text{-}5}$ = 150 mV | $d_t$ | typ. | – | 0,12 % |
| f = 1 kHz; $V_{4\text{-}5}$ = 500 mV | $d_t$ | < | 0,2 | – |
| Amplitude response | | flat: 20 Hz to 20 kHz | | see Fig. 7 |

| **Recording amplifier** (Fig. 9) | | | |
|---|---|---|---|
| with A.L.C.; unless otherwise specified. | | | |
| Open loop gain | $G_o$ | typ. | 80 dB |
| Closed loop voltage gain at f = 1 kHz (note 3) | $G_c$ | typ. | 49 dB |
| Output voltage (clipping level); r.m.s. value | $V_{9\text{-}10(rms)}$ | typ. | 2 V |
| Input impedance pin 8 | $\lvert Z_i \rvert$ | typ. | 40 kΩ |
| Input impedance pin 6 | | | |
| low signal levels | $\lvert Z_i \rvert$ | typ. | 250 kΩ |
| high signal levels | $\lvert Z_i \rvert$ | typ. | 25 Ω |
| Total harmonic distortion | | see Fig. 11 | |
| Amplitude response (note 3) | | see Fig. 10 | |

| **Automatic level control** (see Fig. 8) | | | |
|---|---|---|---|
| $V_{4\text{-}5}$ = 10 mV; f = 1 kHz | $V_{9\text{-}10}$ | typ. | 250 mV |
| $V_{4\text{-}5}$ = 100 mV; f = 1 kHz | $V_{9\text{-}10}$ | typ. | 450 mV |
| $V_{4\text{-}5}$ = 1000 mV; f = 1 kHz | $V_{9\text{-}10}$ | typ. | 750 mV |
| $V_{4\text{-}5}$ = 2000 mV; f = 1 kHz | $V_{9\text{-}10}$ | typ. | 880 mV |
| Limiting time (see Fig. 12) | $t_l$ | typ. | 10 ms |
| Level setting time (see Fig. 12) | $t_s$ | typ. | 4 s |
| Recovery time (see Fig. 13) | $t_r$ | typ. | 35 s |

Notes

1. For recording see Fig. 3; for playback see Fig. 5.
2. $R_S$ = 500 Ω; bandwidth = 300 Hz to 15 kHz.
3. Pin 6 not connected to pin 8.

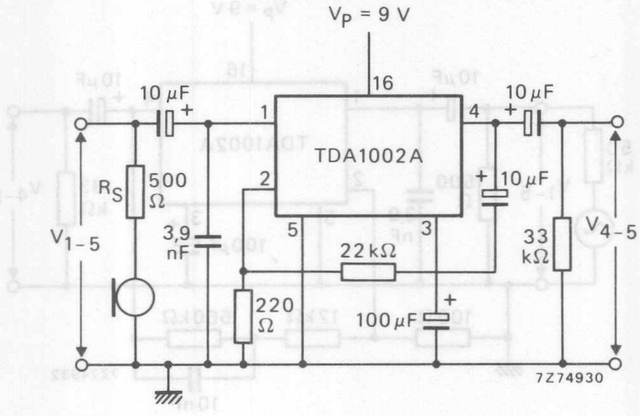



Fig. 3 Preamplifier used as microphone amplifier.

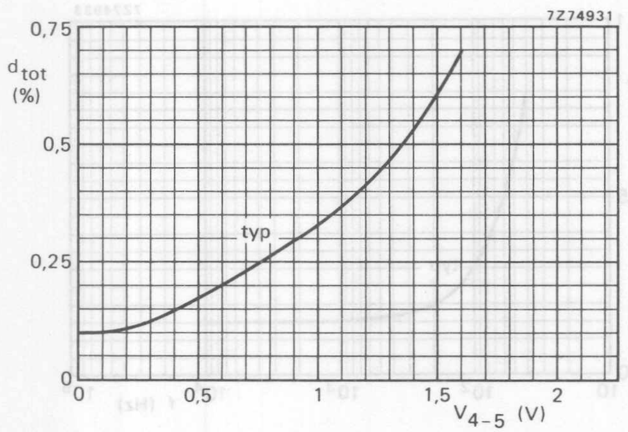



Fig. 4 Total harmonic distortion of preamplifier used for recording.

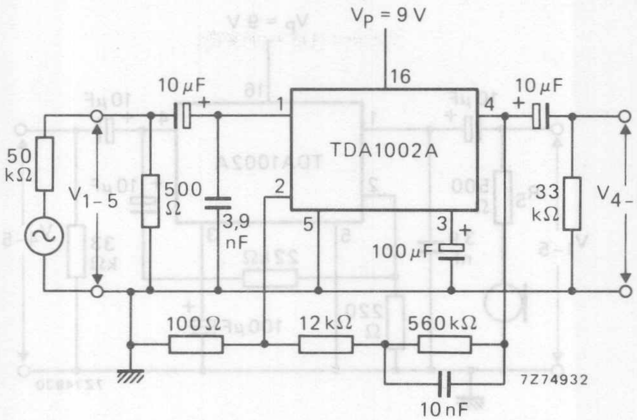



Fig. 5 Preamplifier used for playback.

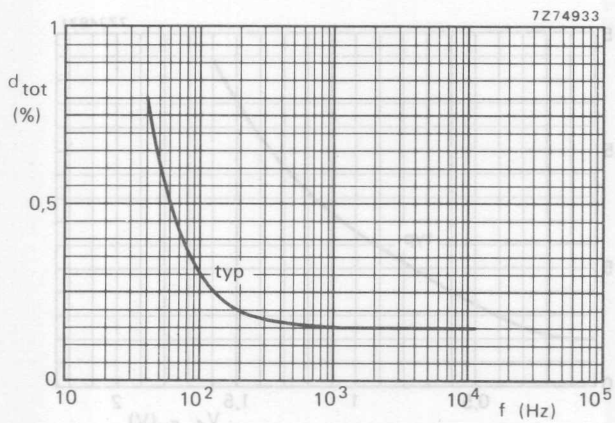



Fig. 6 Total harmonic distortion of preamplifier used for playback at $V_{4\text{-}5}$ = 150 mV.

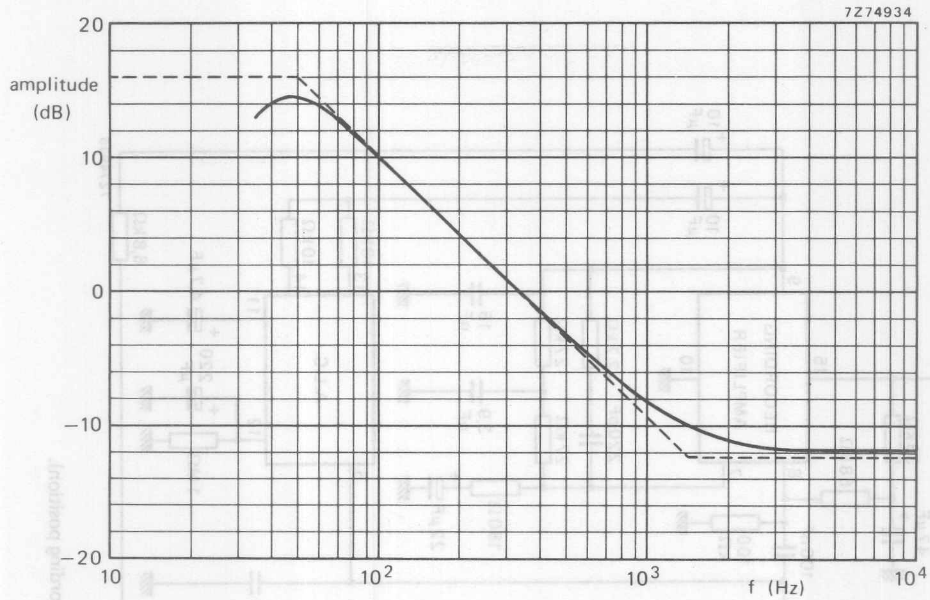



Fig. 7 Amplitude response of preamplifier used for playback; typical values.
0 dB = input voltage of 0,3 mV at f = 333 Hz. Dotted line according to DIN 45513.

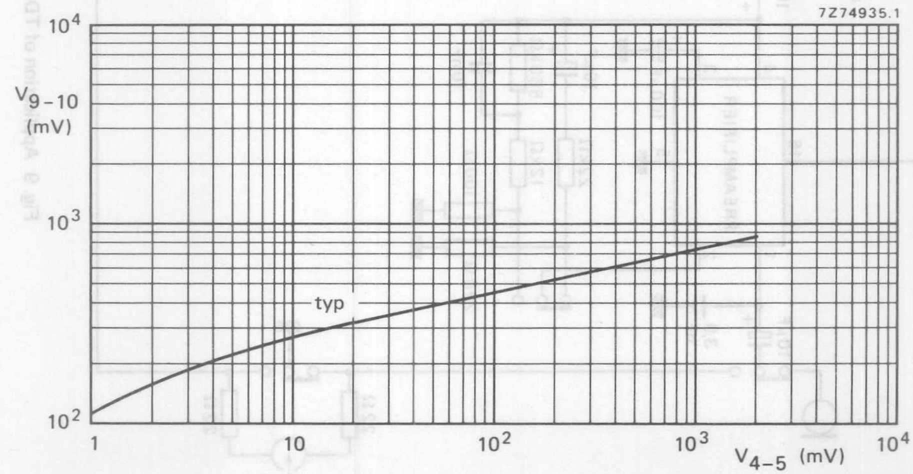



Fig. 8 Automatic level control; for circuitry see Fig. 9; f = 1 kHz.

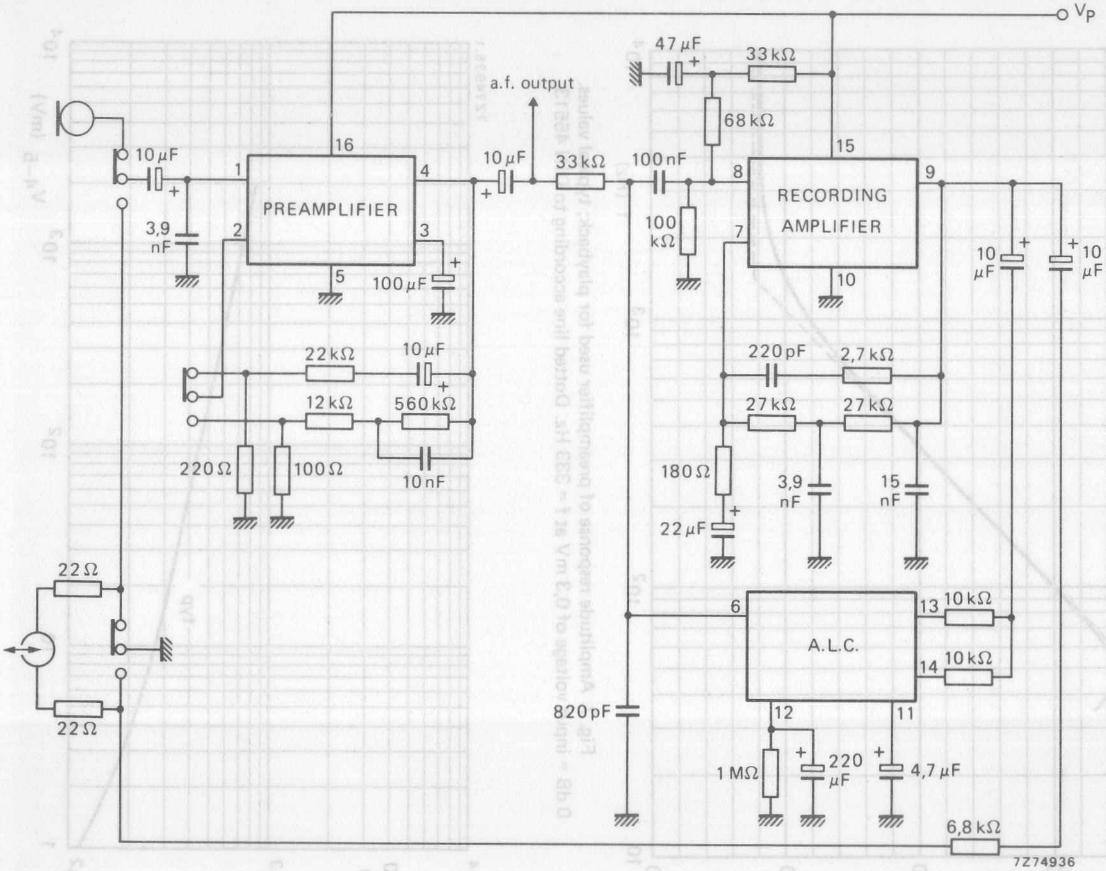



Fig. 9 Application of TDA1002A (recording position).

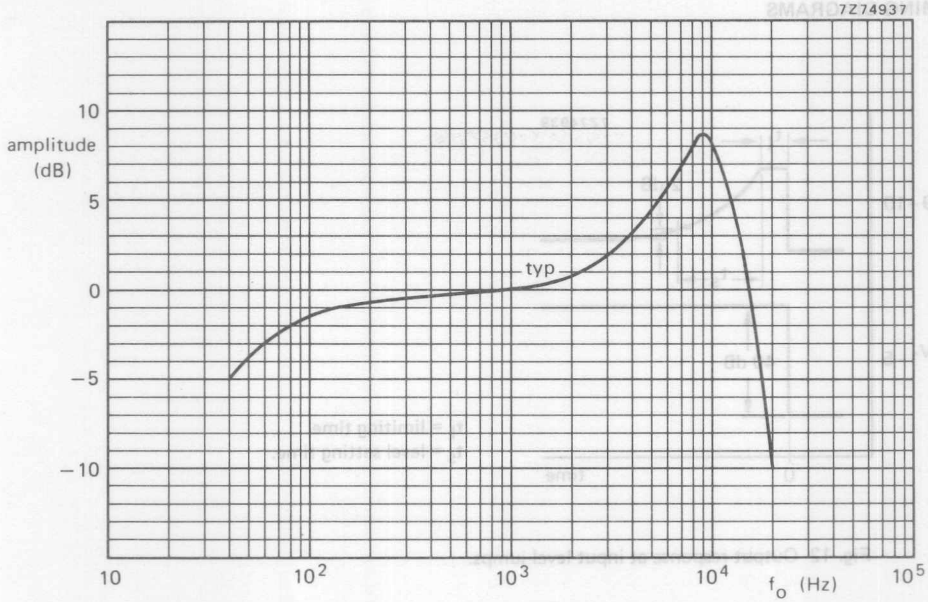



Fig. 10 Amplitude response of recording amplifier (A.L.C. not connected).

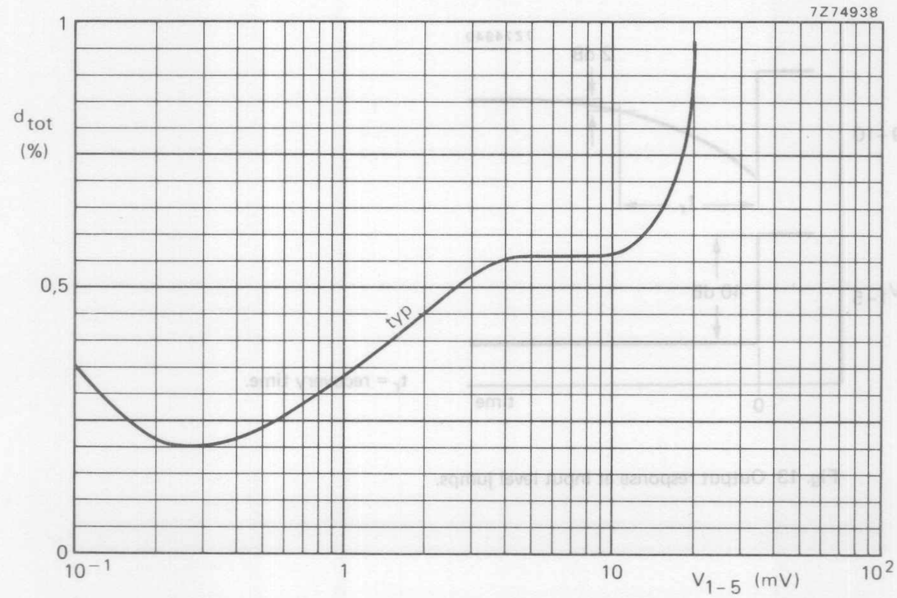



Fig. 11 Total harmonic distortion recording amplifier with A.L.C.; f = 1 kHz.

TIMING DIAGRAMS

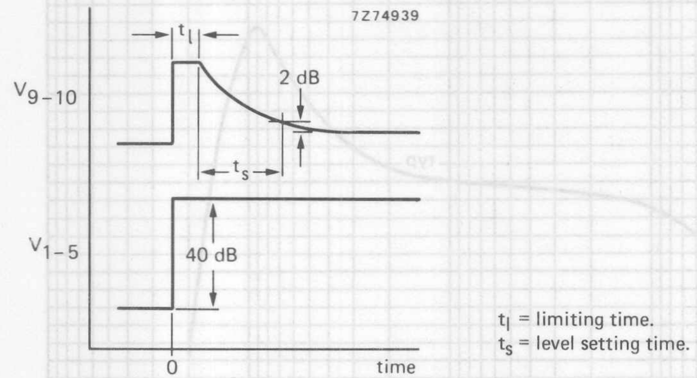



Fig. 12 Output response at input level jumps.

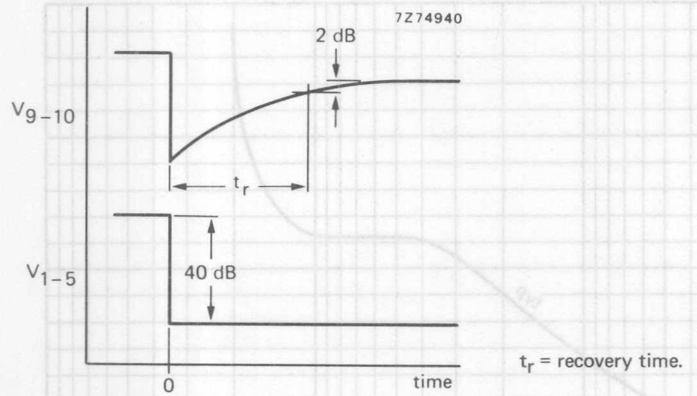



Fig. 13 Output response at input level jumps.

# FREQUENCY MULTIPLEX PLL STEREO DECODER

The TDA1005A is a high quality PLL stereo decoder based on the frequency-division multiplex (f.d.m.) principle, performing:

- excellent ACI (Adjacent Channel Interference) and SCA (Storecast) rejection
- very low BFC (Beat-Frequency Components) distortion in the higher frequency region

The circuit incorporates the following features:

- with simplified peripheral circuitry the circuit can perform as a time-division multiplex (t.d.m.) decoder, for use in economic medium and low-class apparatus
- for car radios: operation at a supply voltage of 8 V
- extra pin for smooth mono/stereo take-over without "clicks"
- automatic mono/stereo switching (minimum switching level is 16 mV), controlled by both pilot signal and field strength level
- low distortion in the loop resonance frequency region (≈ 300 Hz; THD = 0,2% typ.)
- external adjustment for obtaining optimum channel separation in the complete receiver
- internal amplification: t.d.m., 7 dB; f.d.m., 10 dB
- driver for stereo indicator lamp
- externally switchable: VCO-off or mono condition
- guaranteed VCO capture range (> 3,5% or 2,7 kHz)

## QUICK REFERENCE DATA

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range | $V_{8\text{-}16}$ | | 8 to 18 | | V |
| Supply voltage | $V_{8\text{-}16}$ | typ. | | 15 | V |
| Ambient temperature | $T_{amb}$ | typ. | | 25 | °C |
| Measured at $V_{i(p\text{-}p)}$ = 1 V (MUX signal with 8% pilot) | | | t.d.m. | f.d.m. | |
| Channel separation at f = 1 kHz | $\alpha$ | typ. | 50 | 55 | dB |
| Carrier suppression | | | | | |
| at f = 19 kHz | $\alpha_{19}$ | typ. | 36 | 36 | dB |
| at f = 38 kHz | $\alpha_{38}$ | typ. | 45 | 40 | dB |
| at f = 76 kHz | $\alpha_{76}$ | typ. | 80 | 75 | dB |
| ACI rejection at f = 114 kHz | $\alpha_{114}$ | typ. | 52 | 70 | dB |
| SCA rejection at f = 67 kHz | $\alpha_{67}$ | typ. | 85 | 90 | dB |
| VCO capture range | | > | 3,5 | 3,5 | % |
| Total harmonic distortion | | | | | |
| $f_m$ = 1 kHz | THD | typ. | 0,2 | 0,1 | % |
| $f_m$ = 300 Hz to 10 kHz | THD | typ. | 0,2 | 0,1 | % |
| BFC suppression | $d_{BFC}$ | > | 40 | 60 | dB |

## PACKAGE OUTLINES

TDA1005A ; 16-lead DIL; plastic (SOT-38).
TDA1005AT; 16-lead flat pack; plastic (SO-16; SOT-109A).

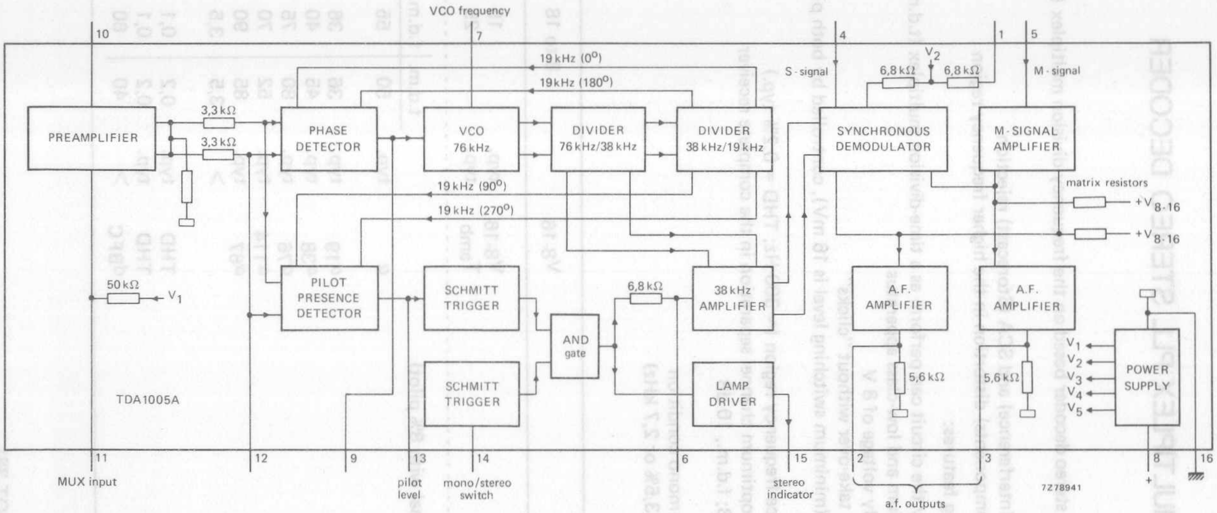



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{8\text{-}16}$ | max. | 18 V |
| Indicator lamp voltage | $V_{15\text{-}16}$ | max. | 22 V |
| Mono/stereo switching voltage | $V_{14\text{-}16}$ | max. | 4 V |
| Indicator lamp current | $I_{15}$ | max. | 100 mA |
| Indicator lamp turn-on current (peak value) | $I_{15M}$ | max. | 200 mA |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | −55 to + 150 °C | |
| Operating ambient temperature (see also Fig. 2) | $T_{amb}$ | −25 to + 150 °C | |

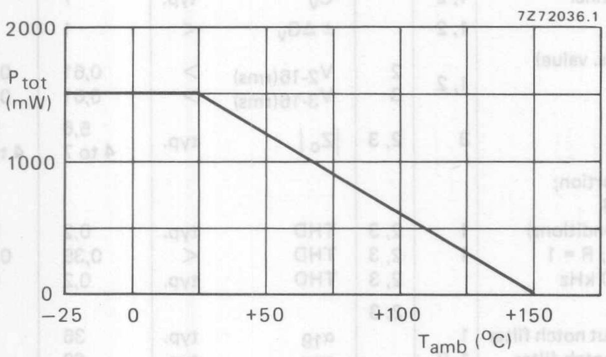



Fig. 2 Power derating curve.

## A.C. CHARACTERISTICS and APPLICATION INFORMATION

$T_{amb}$ = 25 °C; $V_{8\text{-}16}$ = 15 V (unless otherwise specified); see also Fig. 7 and Fig. 10.

| | note | pin | parameter | | t.d.m. | f.d.m. | unit |
|---|---|---|---|---|---|---|---|
| Channel separation see Figs 23 and 24 | 1, 2 | 2, 3 | $\alpha$ | > | 40 | 45 | dB |
| | | | | typ. | 50 | 55 | dB |
| F.M.−I.F. roll-off correction range | 1, 2 | | | | 48 to 72 | | kHz |
| Input MUX-voltage; L = 1; R = 1 for THD < 0,35% | 1, 2 | 11 | $V_{i(p\text{-}p)}$ | typ. | 1 | 1 | V |
| Input impedance | | 11 | $\lvert Z_i \rvert$ | > | 35 | 35 | kΩ |
| | | | | typ. | 50 | 50 | kΩ |
| Voltage gain per channel | 1, 2 | | $G_v$ | typ. | 7 | 10 | dB |
| Channel balance | 1, 2 | | $\pm \Delta G_v$ | < | 1 | 1 | dB |
| Output voltage (r.m.s. value) L = 1; R = 1 | 1, 2 | 2 | $V_{2\text{-}16(rms)}$ | > | 0,61 | 0,97 | V |
| | | 3 | $V_{3\text{-}16(rms)}$ | > | 0,61 | 0,97 | V |
| Output impedance | 3 | 2, 3 | $\lvert Z_o \rvert$ | typ. | 5,6 | 5,6 | kΩ |
| | | | | | 4 to 7 | 4 to 7 | kΩ |
| Total harmonic distortion; see Figs 25 and 26 | | | | | | | |
| $f_m$ = 1 kHz (all conditions) | 1 | 2, 3 | THD | typ. | 0,2 | 0,1 | % |
| $f_m$ = 1 kHz; L = 1; R = 1 | 1 | 2, 3 | THD | < | 0,35 | 0,35 | % |
| $f_m$ = 300 Hz to 10 kHz | | 2, 3 | THD | typ. | 0,2 | 0,1 | % |
| Carrier suppression | | 2, 3 | | | | | |
| f = 19 kHz; without notch filter | 1 | | $\alpha_{19}$ | typ. | 36 | 36 | dB |
| f = 19 kHz; with notch filter | 1, 9 | | $\alpha_{19}$ | typ. | 60 | 60 | dB |
| f = 38 kHz; without notch filter | 1 | | $\alpha_{38}$ | > | 40 | 38 | dB |
| f = 38 kHz; with notch filter | 1, 9 | | $\alpha_{38}$ | > | 72 | 72 | dB |
| f = 57 kHz; without notch filter | 1 | | $\alpha_{57}$ | typ. | 46 | 56 | dB |
| f = 57 kHz; with notch filter | 1, 9 | | $\alpha_{57}$ | typ. | 59 | 61 | dB |
| f = 76 kHz; without notch filter | 1 | | $\alpha_{76}$ | typ. | 80 | 75 | dB |
| ACI rejection | | 2, 3 | | | | | |
| at f = 114 kHz | 4 | | $\alpha_{114}$ | typ. | 52 | 70 | dB |
| at f = 190 kHz | 4 | | $\alpha_{190}$ | typ. | 55 | 74 | dB |
| SCA rejection at f = 67 kHz | 5 | 2, 3 | $\alpha_{67}$ | typ. | 85 | 90 | dB |
| Ripple rejection; f = 100 Hz; $V_{8\text{-}16(rms)}$ = 200 mV | | | RR | > | 40 | 40 | dB |
| | | | | typ. | 50 | 50 | dB |

| | note | pin | parameter | | t.d.m. | f.d.m. | unit |
|---|---|---|---|---|---|---|---|
| VCO; adjustable with $R_{7\text{-}16}$ | | | | | | | |
| nominal frequency | 6 | | $f_{VCO}$ | typ. | 76 | 76 | kHz |
| capture range (deviation from 76 kHz centre frequency) | | | | | | | |
| 19 kHz pilot signal of 32 mV | 6 | | | > | 3,5 | 3,5 | % |
| temperature coefficient | | | | | | | |
| uncompensated | 6 | | $-TC$ | typ. | $450.10^{-6}$ | $450.10^{-6}$ | $K^{-1}$ |
| compensated | 6 | | $\pm TC$ | typ. | $200.10^{-6}$ | $200.10^{-6}$ | $K^{-1}$ |
| Stereo/mono switch | | | | | | | |
| when equal to 19 kHz pilot-tone threshold voltage; adjustable with $R_{13\text{-}8}$ | 7 | 11 | $V_i$ | | 10 to 100 | 10 to 100 | mV |
| when equal to threshold voltage at $R_{13\text{-}8}$ = 620 kΩ | | | | | | | |
| for switching to stereo | | 11 | $V_i$ | | 7 to 16 | 7 to 16 | mV |
| for switching to mono | | 11 | $V_i$ | < | 5 | 5 | mV |
| hysteresis | 8 | 11 | $\Delta V_i$ | typ. | 2,5 | 2,5 | dB |
| Smooth take-over circuit | | | | | | | |
| full mono | 8 | 6 | $V_{6\text{-}16}$ | < | 0,65 | 0,65 | V |
| full stereo | 8 | 6 | $V_{6\text{-}16}$ | > | 1,3 | 1,3 | V |

Notes
1. $V_{i(p\text{-}p)}$ = 1 V (MUX signal with 8% pilot level).
2. $f_m$ = 1 kHz.
3. At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.
4. Measured with a composite input signal: L = R; $f_m$ = 1 kHz; 90% M-signal; 9% pilot signal; 1% spurious signal of 110 kHz (for $\alpha_{114}$) or 186 kHz (for $\alpha_{190}$).
   ACI suppression is defined as: $20 \log \frac{V_o \text{ (at 4 kHz)}}{V_o \text{ (at 1 kHz)}}$.
5. Measured with a composite input signal: L = R; $f_m$ = 1 kHz; 80% S-signal; 9% pilot signal; 10% SCA carrier (67 kHz); $d_{13} = 20 \log \frac{V_o \text{ (at 9 kHz)}}{V_o \text{ (at 1 kHz)}}$.
6. See also Figs 7 and 10; compensated with RC network on pin 7.
7. Adjustable with $R_{13\text{-}8}$; see also Fig. 28; for field strength dependent input (pin 14) see next page.
8. $\Delta V_i = 20 \log \frac{V_{11\text{-}16} \text{ (mono/stereo)}}{V_{11\text{-}16} \text{ (stereo/mono)}}$.
   For additional circuitry on pin 6 see Figs 7 and 10; for graph see Fig. 29.
9. For example of notch filter see Fig. 6.

## D.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_{8-16}$ = 15 V (unless otherwise specified)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{8-16}$ | | 8 to 18 V * |
| Total current (except indicator lamp) | $I_8$ | typ. | 21 mA |
| Power dissipation (operating) | | | |
| at lamp current $I_{15}$ = 100 mA; $V_{8-16}$ = 18 V | $P_{tot}$ | < | 570 mW |
| Saturation voltage of lamp driver | | | |
| at $I_{15}$ = 100 mA | $V_{15-16}$ | typ. | 0,9 V |
| Maximum lamp driver voltage | $V_{15-16}$ | < | 22 V |
| Switching voltage | | | |
| to mono | $V_{14-16}$ | > | 1,2 V ** |
| to stereo | $V_{14-16}$ | < | 0,65 V |
| hysteresis | $V_{14-16}$ | typ. | 0,2 V |

## APPLICATION NOTES

**1. Switching-off the VCO**

If the internal gain is used with A.M. reception, the VCO can be switched off by connecting pin 9 via a 100 kΩ resistor to ground (no h.f. signal on the leads), or connecting pin 7 to ground.

**2. Mono button**

The decoder can be switched to the mono position by connecting pin 12 to ground. The VCO then remains operational so this possibility cannot be used with A.M. reception.

**3. Economic periphery**

a. For a fixed stereo switching level of ⩽ 16 mV a resistor of 620 kΩ can be connected between pin 13 and positive supply (+) instead of a potentiometer in series with a resistor.
b. The 10 kΩ resistor connected in parallel with the stereo indicator lamp can be omitted, however, some TDA1005A circuits will switch to mono during lamp failure.
c. The 10 μF capacitor in series with a 1 kΩ resistor at pin 9 can be decreased to a 1 μF capacitor, bearing in mind that the distortion will increase, especially around loop resonance.
d. A MUX-input filter is not needed, if i.f. roll-off starts at a frequency of 62 kHz.

**4. Printed-circuit boards**

For both the f.d.m. and t.d.m. stereo decoder circuits a printed-circuit board layout is given as an example (Figs 8 and 11). Also for an active filter, which is mainly used with a t.d.m. decoder, a printed-circuit board layout is given in Fig. 4.

**5. Notch filter**

If attention has to be paid for suppression of the 57 kHz signal (T.W.S. = Traffic Warning System) and the 19 kHz signal, an input filter can be used as given in Fig. 6.

* At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.

** Maximum voltage for safe operation: $V_{14-16}$ < 4 V.

## APPLICATION INFORMATION

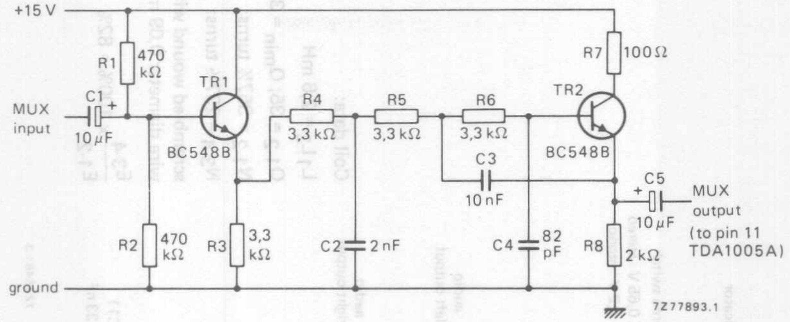



Fig. 3 Active filter circuit diagram.

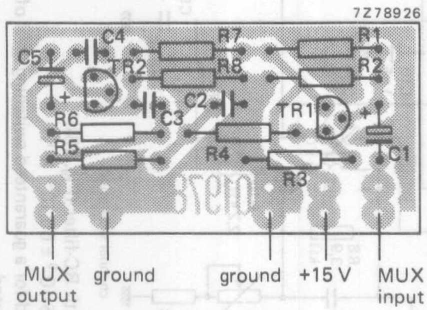



Fig. 4 Printed-circuit board component side, showing component layout.

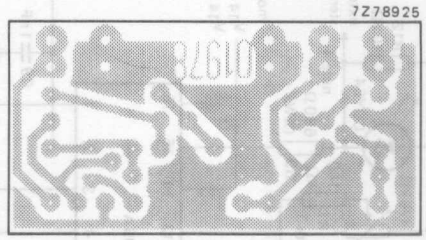
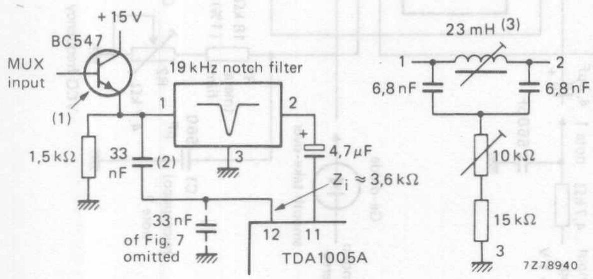
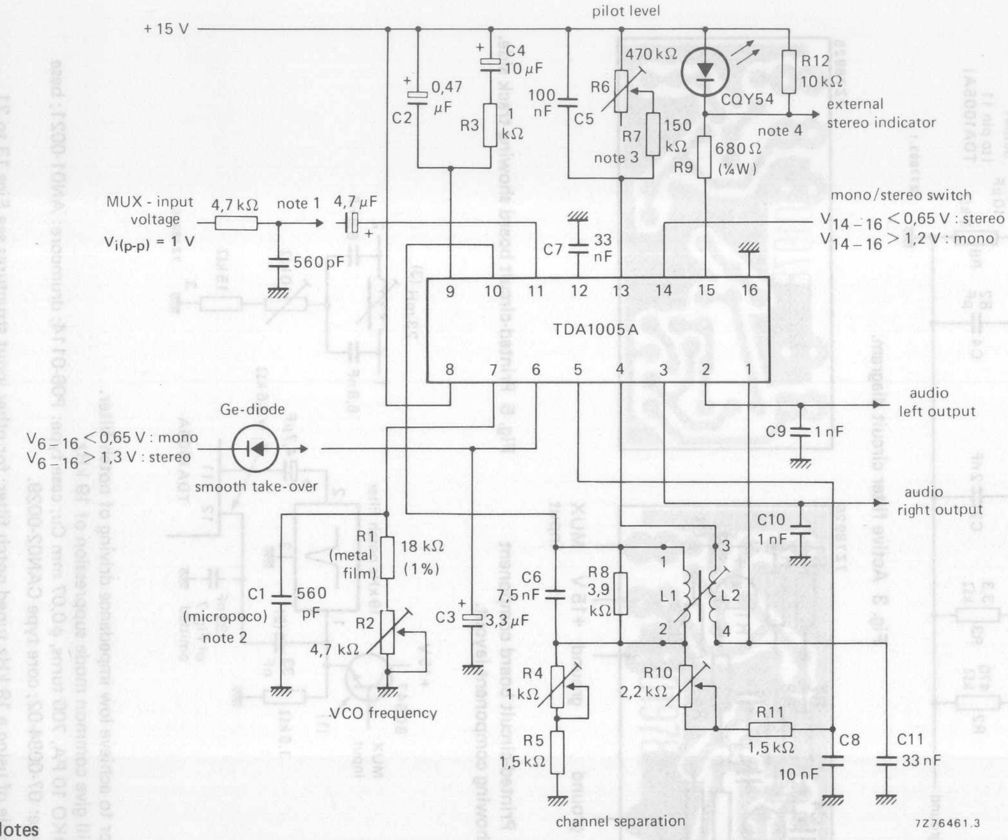



Fig. 5 Printed-circuit board showing track side.




(1) Transistor to achieve low impedance driving of notch filter.
(2) 33 nF will give common mode suppression of 19 kHz.
(3) Coil: TOKO 10 PA, 700 turns, $\phi$0,07 mm Cu; case type: P06-0114; drumcore: AN01-0021; base 5 pins type: 07-0084-02; core type CAN02-0029.

Fig. 6 Example of using a 19 kHz tuned notch filter; for other input structures see Figs 13 to 21.




Coil data:

$L_1L_2 = 2,6$ mH

$Q_{1\text{-}2} = 35$; $Q_{min} \doteq 30$

$N_{1\text{-}2} = 357½$ turns;

$N_{3\text{-}4} = 297½$ turns:

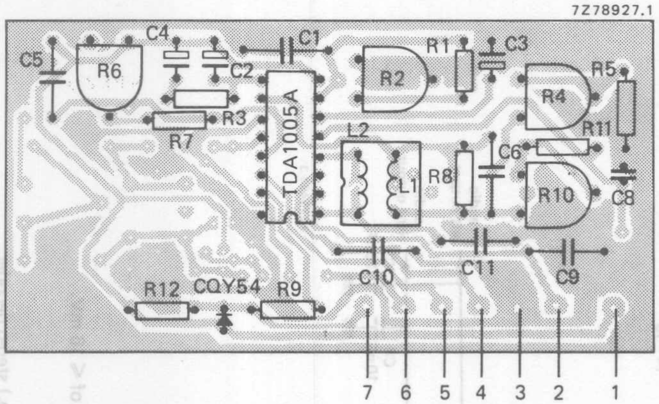
scrambled wound with wire diameter 0,09 mm,

$$\frac{E_{3\text{-}4}}{E_{1\text{-}2}} \times 100\% = 82\%$$

## Notes

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ $K^{-1}$.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of ⩽ 16 mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 7 Basic application circuit of a frequency-division multiplex (f.d.m.) stereo decoder.




1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 8 Printed-circuit board component side of an f.d.m. decoder, showing component layout. For circuit diagram see Fig. 7.

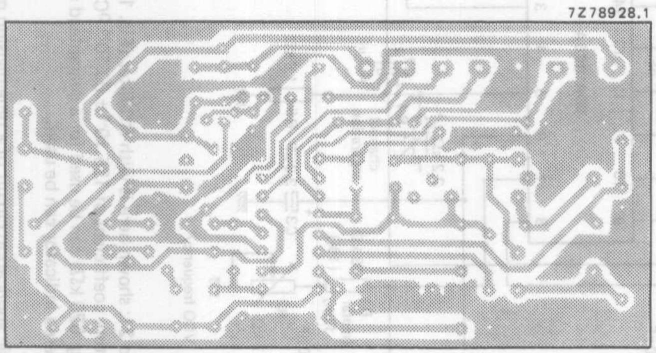
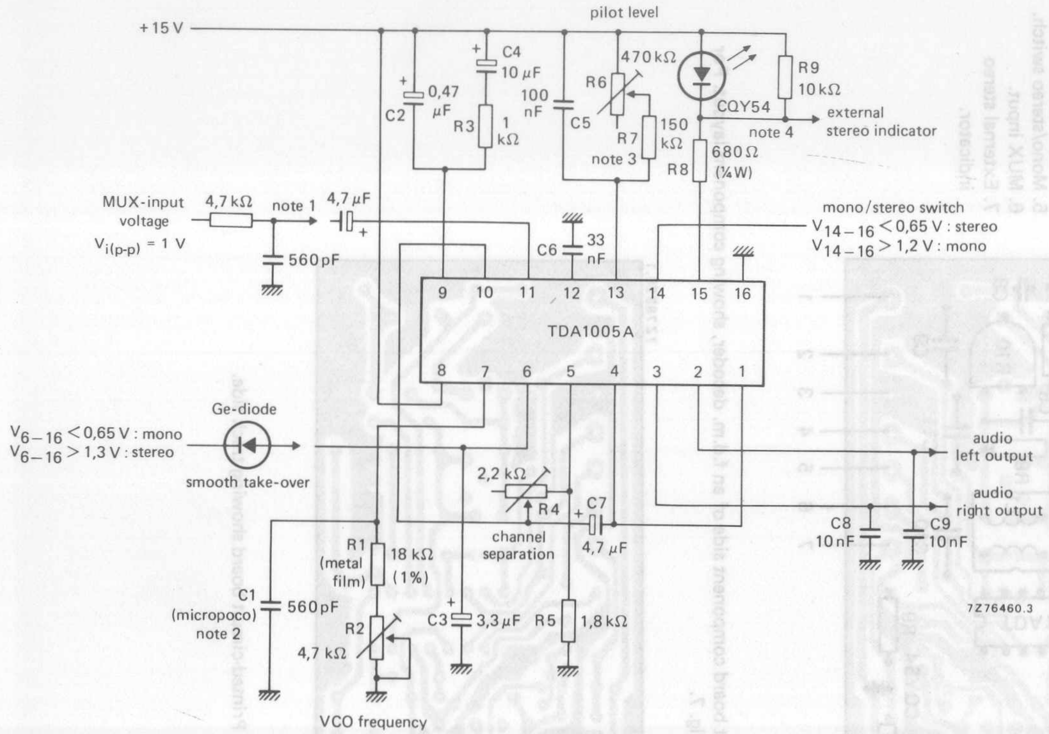



Fig. 9 Printed-circuit board showing track side.

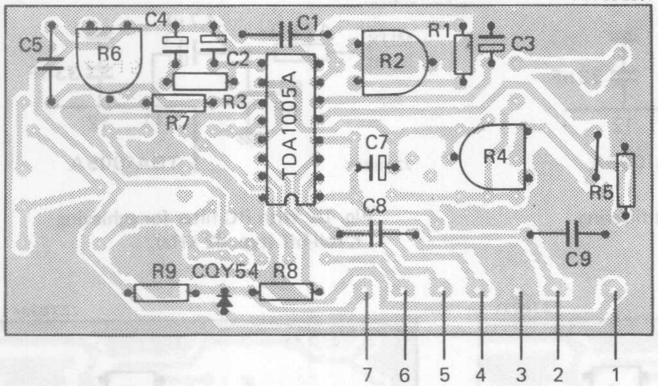



Notes

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ $^{o}C^{-1}$.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of ⩽ 16 mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 10 Basic application circuit of a time-division multiplex (t.d.m.) stereo decoder.

7Z78929.1




1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 11 Printed-circuit board component side of a t.d.m. decoder, showing component layout. For circuit diagram see Fig. 10.

7Z78928.1

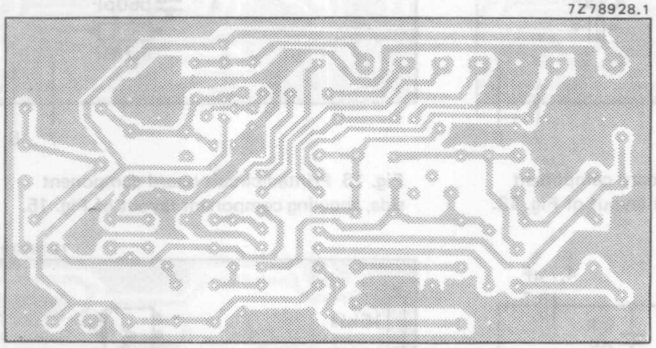


Fig. 12 Printed-circuit board showing track side.

INPUT STRUCTURES (see also Figs 7 and 10)

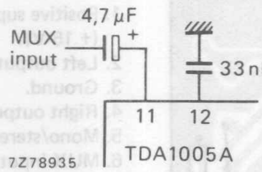



Fig. 13 Without filtering.

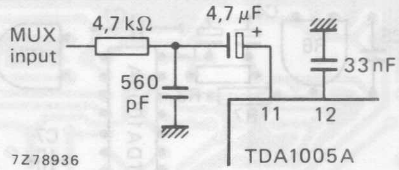



Fig. 15 With RC-filter for achieving i.f. roll-off (typ. 62 kHz).

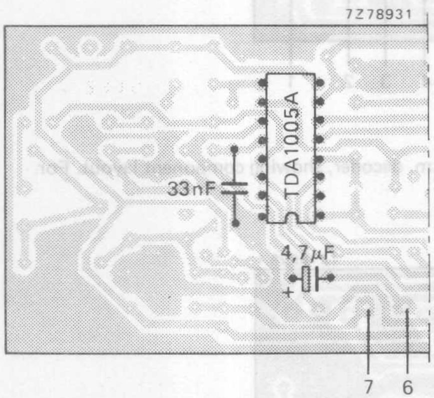



Fig. 14 Printed-circuit board component side, showing component layout of Fig. 13.

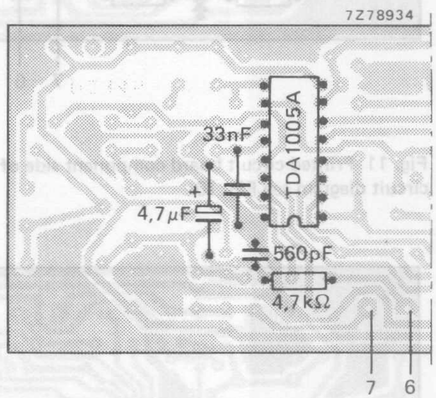



Fig. 16 Printed-circuit board component side, showing component layout of Fig. 15.

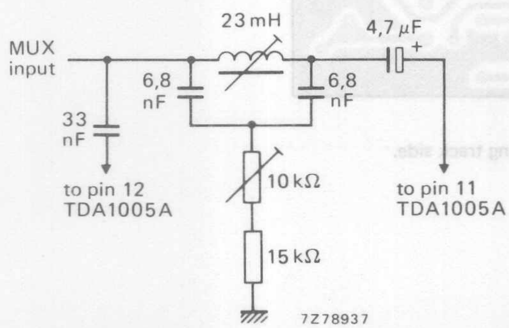



Fig. 17 With 19 kHz notch filter.

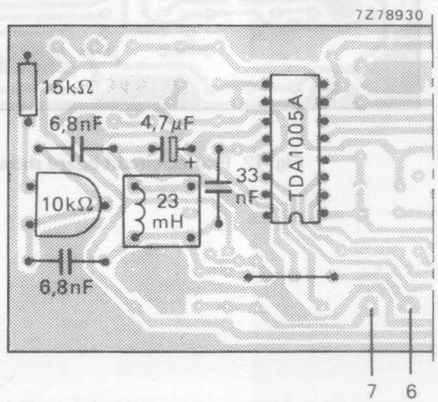



Fig. 18 Printed-circuit board component side, showing component layout of Fig. 17.

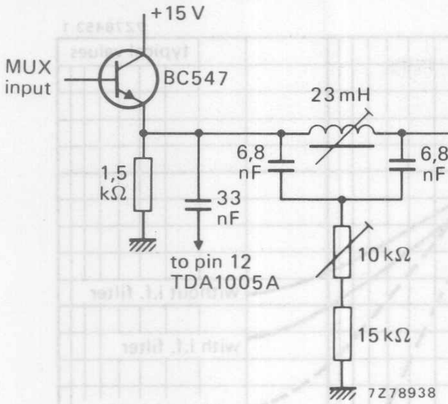



Fig. 19 With buffer stage (to achieve low impedance driving of notch filter; see Fig. 6) and 19 kHz notch filter.

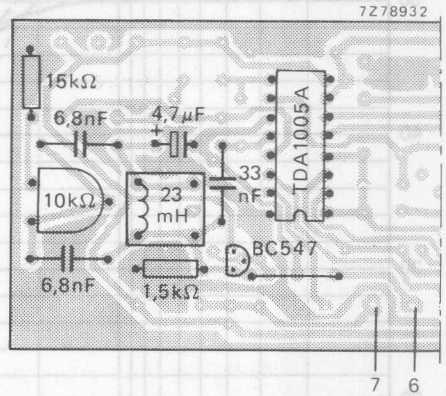



Fig. 20 Printed-circuit board component side, showing component layout of Fig. 19.

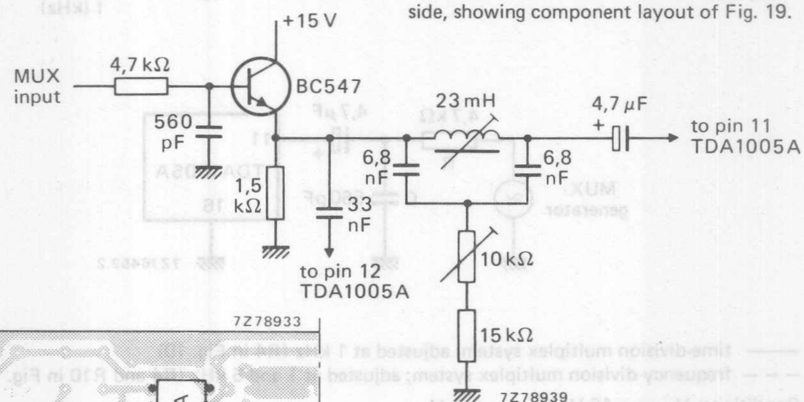



Fig. 21 With RC-filter, buffer stage and 19 kHz notch filter.

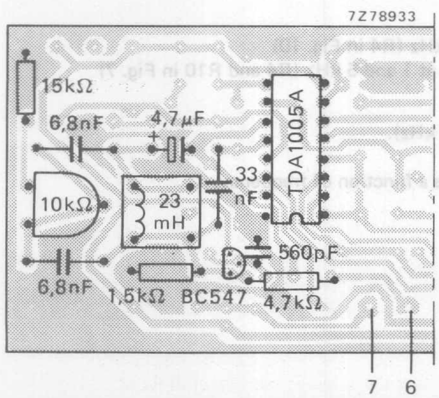
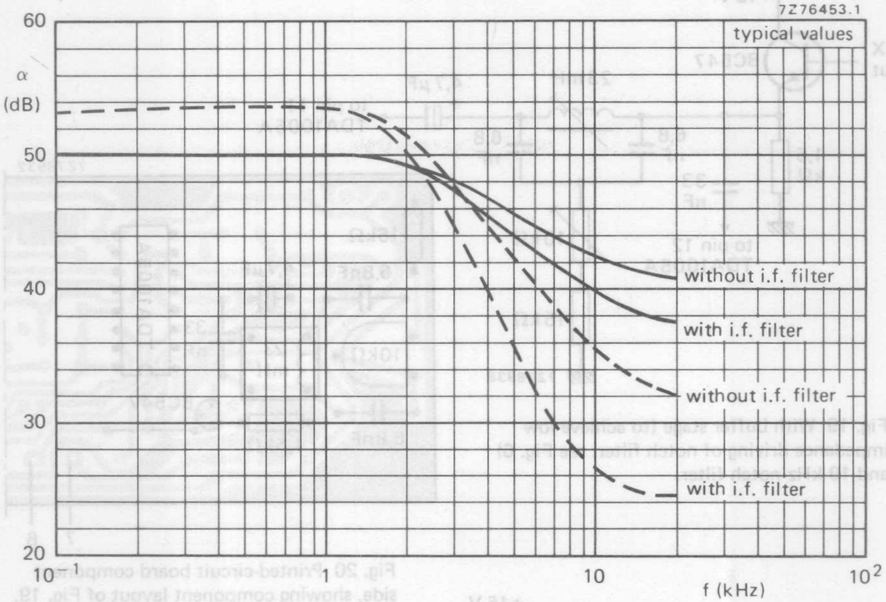
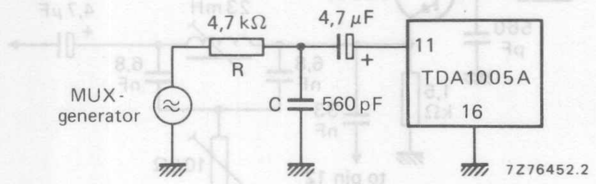



Fig. 22 Printed-circuit board component side, showing component layout of Fig. 21.




—— time-division multiplex system; adjusted at 1 kHz (R4 in Fig. 10)
– – – frequency-division multiplex system; adjusted at 1 and 5 kHz (R4 and R10 in Fig. 7)

Conditions: $V_{8\text{-}16} = 15$ V; $V_{i(p\text{-}p)} = 1$ V.

Note: RC-filter for simulating the i.f. roll-off (typ. 62 kHz).

Fig. 23 Channel separation as a function of frequency.

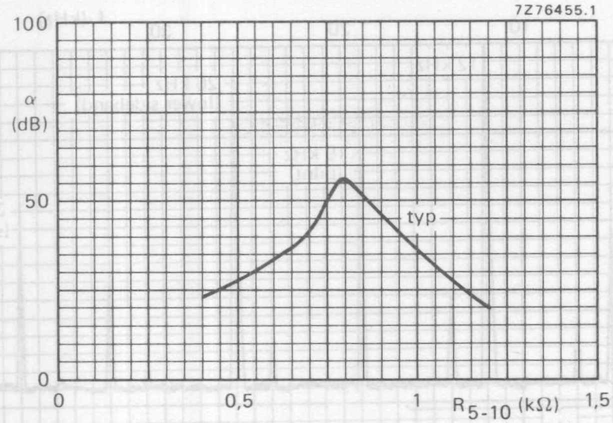



Fig. 24 Channel separation at f = 1 kHz as a function of resistance between pins 5 and 10 for a t.d.m. system. For test circuit see Fig. 23.

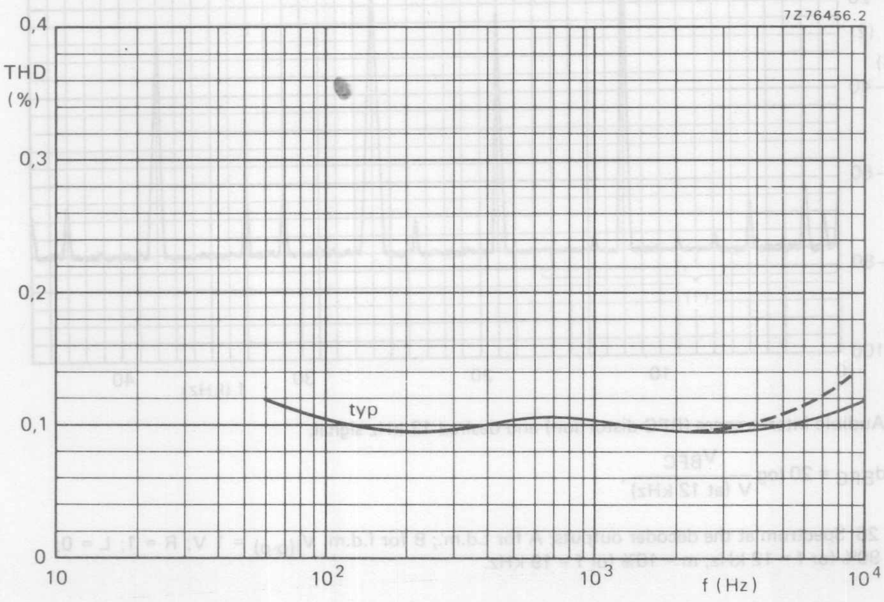
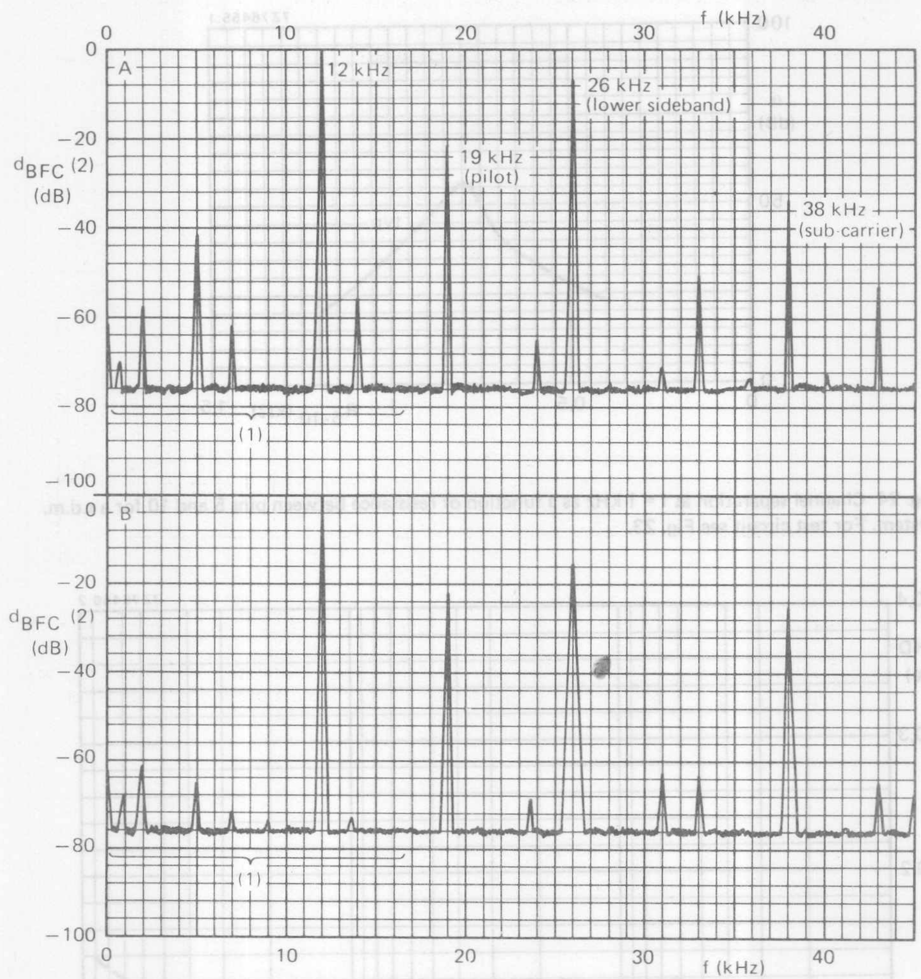



Fig. 25 Distortion as a function of audio frequency; R = 1; L = 0; $V_{8\text{-}16}$ = 15 V; $V_{2\text{-}16} = V_{3\text{-}16}$ = 1 V (r.m.s.). – – – t.d.m. system; ——— f.d.m. system.




(1) Audible interferences (BFC-distortion) and desired 12 kHz signal.

(2) $d_{BFC} = 20 \log \frac{V_{BFC}}{V \text{ (at 12 kHz)}}$.

Fig. 26 Spectrum at the decoder outputs; A for t.d.m.; B for f.d.m. $V_{i(p-p)} = 1$ V; R = 1; L = 0; m = 90% for f = 12 kHz; m = 10% for f = 19 kHz.

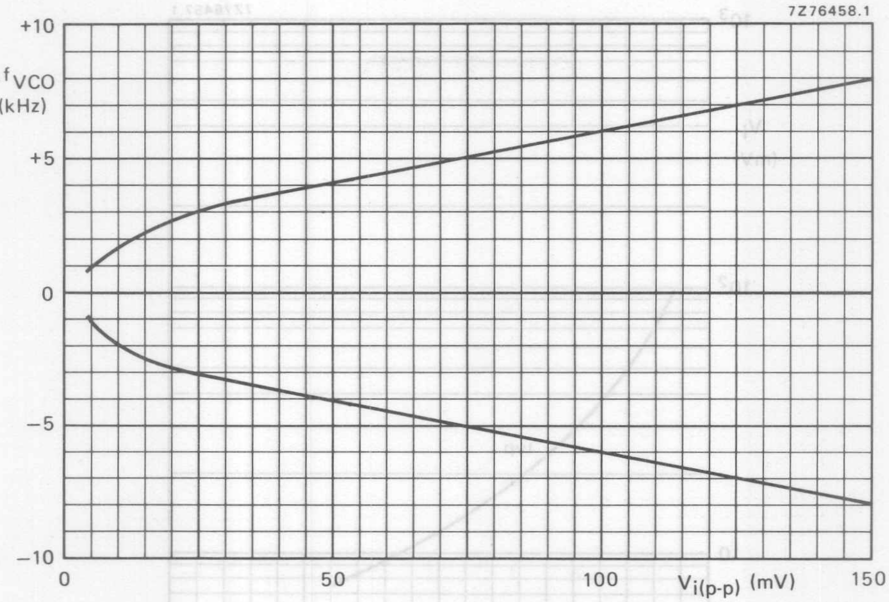



Fig. 27 Typical values of the capture range of the oscillator as a function of the pilot threshold voltage at MUX-input.
$V_{8\text{-}16}$ = 15 V; $\Delta f_{VCO} = f_{VCO} - 76$ kHz where: $f_{VCO}$ = modulated, free-running oscillator frequency; $\Delta f_{VCO}$ = maximum $f_{VCO}$ deviation which will be captured if pilot signal (pin 11) is switched-on.

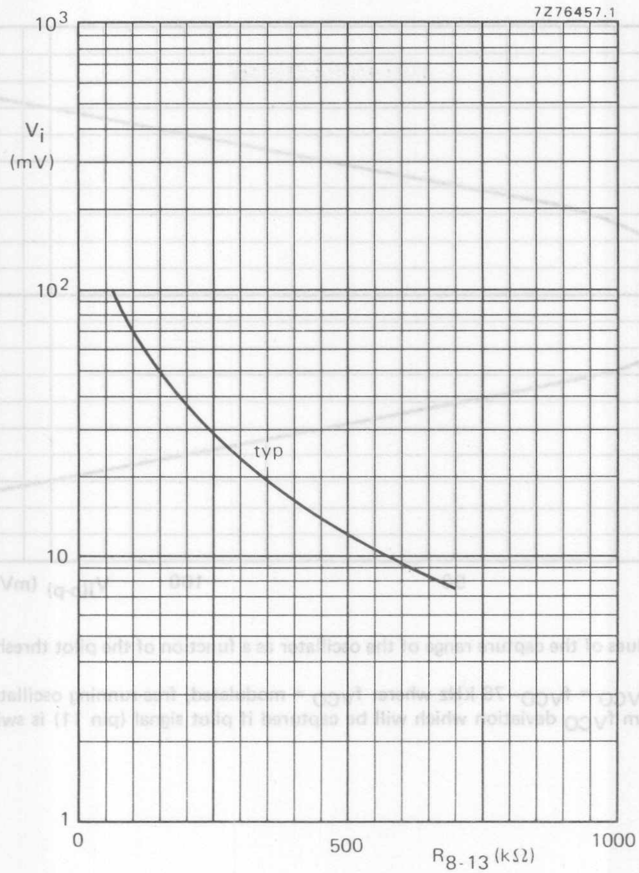



Fig. 28 Pilot input voltage switching level (stereo 'on') as a function of resistance between pins 8 and 13.

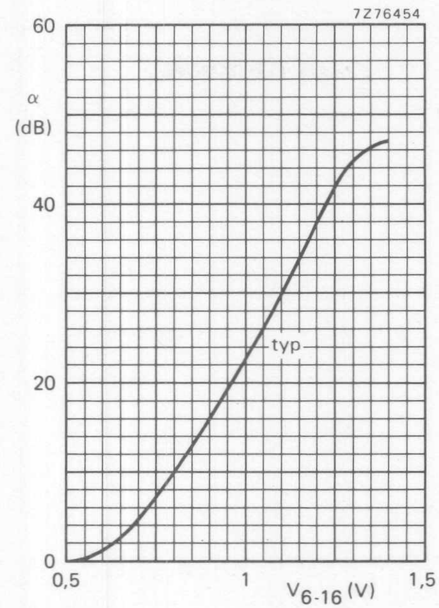



Fig. 29 Channel separation as a function of $V_{6\text{-}16}$ at 1 kHz (smooth take-over).

# 6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
# 10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:
- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 24 | V |
| Repetitive peak output current | $I_{ORM}$ | max. | 3 | A |
| Output power at pin 2; $d_{tot}$ = 10% | | | | |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | typ. | 6,4 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6,2 | W |
| $V_P$ = 14,4 V; $R_L$ = 8 Ω | $P_o$ | typ. | 3,4 | W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4 | $P_o$ | typ. | 9 | W |
| Total harmonic distortion at $P_o$ = 1 W; $R_L$ = 4 Ω | $d_{tot}$ | typ. | 0,2 | % |
| Input impedance | | | | |
| preamplifier (pin 8) | $\vert Z_i \vert$ | typ. | 30 | kΩ |
| power amplifier (pin 6) | $\vert Z_i \vert$ | typ. | 20 | kΩ |
| Total quiescent current at $V_P$ = 14,4 V | $I_{tot}$ | typ. | 31 | mA |
| Sensitivity for $P_o$ = 5,8 W; $R_L$ = 4 Ω | $V_i$ | typ. | 10 | mV |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

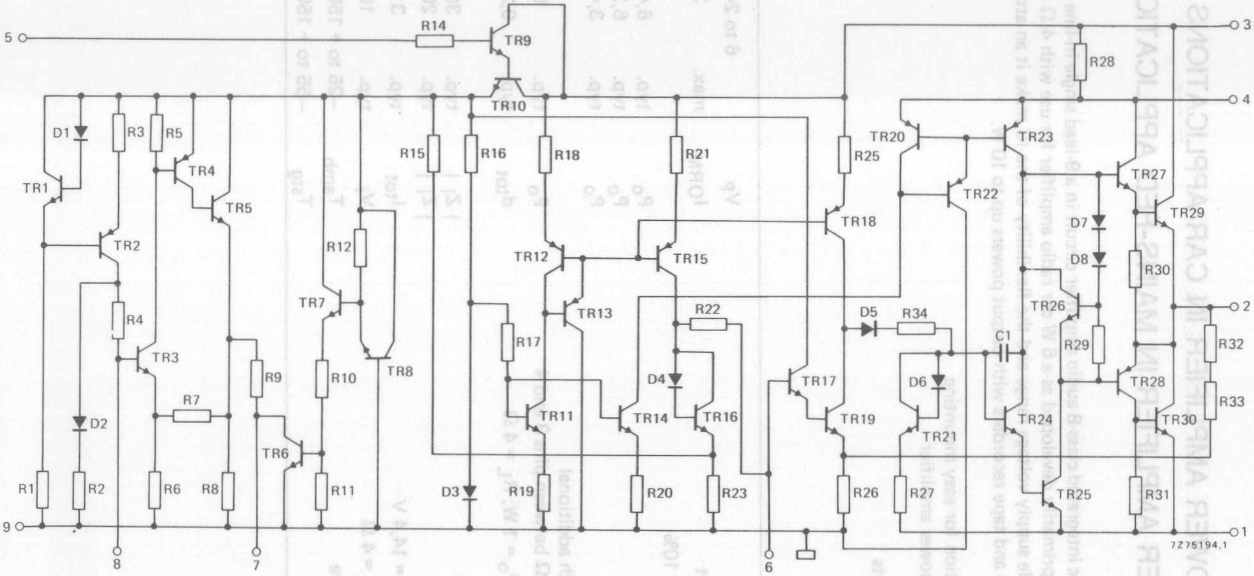



Fig. 1 Circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 24 V |
| Peak output current | $I_{OM}$ | max. | 5 A |
| Repetitive peak output current | $I_{ORM}$ | max. | 3 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during sine-wave drive; without heatsink at $V_P$ = 14,4 V | $t_{sc}$ | max. | 100 hours |

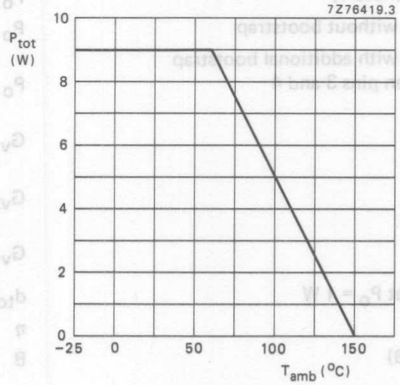



Fig. 2 Power derating curve.

## HEATSINK DESIGN

Assume $V_P$ = 14,4 V; $R_L$ = 2 Ω; $T_{amb}$ = 60 °C maximum; thermal shut-down starts at $T_j$ = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3,9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$$R_{th\ h\text{-}a} = 23 - (10 + 1) = 12\ \text{K/W}.$$

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 24 | V |
| Repetitive peak output current | $I_{ORM}$ | $<$ | 3 | A |
| Total quiescent current at $V_P$ = 14,4 V | $I_{tot}$ | typ. | 31 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 14,4 V; $R_L$ = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

| | | | | |
|---|---|---|---|---|
| A.F. output power (see Fig. 4) at $d_{tot}$ = 10%; measured at pin 2; with bootstrap | | | | |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω (note 1) | $P_o$ | typ. | 6,4 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω (note 1 and 2) | $P_o$ | $>$ | 5,9 | W |
| | | typ. | 6,2 | W |
| $V_P$ = 14,4 V; $R_L$ = 8 Ω (note 1) | $P_o$ | typ. | 3,4 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω; without bootstrap | $P_o$ | typ. | 5,7 | W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4 | $P_o$ | typ. | 9 | W |
| Voltage gain | | | | |
| preamplifier (note 3) | $G_{v1}$ | typ. | 24 | dB |
| | | | 21 to 27 | dB |
| power amplifier | $G_{v2}$ | typ. | 30 | dB |
| | | | 27 to 33 | dB |
| total amplifier | $G_{v\,tot}$ | typ. | 54 | dB |
| | | | 51 to 57 | dB |
| Total harmonic distortion at $P_o$ = 1 W | $d_{tot}$ | typ. | 0,2 | % |
| Efficiency at $P_o$ = 6 W | $\eta$ | typ. | 75 | % |
| Frequency response (−3 dB) | B | | 80 Hz to 15 | kHz |
| Input impedance | | | | |
| preamplifier (note 4) | $\lvert Z_i \rvert$ | typ. | 30 | kΩ |
| | | | 20 to 40 | kΩ |
| power amplifier (note 5) | $\lvert Z_i \rvert$ | typ. | 20 | kΩ |
| | | | 14 to 26 | kΩ |
| Output impedance of preamplifier; pin 7 (note 5) | $\lvert Z_o \rvert$ | typ. | 20 | kΩ |
| | | | 14 to 26 | kΩ |
| Output voltage preamplifier (r.m.s. value) | | | | |
| $d_{tot}$ < 1% (pin 7) (note 3) | $V_{o(rms)}$ | $>$ | 0,7 | V |
| Noise output voltage (r.m.s. value; note 6) | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,3 | mV |
| $R_S$ = 8,2 kΩ | $V_{n(rms)}$ | typ. | 0,7 | mV |
| | | $<$ | 1,4 | mV |
| Ripple rejection at f = 1 kHz to 10 kHz (note 7) | RR | $>$ | 42 | dB |
| at f = 100 Hz; C2 = 1 μF | RR | $>$ | 37 | dB |
| Sensitivity for $P_o$ = 5,8 W | $V_i$ | typ. | 10 | mV |
| Bootstrap current at onset of clipping; pin 4 (r.m.s. value) | $I_{4(rms)}$ | typ. | 30 | mA |

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

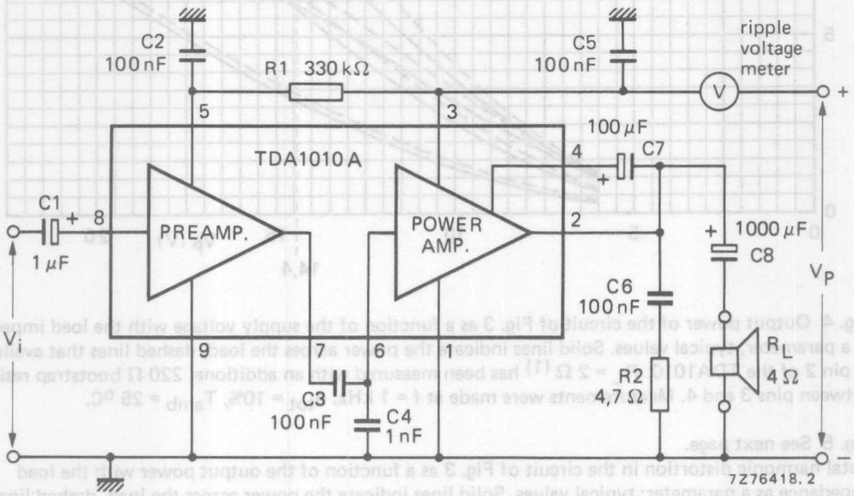



Fig. 3 Test circuit.

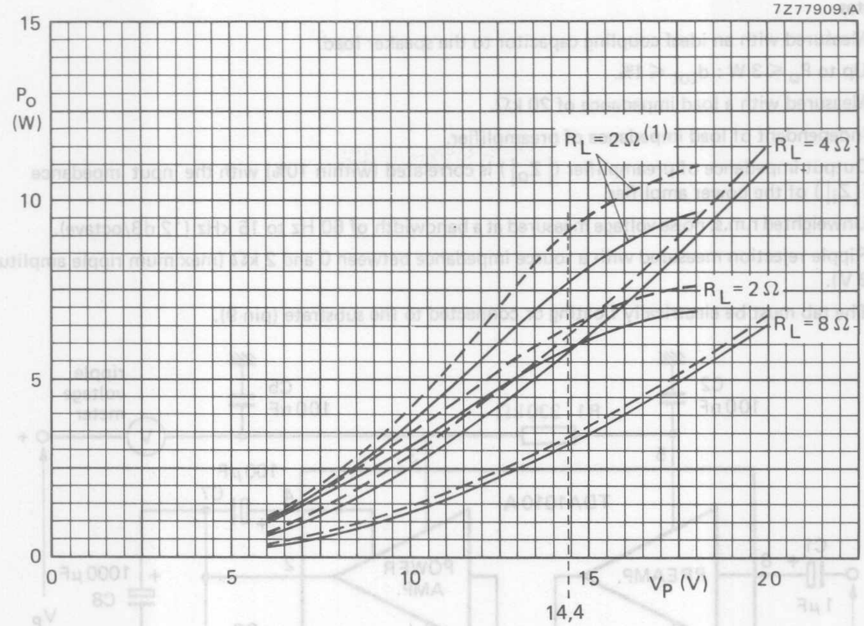



Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, $d_{tot}$ = 10%, $T_{amb}$ = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, $V_P$ = 14,4 V.

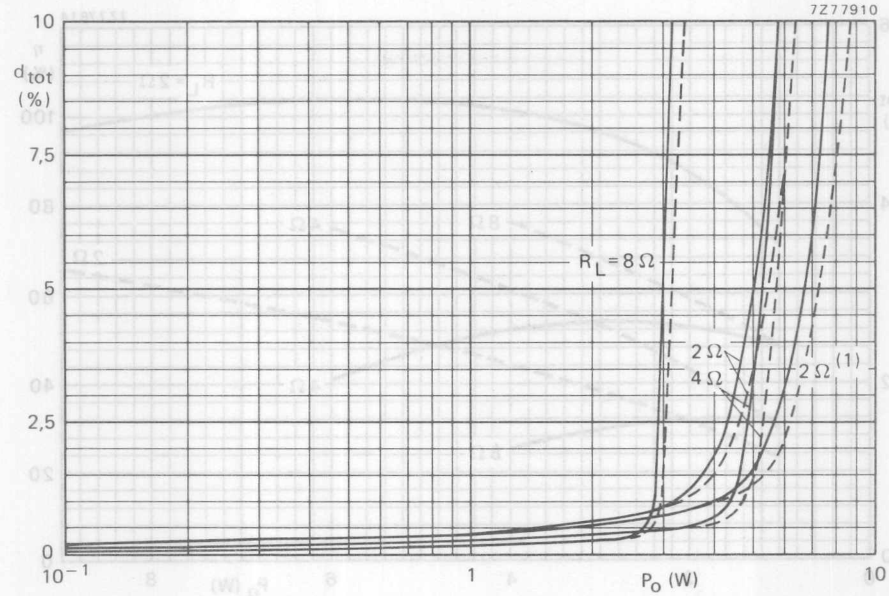



Fig. 5 For caption see preceding page.

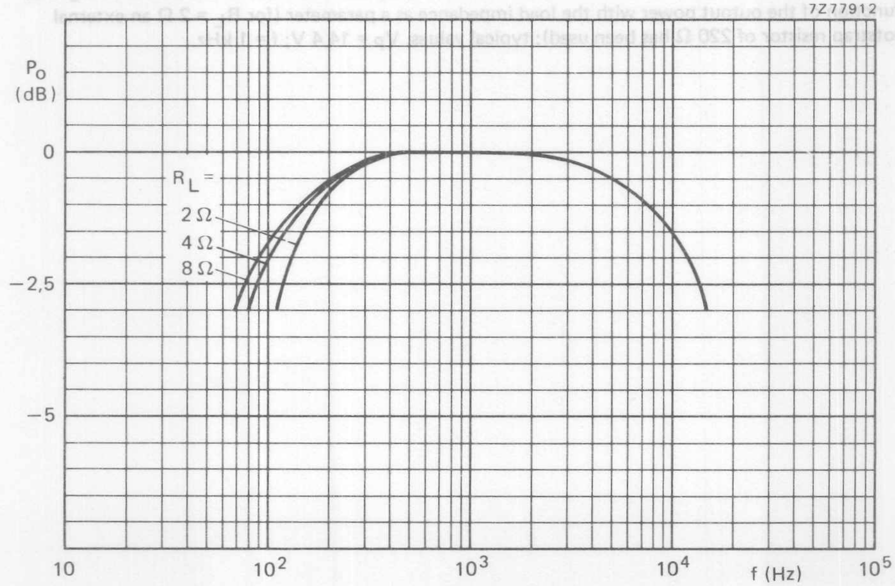



Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. $P_O$ relative to 0 dB = 1 W; $V_P$ = 14,4 V.

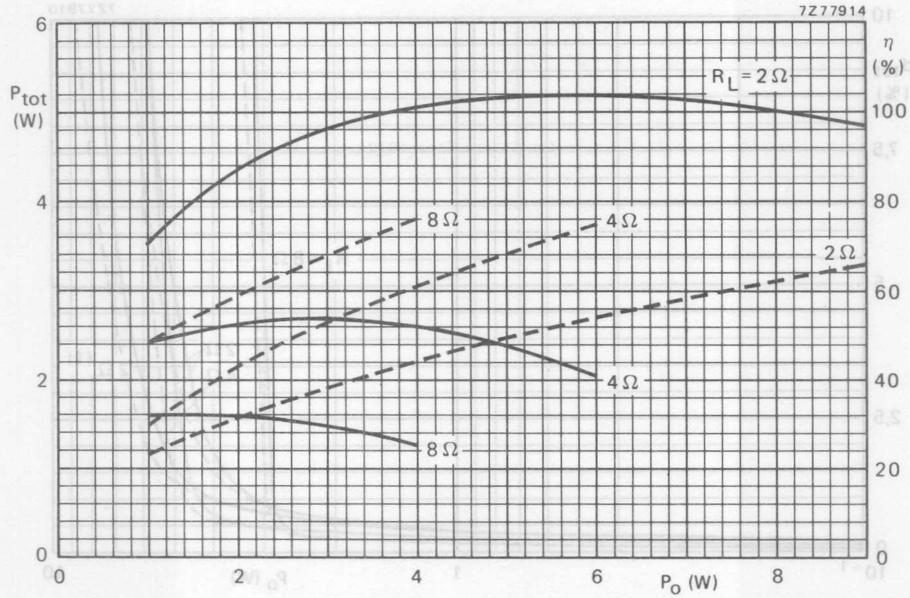



Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\ \Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

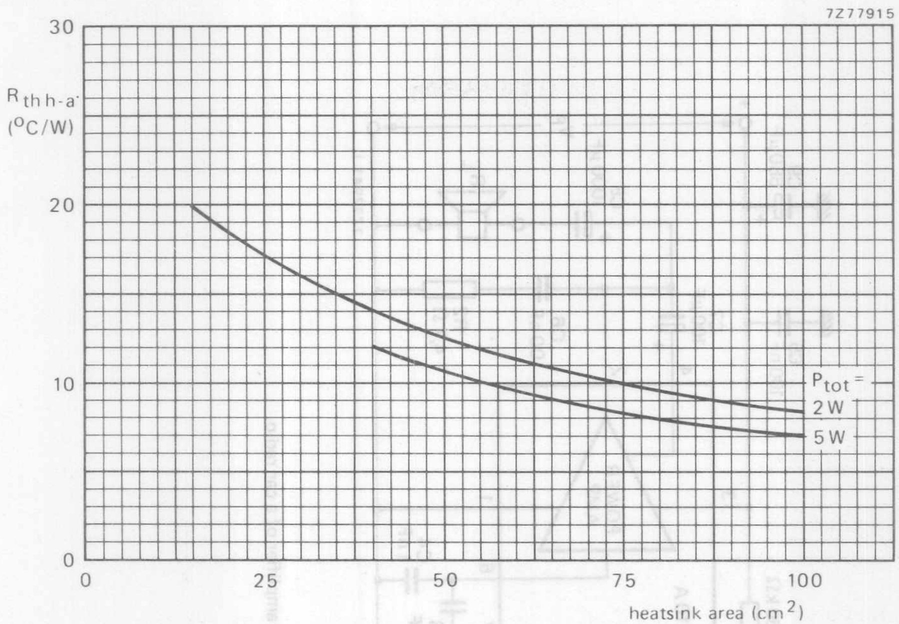



Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

## APPLICATION INFORMATION

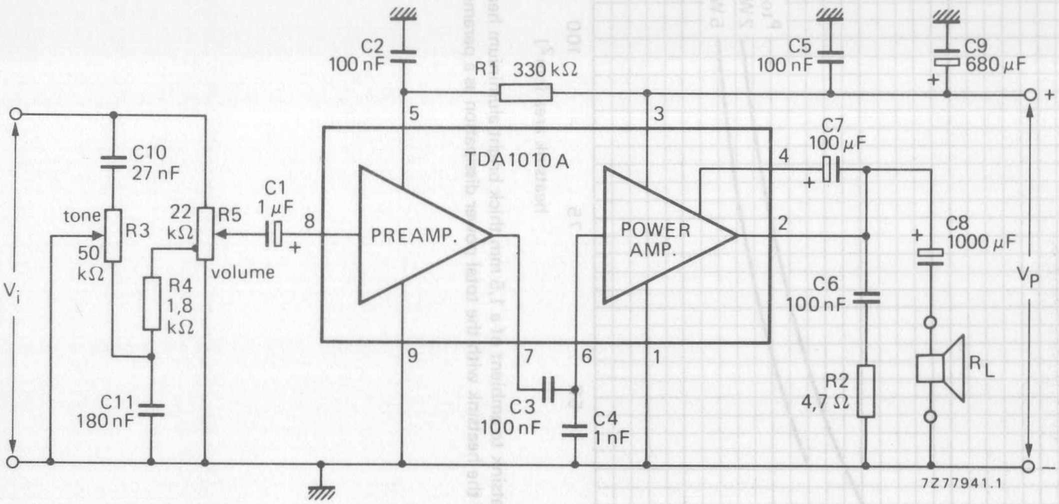



Fig. 9 Complete mono audio amplifier of a car radio.

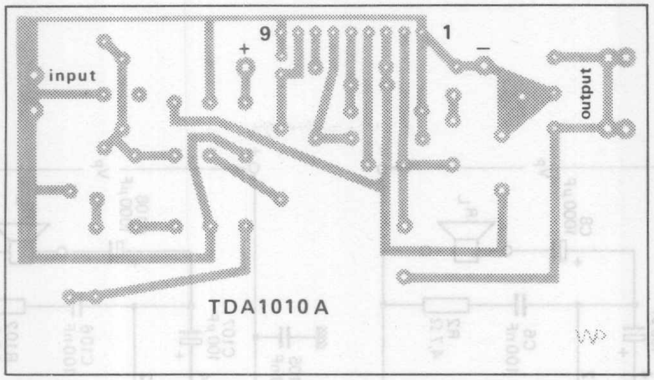



Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

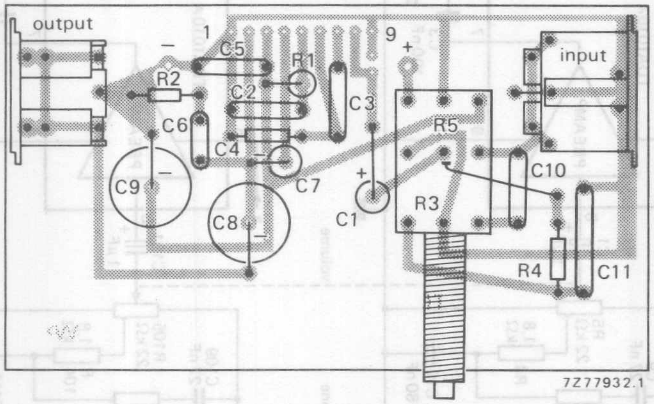



Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

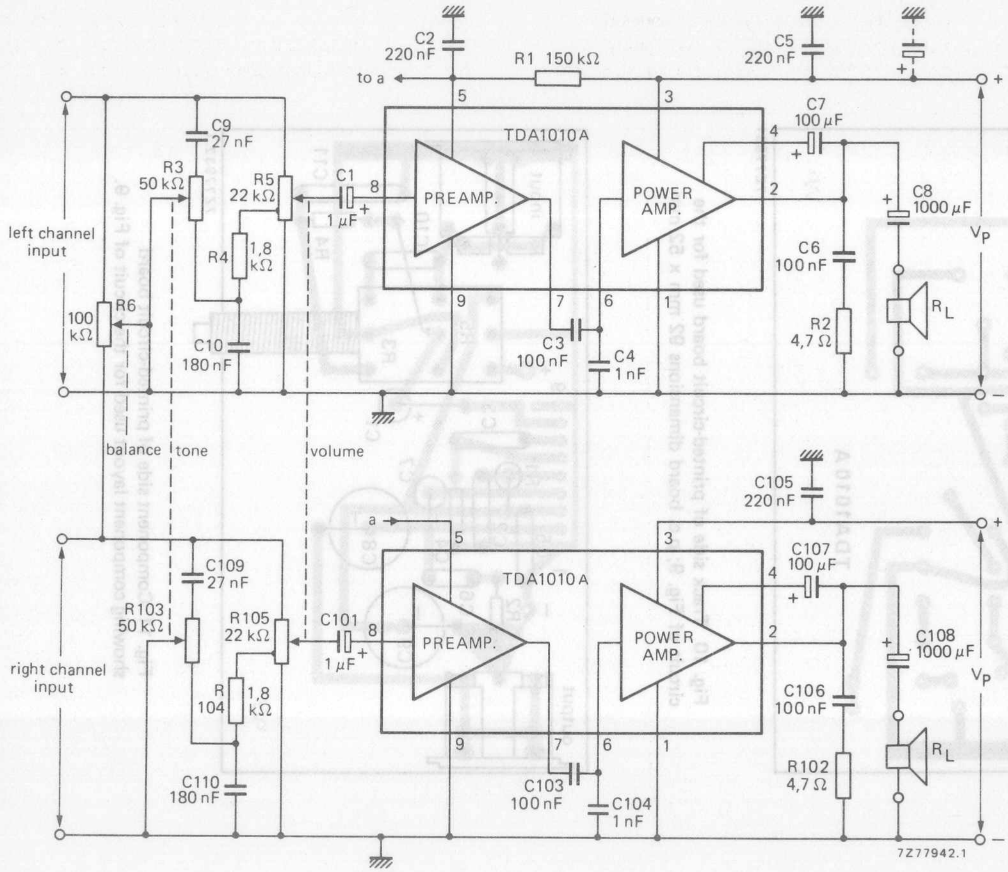



Fig. 12 Complete stereo car radio amplifier.

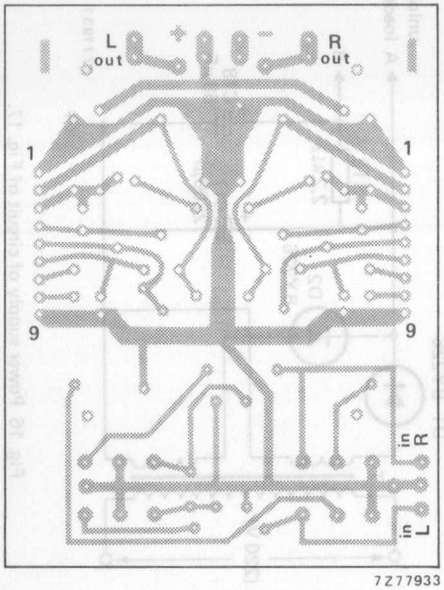



Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

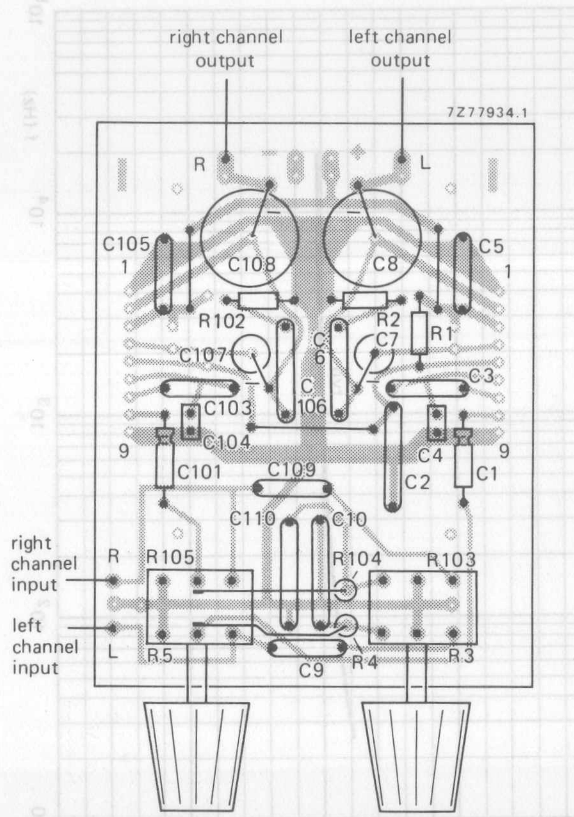



Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

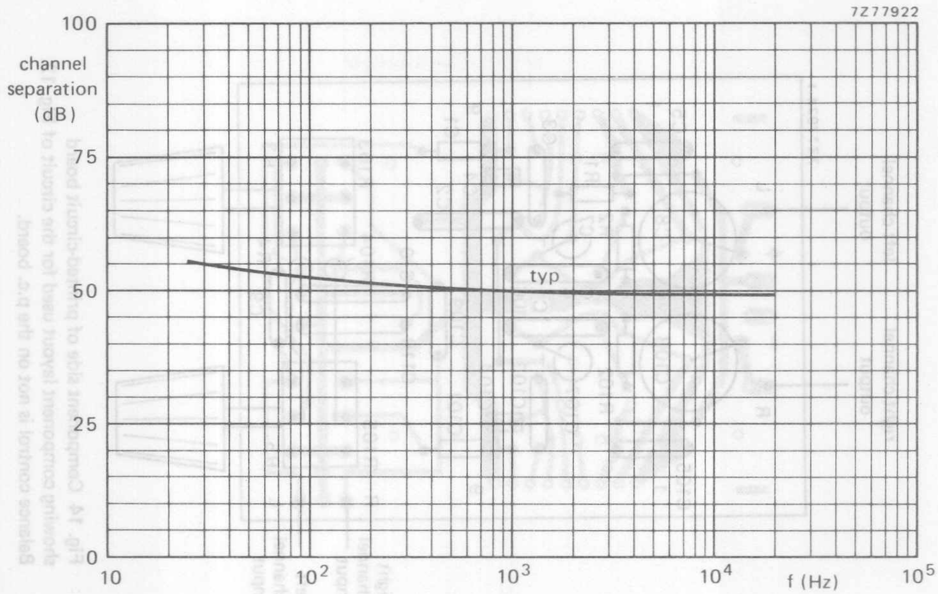



Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

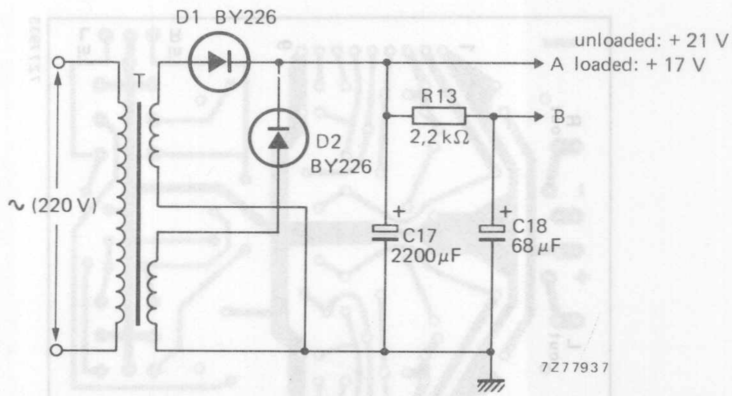



Fig. 16 Power supply of circuit of Fig. 17.

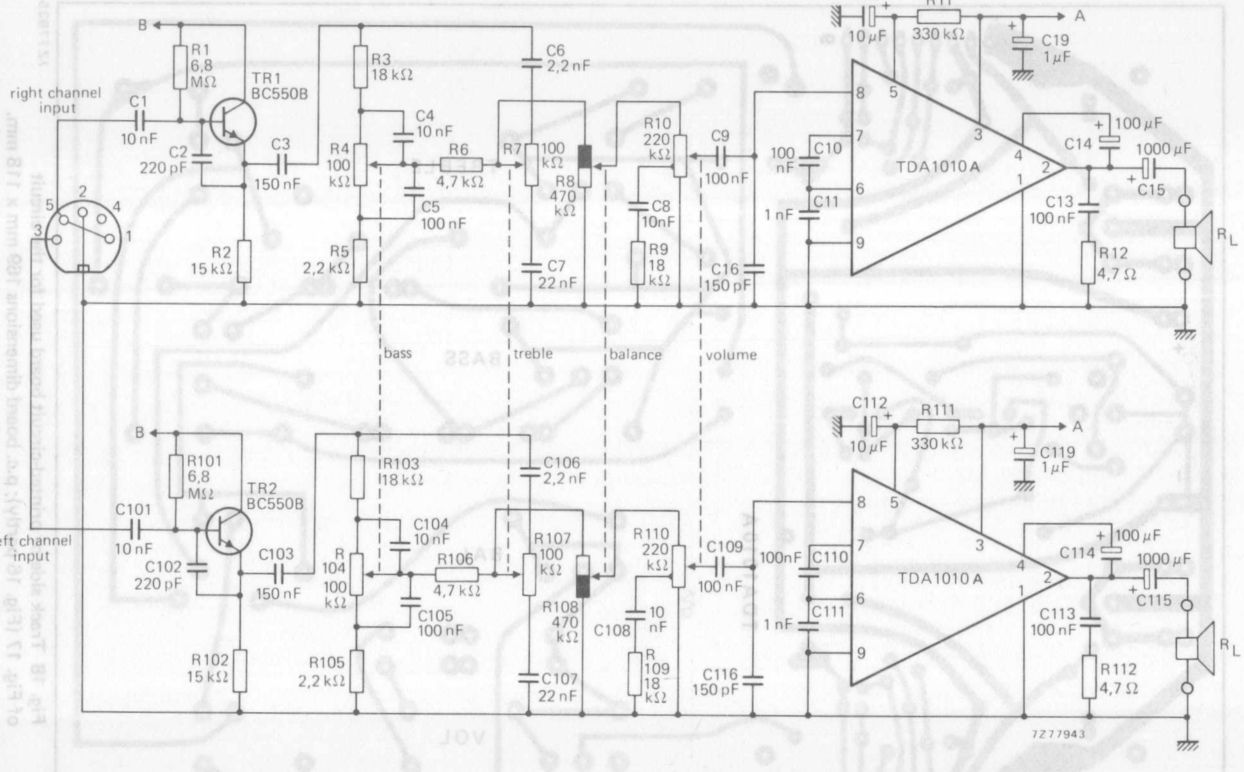



Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

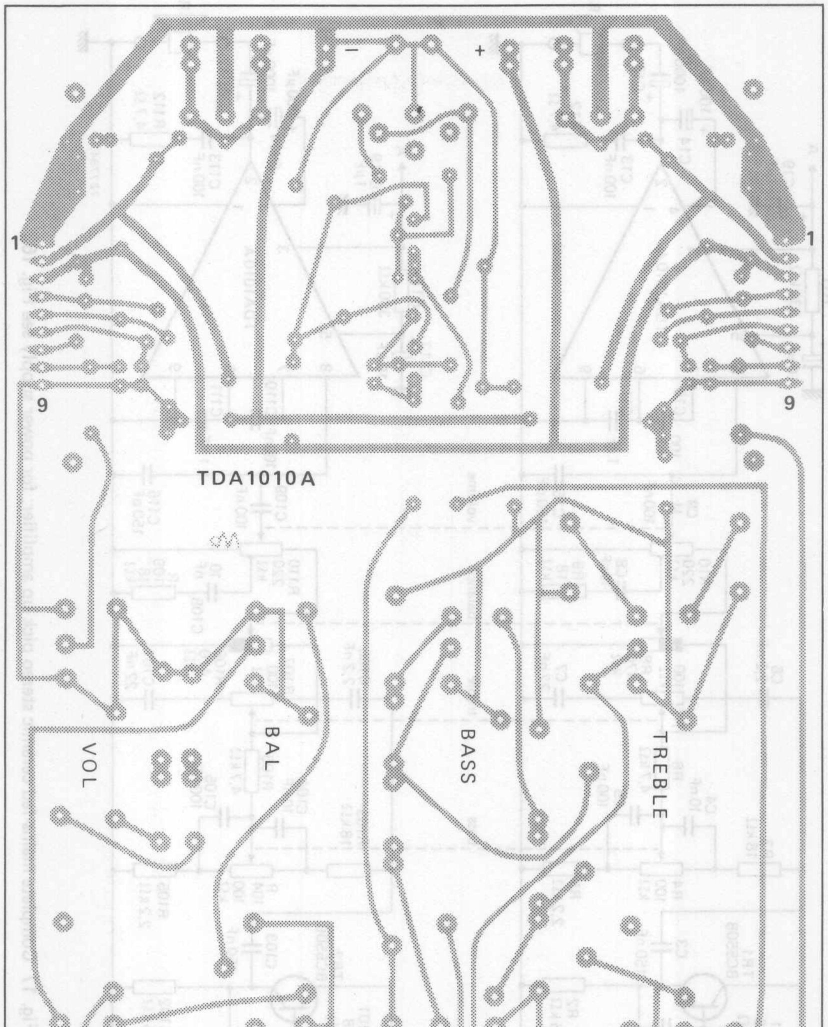



Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

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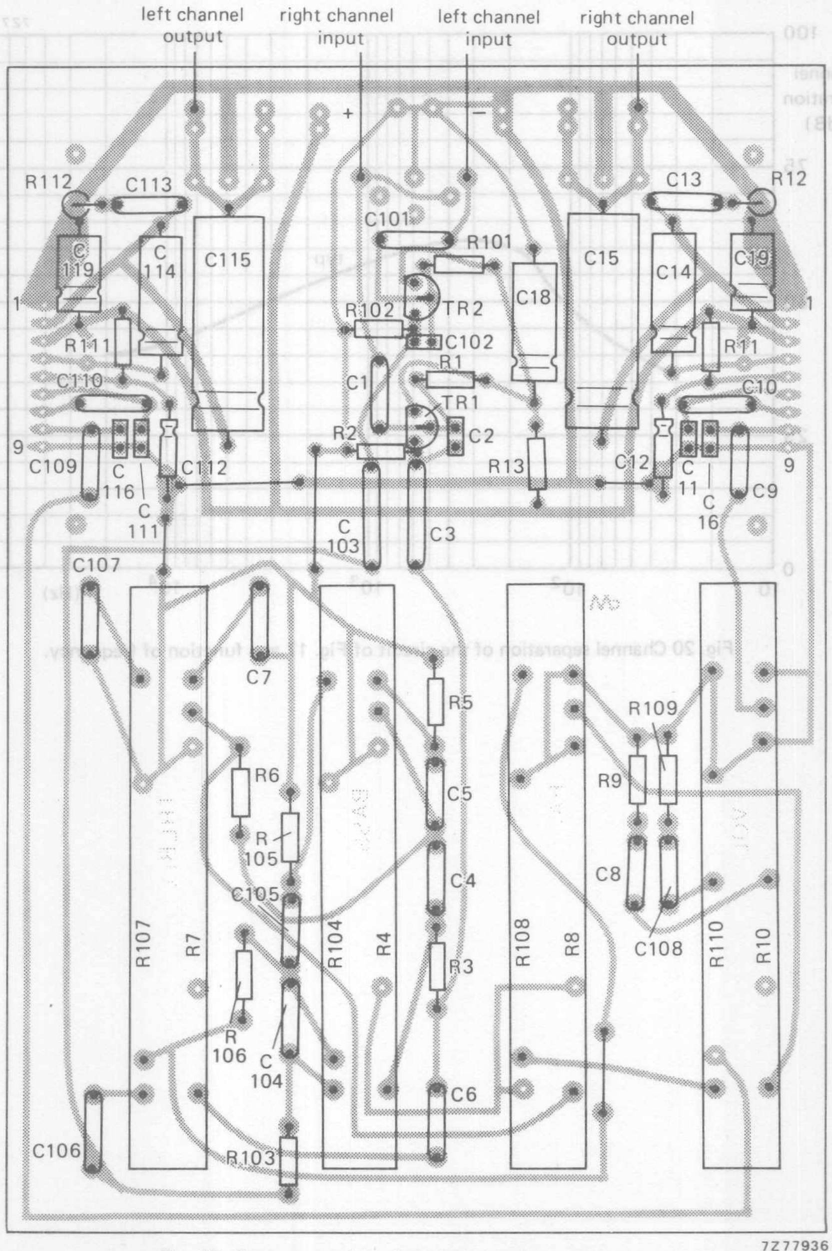



Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

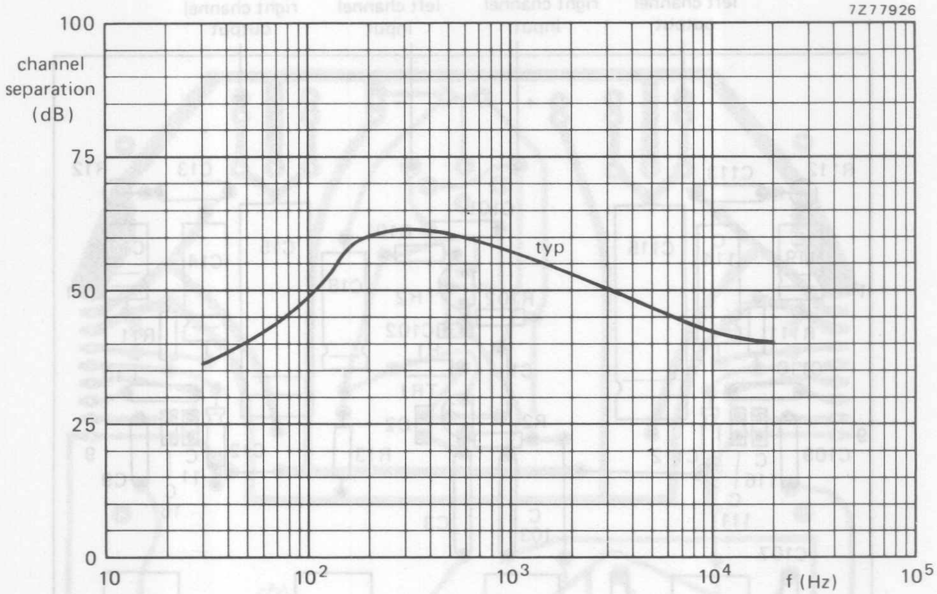



Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

# 2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 20 | V |
| Peak output current | $I_{OM}$ | max. | 3 | A |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 16 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6,5 | W |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| Total harmonic distortion at $P_o$ = 1 W; $R_L$ = 4 Ω | $d_{tot}$ | typ. | 0,2 | % |
| Input impedance | | | | |
| preamplifier (pin 8) | $\|Z_i\|$ | > | 100 | kΩ |
| power amplifier (pin 6) | $\|Z_i\|$ | typ. | 20 | kΩ |
| Total quiescent current | $I_{tot}$ | typ. | 14 | mA |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

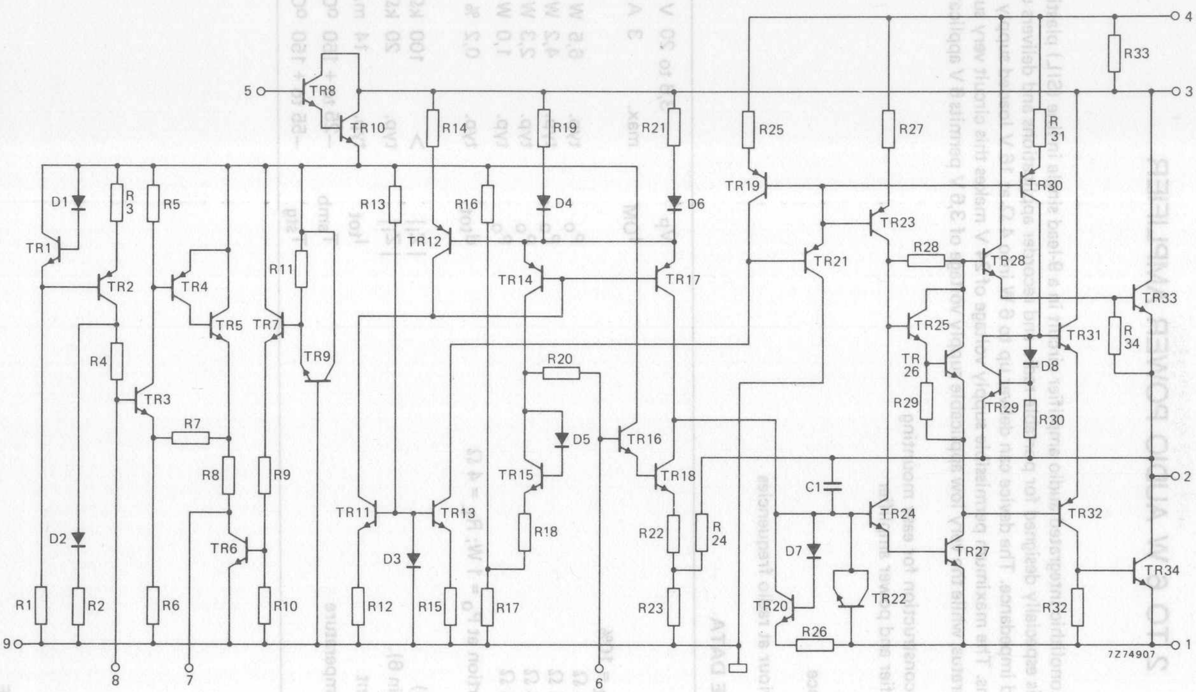



Fig. 1 Circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 24 V |
| Peak output current | $I_{OM}$ | max. | 3 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during sine-wave drive; $V_P$ = 12 V | $t_{sc}$ | max. | 100 hours |

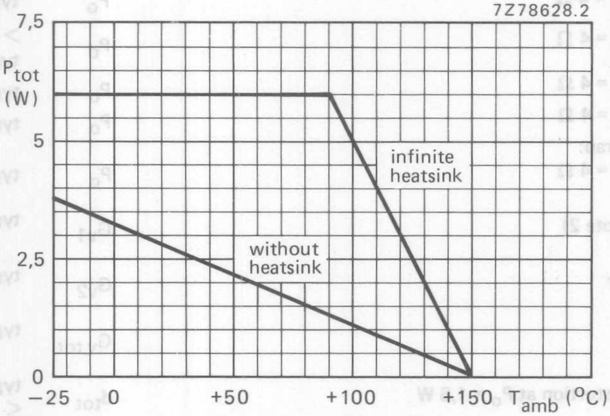



Fig. 2 Power derating curve.

## HEATSINK DESIGN

Assume $V_P$ = 12 V; $R_L$ = 4 Ω; $T_{amb}$ = 60 °C maximum; $P_o$ = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{1,8} = 50\ \mathrm{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 20 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 2 | A |
| Total quiescent current at $V_P$ = 12 V | $I_{tot}$ | typ. | 14 | mA |
| | | < | 22 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 12 V; $R_L$ = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

| | | | | |
|---|---|---|---|---|
| A.F. output power at $d_{tot}$ = 10% (note 1) | | | | |
| with bootstrap: | | | | |
| $V_P$ = 16 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6,5 | W |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | > | 3,6 | W |
| | | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| without bootstrap: | | | | |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 3,0 | W |
| Voltage gain: | | | | |
| preamplifier (note 2) | $G_{v1}$ | typ. | 23 | dB |
| | | | 21 to 25 | dB |
| power amplifier | $G_{v2}$ | typ. | 29 | dB |
| | | | 27 to 31 | dB |
| total amplifier | $G_{v\,tot}$ | typ. | 52 | dB |
| | | | 50 to 54 | dB |
| Total harmonic distortion at $P_o$ = 1,5 W | $d_{tot}$ | typ. | 0,3 | % |
| | | < | 1 | % |
| Frequency response; –3 dB (note 3) | B | | 60 Hz to 15 | kHz |
| Input impedance: | | | | |
| preamplifier (note 4) | $\|Z_{i1}\|$ | > | 100 | kΩ |
| | | typ. | 200 | kΩ |
| power amplifier | $\|Z_{i2}\|$ | typ. | 20 | kΩ |
| Output impedance preamplifier | $\|Z_{o1}\|$ | typ. | 1 | kΩ |
| Output voltage preamplifier (r.m.s. value) | | | | |
| $d_{tot}$ < 1% (note 2) | $V_{o(rms)}$ | > | 0,7 | V |
| Noise output voltage (r.m.s. value; note 5) | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,2 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,6 | mV |
| | | < | 1,4 | mV |
| Noise output voltage at f = 500 kHz (r.m.s. value) | | | | |
| B = 5 kHz; $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 8 | μV |
| Ripple rejection (note 6) | | | | |
| f = 1 to 10 kHz | RR | typ. | 42 | dB |
| f = 100 Hz; C2 = 1 μF | RR | > | 35 | dB |
| Bootstrap current at onset of clipping; pin 4 (r.m.s. value) | $I_{4(rms)}$ | typ. | 35 | mA |

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at $P_o$ = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

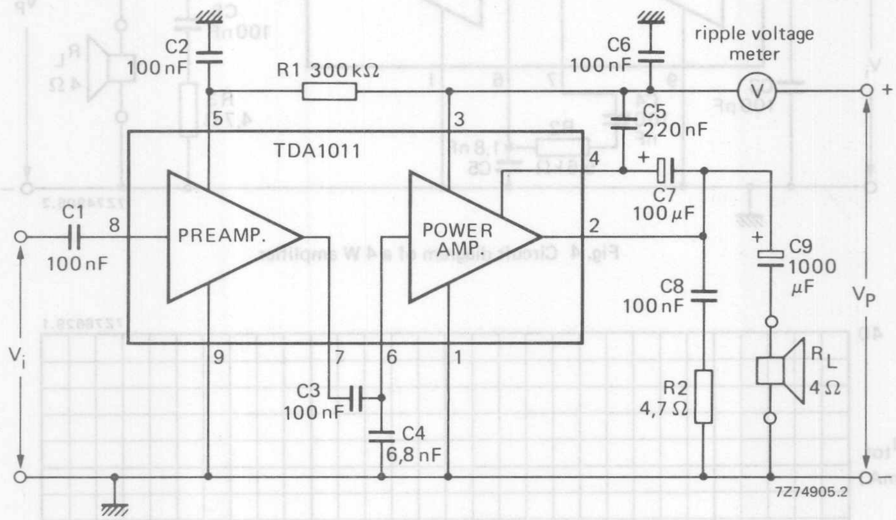



Fig. 3 Test circuit.

## APPLICATION INFORMATION

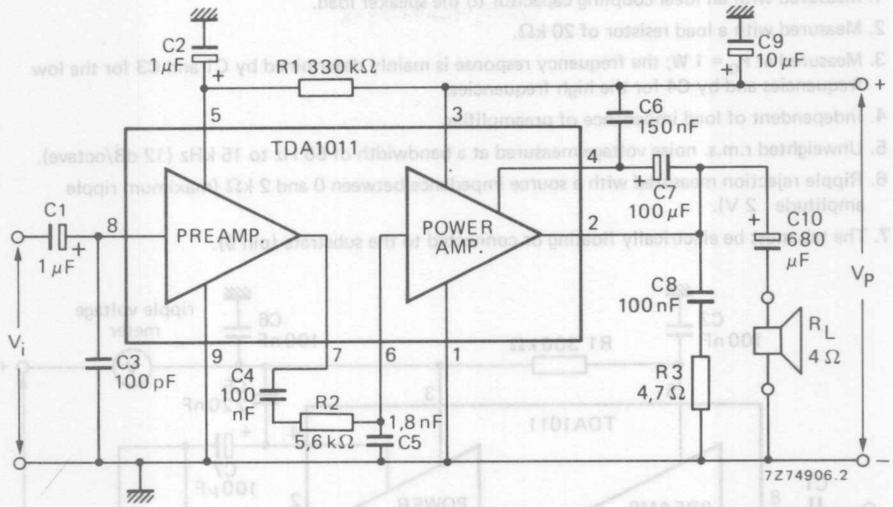



Fig. 4 Circuit diagram of a 4 W amplifier.

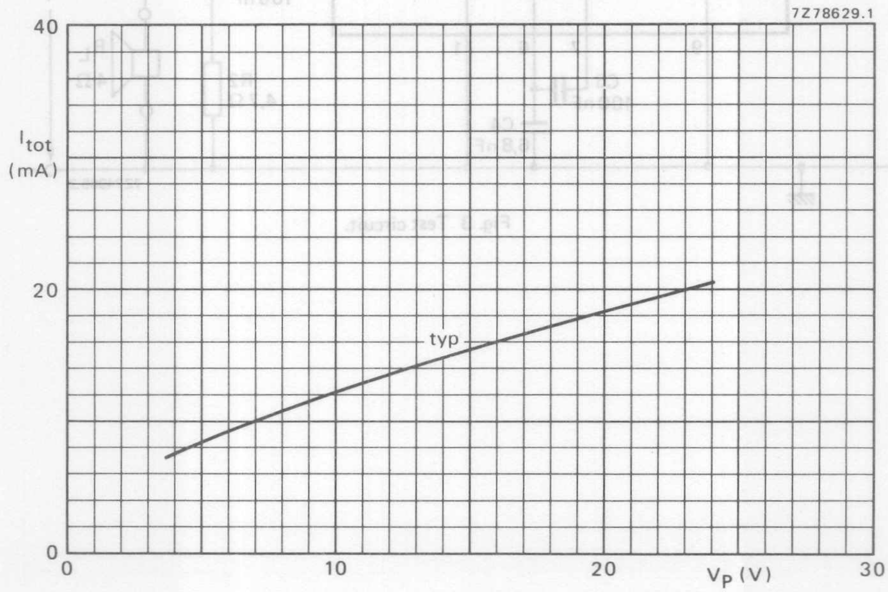



Fig. 5 Total quiescent current as a function of supply voltage.

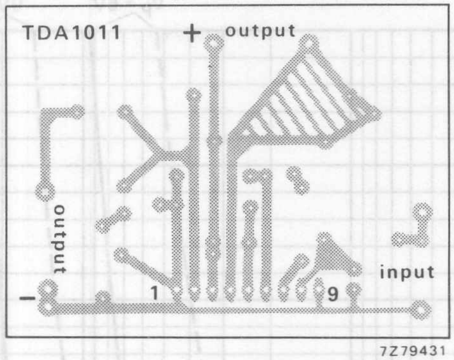



Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4;
p.c. board dimensions 62 mm x 48 mm.

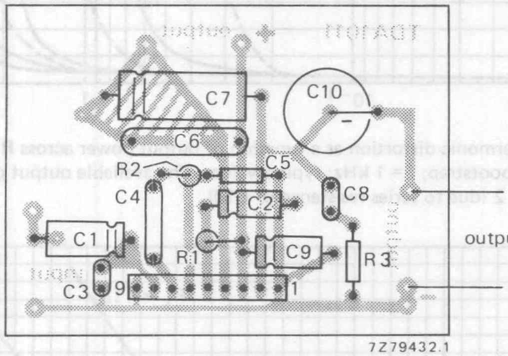



Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

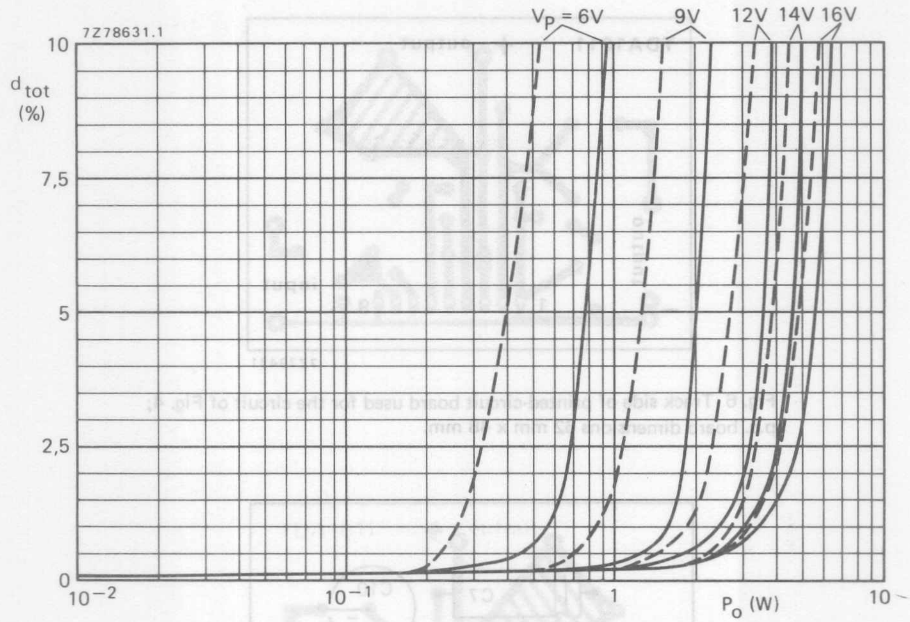



Fig. 8 Total harmonic distortion as a function of output power across $R_L$; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

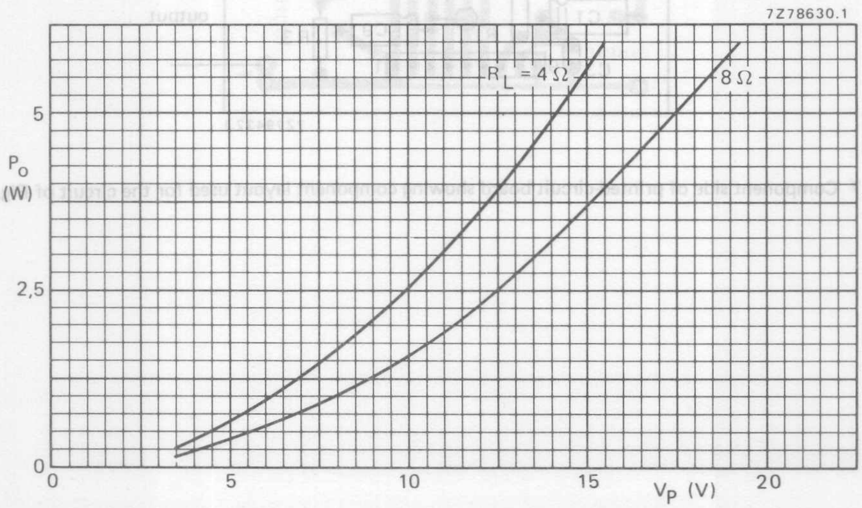



Fig. 9 Output power across $R_L$ as a function of supply voltage with bootstrap; $d_{tot}$ = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

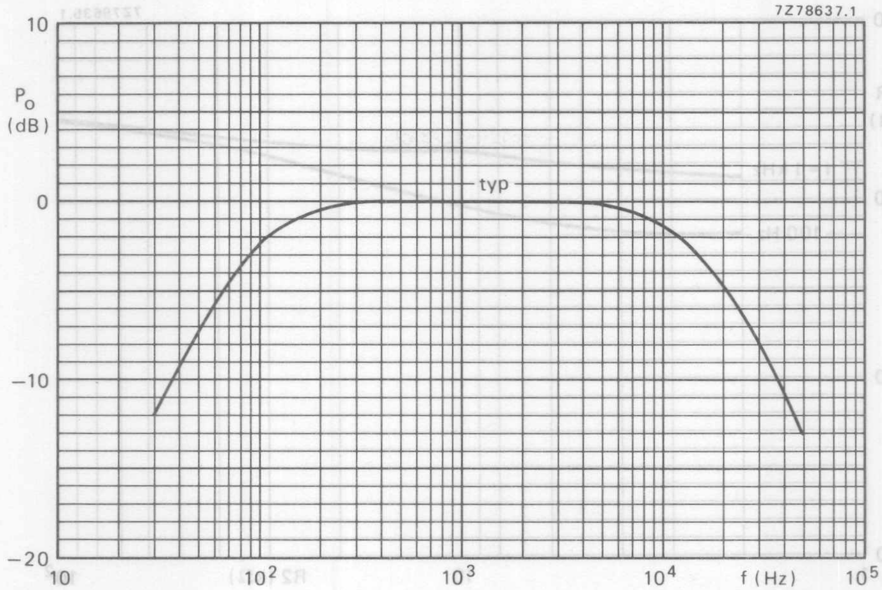



Fig. 10 Voltage gain as a function of frequency; $P_o$ relative to 0 dB = 1 W; $V_P$ = 12 V; $R_L$ = 4 Ω.

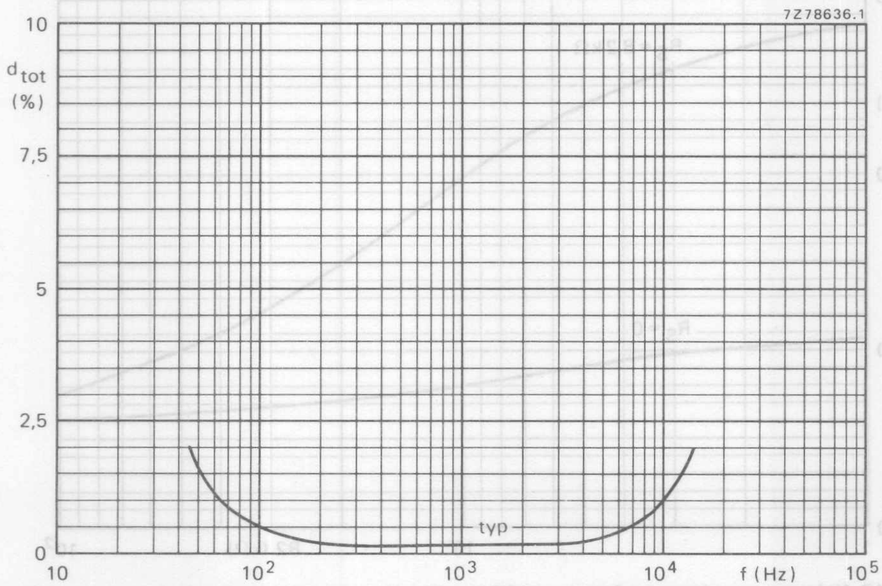



Fig. 11 Total harmonic distortion as a function of frequency; $P_o$ = 1 W; $V_P$ = 12 V; $R_L$ = 4 Ω.

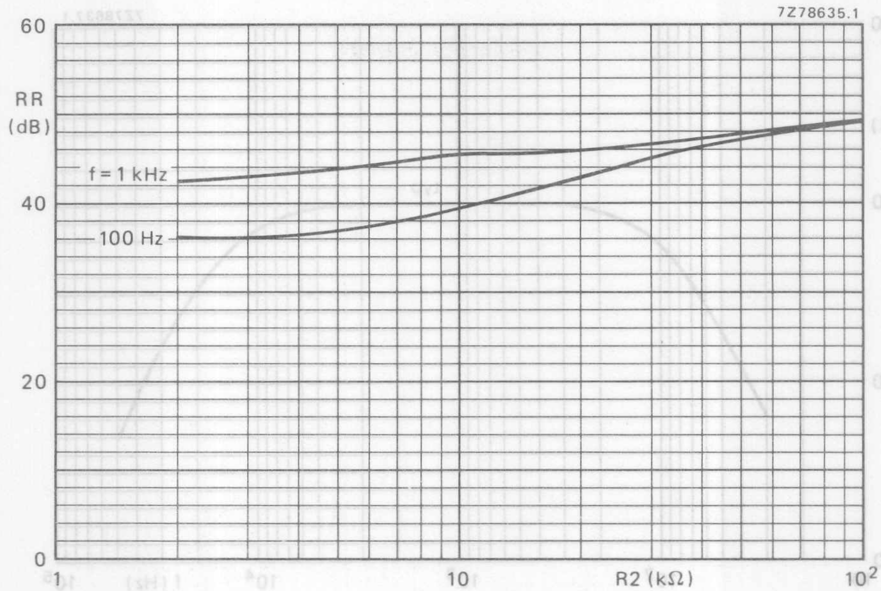



Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

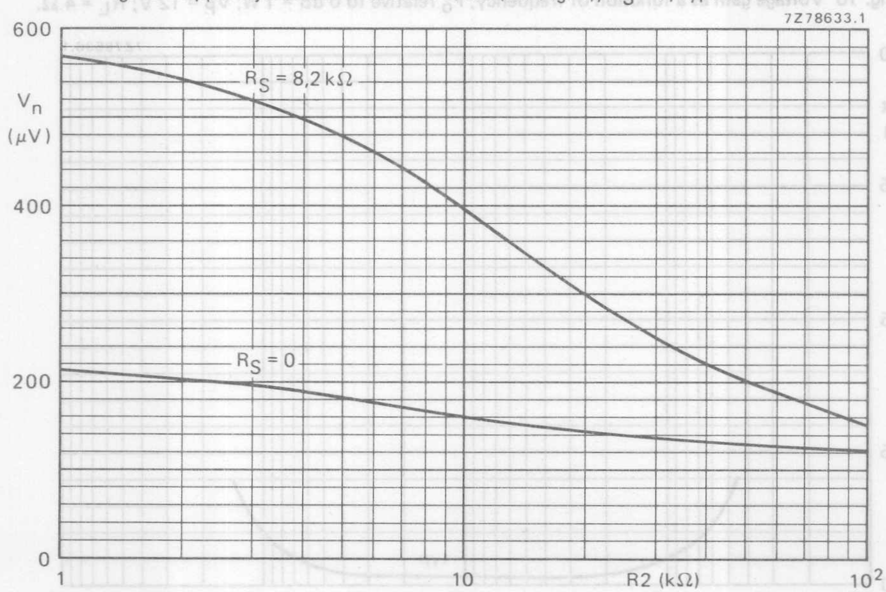



Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

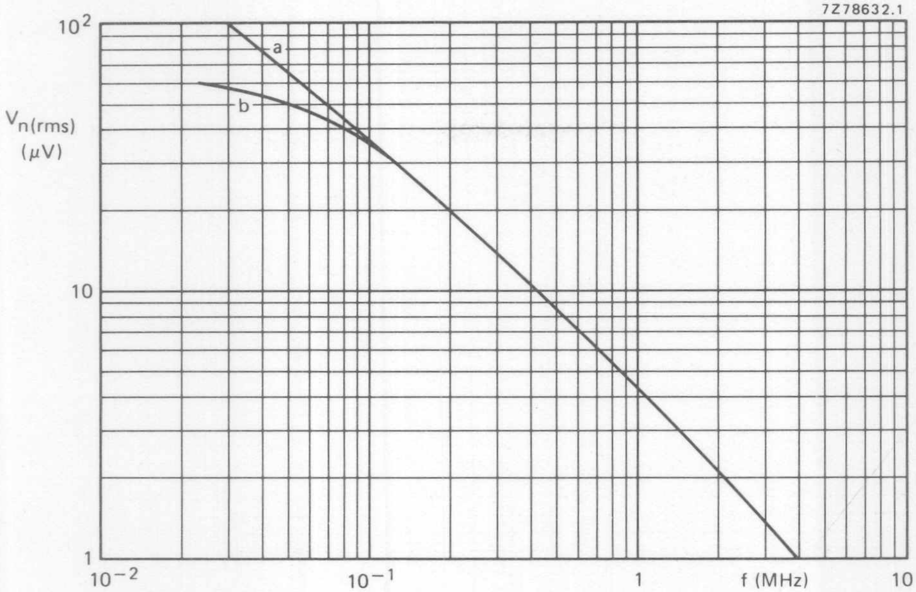



Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; $R_S$ = 0; typical values.

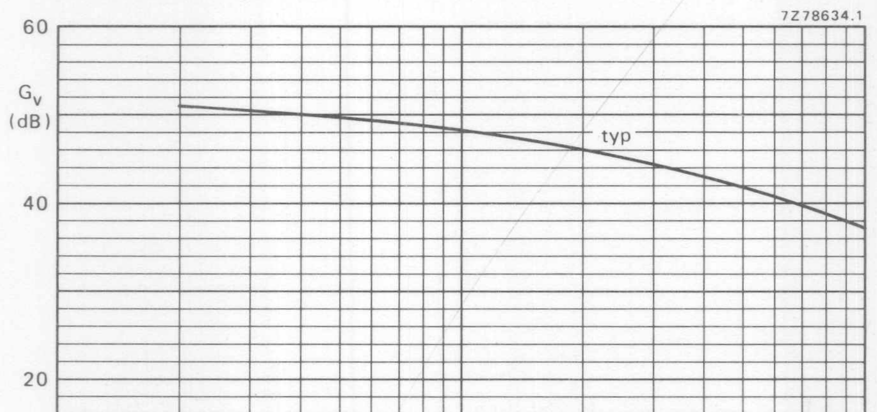



Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

# 2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 5,4 to 20 | V |
| Peak output current | $I_{OM}$ | max. | 3 | A |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 16 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6,5 | W |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| Total harmonic distortion at $P_o$ = 1 W; $R_L$ = 4 Ω | $d_{tot}$ | typ. | 0,2 | % |
| Input impedance preamplifier (pin 8) | $\lvert Z_i \rvert$ | > | 100 | kΩ |
| Total quiescent current | $I_{tot}$ | typ. | 14 | mA |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

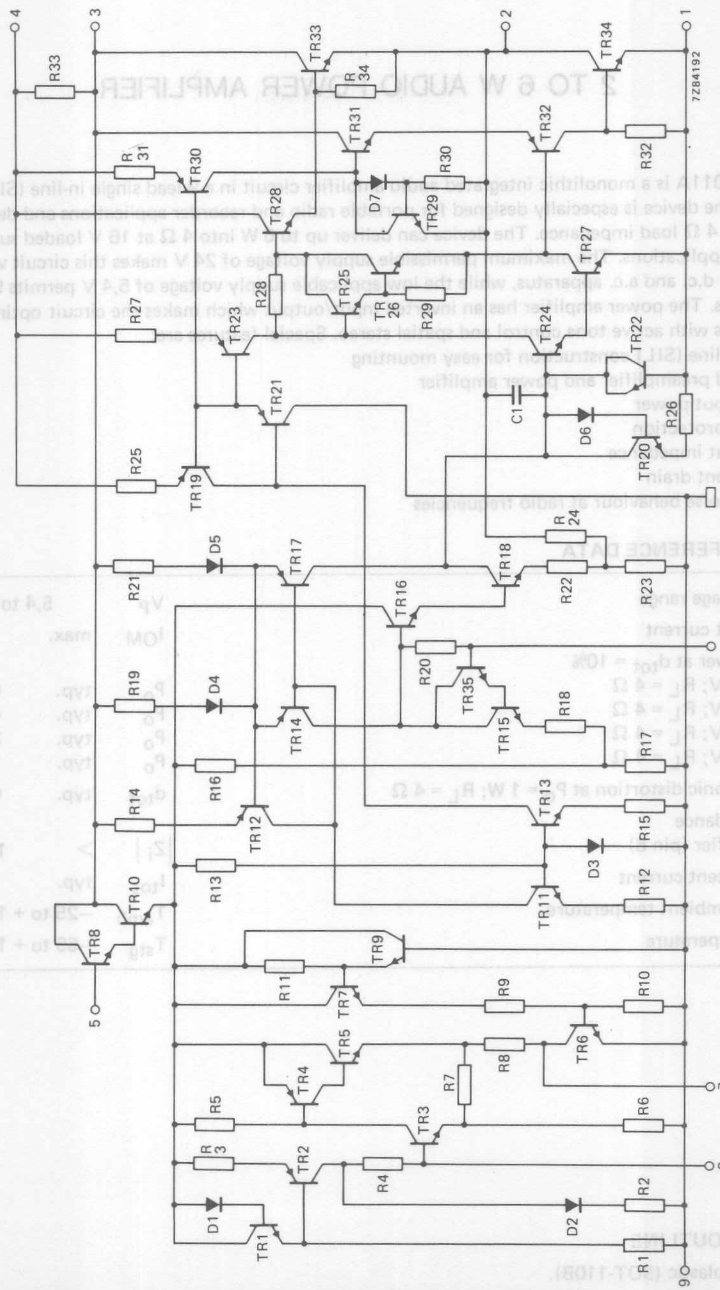


Fig. 1 Circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 24 V |
| Peak output current | $I_{OM}$ | max. | 3 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during sine-wave drive; $V_P$ = 12 V | $t_{sc}$ | max. | 100 hours |

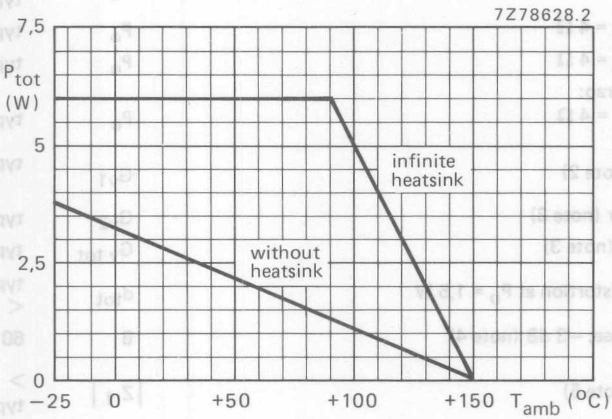



Fig. 2 Power derating curve.

## HEATSINK DESIGN

Assume $V_P$ = 12 V; $R_L$ = 4 Ω; $T_{amb}$ = 60 °C maximum; $P_o$ = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{1,8} = 50\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 5,4 to 20 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 2 | A |
| Total quiescent current at $V_P$ = 12 V | $I_{tot}$ | typ. | 14 | mA |
| | | < | 22 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 12 V; $R_L$ = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

| | | | | |
|---|---|---|---|---|
| A.F. output power at $d_{tot}$ = 10% (note 1) | | | | |
| with bootstrap: | | | | |
| $V_P$ = 16 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6,5 | W |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | > | 3,6 | W |
| | | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| without bootstrap: | | | | |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 3,5 | W |
| Voltage gain: | | | | |
| preamplifier (note 2) | $G_{v1}$ | typ. | 23 | dB |
| | | | 21 to 25 | dB |
| power amplifier (note 3) | $G_{v2}$ | typ. | 29 | dB |
| total amplifier (note 3) | $G_{v\,tot}$ | typ. | 52 | dB |
| Total harmonic distortion at $P_o$ = 1,5 W | $d_{tot}$ | typ. | 0,3 | % |
| | | < | 1 | % |
| Frequency response; −3 dB (note 4) | B | | 60 Hz to 15 | kHz |
| Input impedance: | | | | |
| preamplifier (note 5) | $\lvert Z_{i1} \rvert$ | > | 100 | kΩ |
| | | typ. | 200 | kΩ |
| Output impedance preamplifier | $\lvert Z_{o1} \rvert$ | typ. | 1 | kΩ |
| Output voltage preamplifier (r.m.s. value) | | | | |
| $d_{tot}$ < 1% (note 2) | $V_{o(rms)}$ | > | 1,2 | V |
| Noise output voltage (r.m.s. value; note 6) | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,5 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,8 | mV |
| Noise output voltage at f = 500 kHz (r.m.s. value) | | | | |
| B = 5 kHz; $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 8 | μV |
| Ripple rejection (note 6) | | | | |
| f = 1 to 10 kHz | RR | typ. | 42 | dB |
| f = 100 Hz; C2 = 1 μF | RR | > | 35 | dB |
| Bootstrap current at onset of clipping; pin 4 (r.m.s. value) | $I_{4(rms)}$ | typ. | 35 | mA |
| Stand-by current at maximum $V_P$ (note 8) | $I_{sb}$ | < | 100 | μA |

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at $P_o$ = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

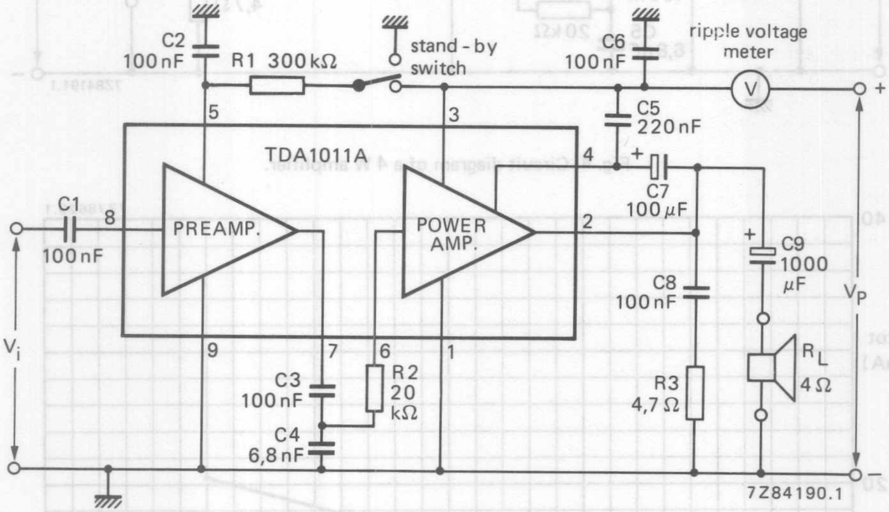



Fig. 3 Test circuit.

## APPLICATION INFORMATION

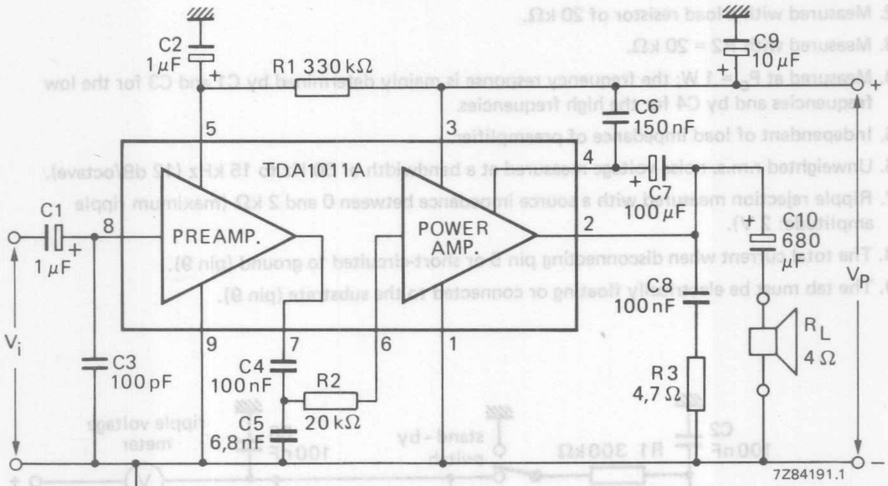



Fig. 4 Circuit diagram of a 4 W amplifier.


Fig. 5 Total quiescent current as a function of supply voltage.

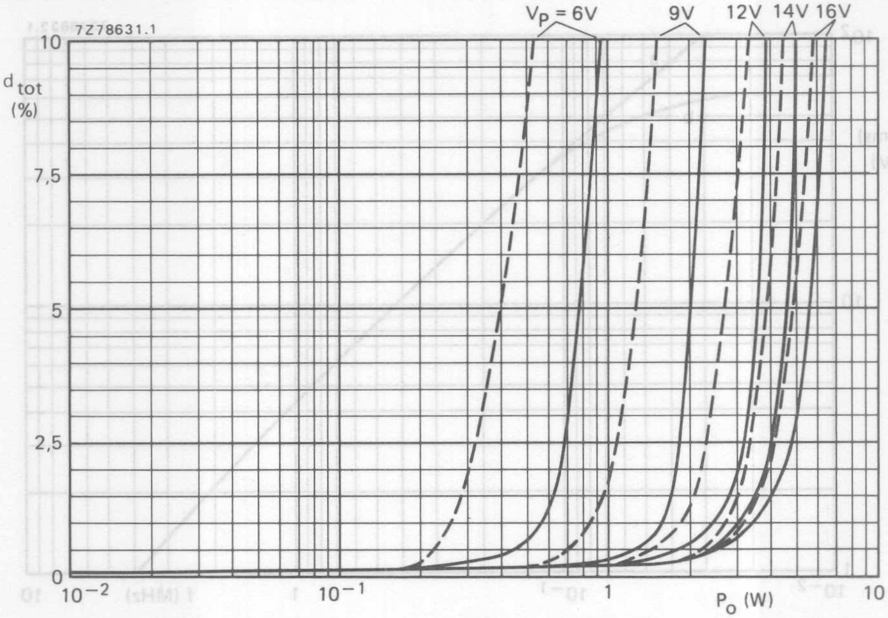



Fig. 6 Total harmonic distortion as a function of output power across $R_L$; ——— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

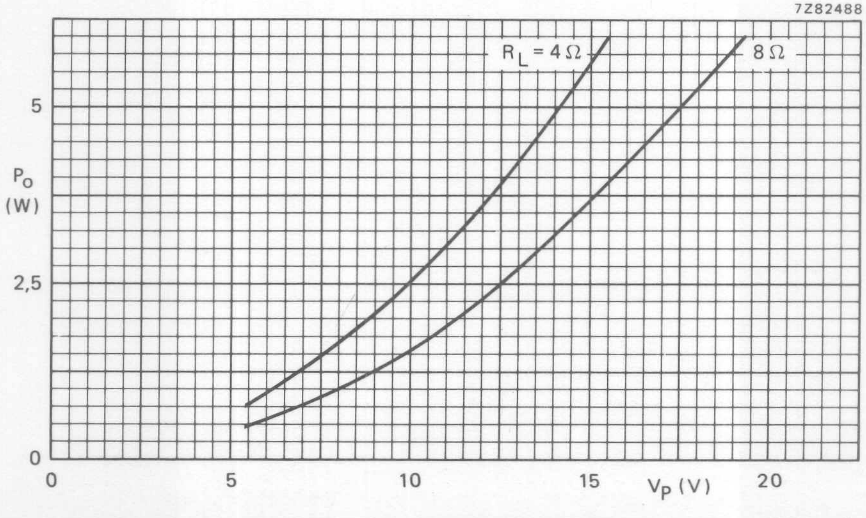



Fig. 7 Output power across $R_L$ as a function of supply voltage with bootstrap; $d_{tot}$ = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C1

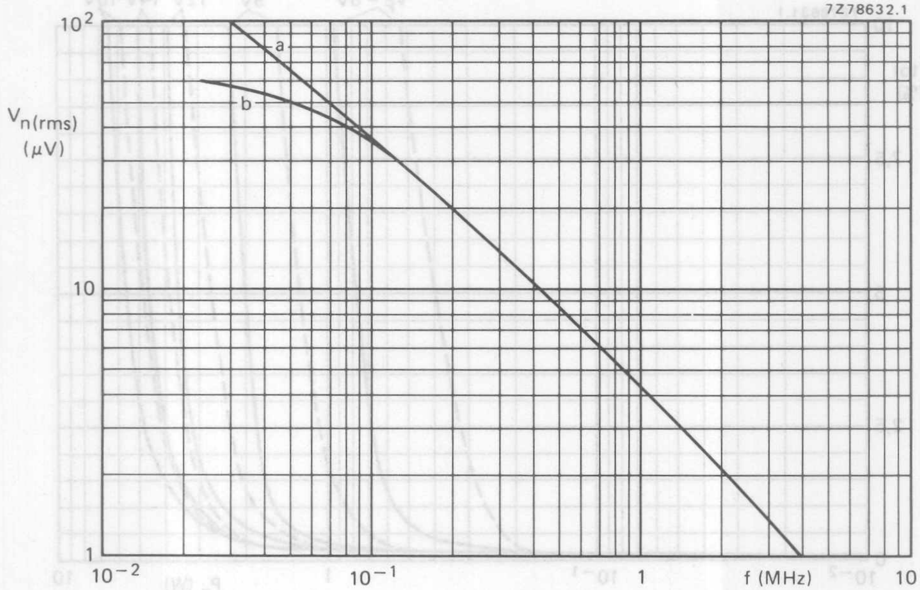



Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; $R_S$ = 0; typical values.

# RECORDING / PLAY-BACK AND 2 W AUDIO POWER AMPLIFIER

The TDA1012 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit is thermal protected and contains the following functions:

- Power amplifier
- Preamplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 18 | V |
| Total quiescent current at $V_P = 9$ V | $I_{tot}$ | typ. | 14 | mA |
| **Power amplifier** | | | | |
| Output power at $d_{tot} = 10$ %<br>$V_P = 9$ V; $R_L = 4\ \Omega$ | $P_o$ | typ. | 2 | W |
| Closed loop voltage gain | $G_c$ | typ. | 36 | dB |
| **Preamplifier** | | | | |
| Open loop voltage gain | $G_o$ | > | 66 | dB |
| Minimum closed loop voltage gain | $G_{c\,min}$ | | 31 | dB |
| Output voltage at $d_{tot} = 1$ % | $V_o$ | > | 2 | V |
| **Automatic Level Control (A.L.C.)** | | | | |
| Gain variation for $\Delta V_i = 40$ dB | $\Delta G_v$ | typ. | 2 | dB |
| **Stabilized supply voltage** | | | | |
| Output voltage | $V_{11\text{-}15}$ | typ. | 4,2 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).

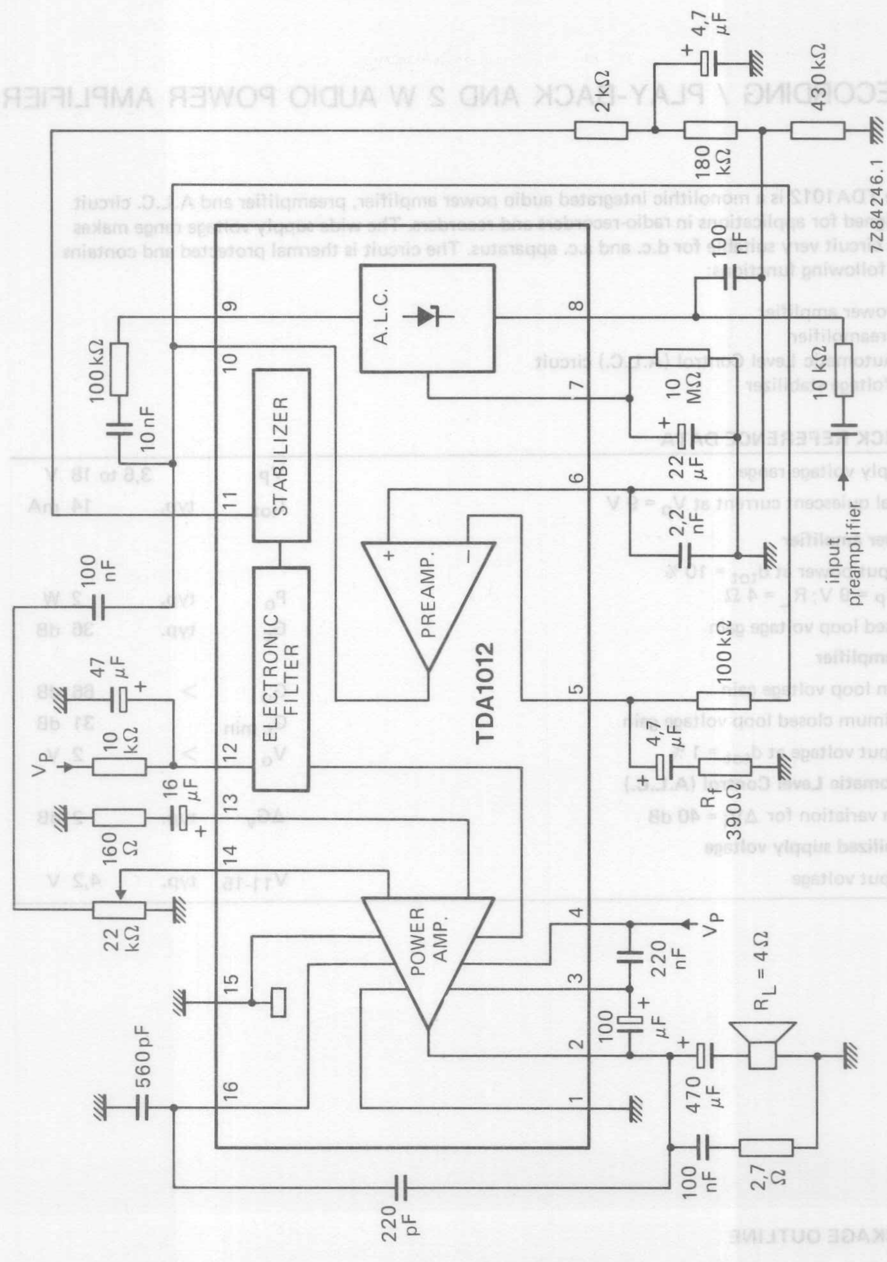



Fig. 1 Block diagram/test circuit.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 4) | $V_P = V_{4\text{-}1}$ | max. | 18 V |
| Non-repetitive peak output current (pin 2) | $I_{OSM}$ | max. | 2 A |
| Storage temperature | $T_{stg}$ | | −55 to +150 °C |
| Crystal temperature | $T_c$ | max. | 150 °C |
| Total power dissipation | see derating curve Fig. 2 | | |
| A.C. short-circuit duration of load during sine-wave drive; $V_P$ = 12 V | $t_{sc}$ | max. | 100 hours |

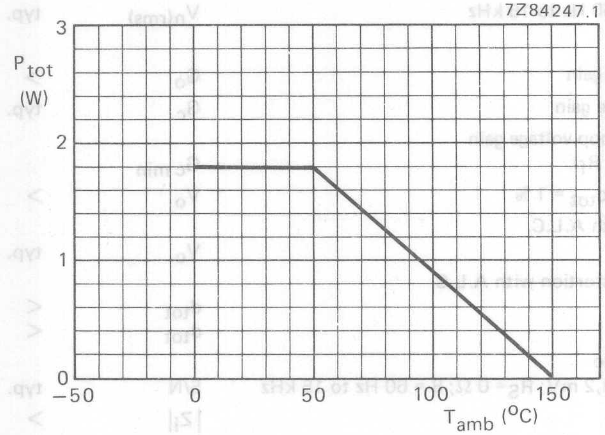



Fig. 2 Power derating curve.

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to ambient | $R_{th\,j\text{-}a}$ | = | 55 K/W |

## CHARACTERISTICS

$V_P = 9$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in test circuit of Fig. 1; unless otherwise specified.

| | | | |
|---|---|---|---|
| **Power amplifier** | | | |
| Output power at $d_{tot} = 10$ % | $P_o$ | typ. | 2 W |
| Closed loop voltage gain | $G_c$ | typ. | 36 dB |
| Total harmonic distortion at $P_o = 1W$ | $d_{tot}$ | < | 1 % |
| Input impedance | $\|Z_i\|$ | > | 1 MΩ |
| Ripple rejection at f = 100 Hz | RR | > | 40 dB |
| Noise output voltage (r.m.s. value) $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz | $V_{n(rms)}$ | typ. | 150 μV |
| **Preamplifier** | | | |
| Open loop voltage gain | $G_o$ | > | 66 dB |
| Closed loop voltage gain | $G_c$ | typ. | 48 dB |
| Minimum closed loop voltage gain (when changing $R_f$) | $G_{c\ min}$ | | 31 dB |
| Output voltage at $d_{tot} = 1$ % | $V_o$ | > | 2 V |
| Output voltage with A.L.C. $V_i = 4{,}8$ mV | $V_o$ | typ. | 1,1 V |
| Total harmonic distortion with A.L.C. | | | |
| $V_i = 4{,}8$ mV | $d_{tot}$ | < | 1 % |
| $V_i = 480$ mV | $d_{tot}$ | < | 3 % |
| Signal-to-noise ratio related to $V_i = 1{,}2$ mV; $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz | S/N | typ. | 60 dB |
| Input impedance | $\|Z_i\|$ | > | 100 kΩ |
| Ripple rejection at f = 100 Hz | RR | > | 52 dB |
| Output impedance | $\|Z_o\|$ | < | 50 Ω |
| **Automatic Level Control (A.L.C.)** | | | |
| Gain variation for $\Delta V_i = 40$ dB | $\Delta G_v$ | typ. | 2 dB |
| Limiting time at $\Delta V_i = 40$ dB | $t_l$ | < | 50 ms |
| Level setting time at $\Delta V_i = 40$ dB | $t_s$ | < | 50 ms |
| Recovery time at $\Delta V_i = 40$ dB | $t_r$ | typ. | 100 s |
| **Voltage stabilizer** | | | |
| Output voltage | $V_{11\text{-}15}$ | typ. | 4,2 V |
| Load current | $I_{11}$ | < | 1 mA |
| Ripple rejection at f = 100 Hz | RR | > | 40 dB |

# 4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

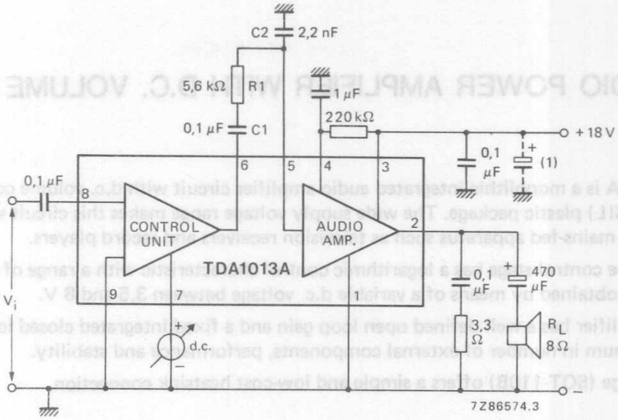
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 1,5 A |
| Total sensitivity (d.c. control at max. gain) for $P_o$ = 2,5 W | $V_i$ | typ. | 55 mV |
| **Audio amplifier** | | | |
| Output power at $d_{tot}$ = 10% $V_P$ = 18 V; $R_L$ = 8 Ω | $P_o$ | typ. | 4,5 W |
| Total harmonic distortion at $P_o$ = 2,5 W; $R_L$ = 8 Ω | $d_{tot}$ | typ. | 0,5 % |
| Sensitivity for $P_o$ = 2,5 W | $V_i$ | typ. | 125 mV |
| **D.C. volume control unit** | | | |
| Gain control range | $\phi$ | > | 80 dB |
| Signal handling at $d_{tot}$ < 1% (d.c. control at 0 dB) | $V_i$ | > | 1,2 V |
| Sensitivity for $V_o$ = 125 mV at max. voltage gain | $V_i$ | typ. | 55 mV |
| Input impedance (pin 8) | $\lvert Z_i \rvert$ | typ. | 250 kΩ |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).




(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with R1 = 5,1 kΩ and C1 = 22 nF.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 35 V |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 3 A |
| Repetitive peak output current | $I_{ORM}$ | max. | 1,5 A |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Crystal temperature | $T_j$ | | −25 to + 150 °C |
| Total power dissipation | see derating curve Fig. 2 | | |

## HEATSINK DESIGN

Assume $V_P$ = 18 V; $R_L$ = 8 Ω; $T_{amb}$ = 60 °C (max.); $T_j$ = 150 °C (max); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 − (9 + 1) = 26 K/W.

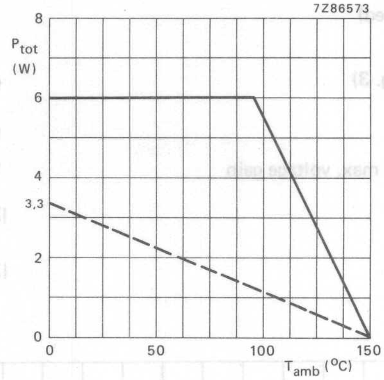



Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

## CHARACTERISTICS

$V_P$ = 18 V; $R_L$ = 8 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | typ. | 18 | V |
| | | | 15 to 35 | V |
| Total quiescent current | $I_{tot}$ | typ. | 35 | mA |
| Noise output voltage (see also note) | $V_n$ | < | 1,4 | mV |
| Total sensitivity (d.c. control at maximum gain) for $P_o$ = 2,5 W | $V_i$ | | 38 to 69 | mV |
| | | typ. | 55 | mV |
| Frequency response (−3 dB) | f | | 35 Hz to 20 | kHz |

**Audio amplifier**

| | | | | |
|---|---|---|---|---|
| Repetitive peak output current | $I_{ORM}$ | < | 1,5 | A |
| Output power at $d_{tot}$ = 10% | $P_o$ | > | 4 | W |
| | | typ. | 4,5 | W |
| Total harmonic distortion at $P_o$ = 2,5 W | $d_{tot}$ | typ. | 0,5 | % |
| | | < | 1 | % |
| Voltage gain | $G_v$ | typ. | 30 | dB |
| Sensitivity for $P_o$ = 2,5 W | $V_i$ | typ. | 125 | mV |
| Input impedance (pin 5) | $\|Z_i\|$ | > | 100 | kΩ |
| | | typ. | 250 | kΩ |

**Note**

Measured in a bandwidth according to IEC 179-curve 'A'; $R_S$ = 5 kΩ and d.c. control at minimum gain.

CHARACTERISTICS (continued)

**D.C. volume control unit**

| | | | | |
|---|---|---|---|---|
| Gain control range (see also Fig. 3) | $\phi$ | > | 80 | dB |
| Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB) | $V_i$ | > | 1,2 | V |
| Sensitivity for $V_o$ = 125 mV at max. voltage gain | $V_i$ | typ. | 55 | mV |
| Input impedance (pin 8) | $\|Z_i\|$ | > | 100 | kΩ |
| | | typ. | 250 | kΩ |
| Output impedance (pin 6) | $\|Z_o\|$ | | 100 to 400 | Ω |
| | | typ. | 200 | Ω |

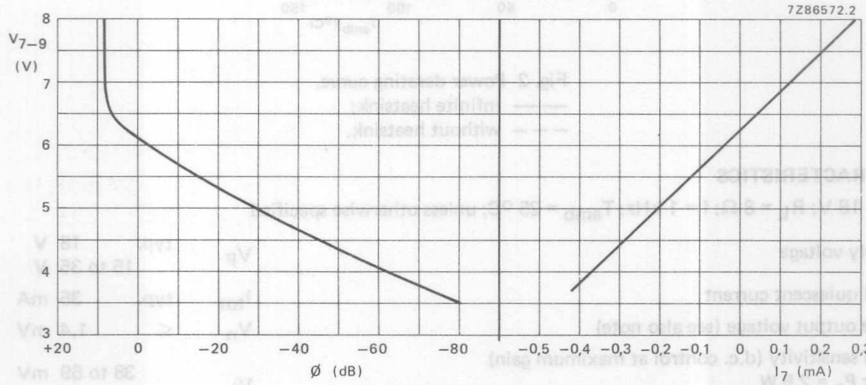



Fig. 3 Typical values gain control; $V_i$ at pin 7.

# 1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 18 | V |
| Peak output current | $I_{OM}$ | max. | 2,5 | A |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| Total harmonic distortion at $P_o$ = 1 W; $R_L$ = 4 Ω | $d_{tot}$ | typ. | 0,3 | % |
| Input impedance | | | | |
| preamplifier (pin 8) | $\|Z_i\|$ | > | 100 | kΩ |
| power amplifier (pin 6) | $\|Z_i\|$ | typ. | 20 | kΩ |
| Total quiescent current | $I_{tot}$ | typ. | 14 | mA |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

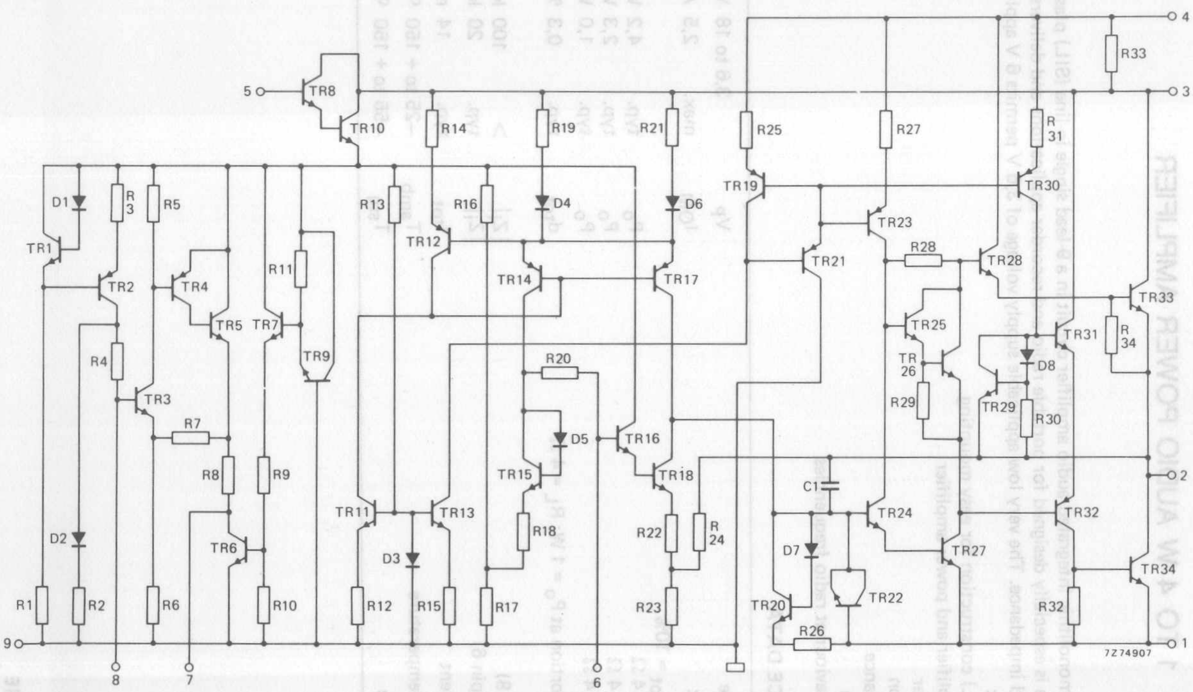



Fig. 1 Circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 18 V |
| Peak output current | $I_{OM}$ | max. | 2,5 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during sine-wave drive; $V_P$ = 12 V | $t_{sc}$ | max. | 100 hours |

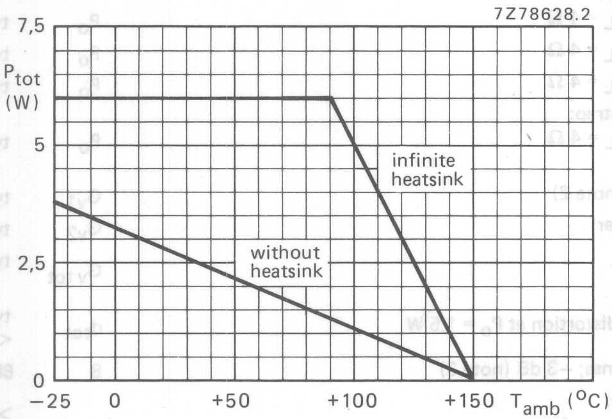



Fig. 2 Power derating curve.

## HEATSINK DESIGN

Assume $V_P$ = 12 V; $R_L$ = 4 Ω; $T_{amb}$ = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1{,}8} = 58\ \text{K/W}.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 18 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 2 | A |
| Total quiescent current at $V_P$ = 12 V | $I_{tot}$ | typ. | 14 | mA |
| | | < | 25 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 12 V; $R_L$ = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

| | | | | |
|---|---|---|---|---|
| A.F. output power at $d_{tot}$ = 10% (note 1) | | | | |
| with bootstrap: | | | | |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,2 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2,3 | W |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1,0 | W |
| without bootstrap: | | | | |
| $V_P$ = 12 V; $R_L$ = 4 Ω | $P_o$ | typ. | 3,0 | W |
| Voltage gain: | | | | |
| preamplifier (note 2) | $G_{v1}$ | typ. | 23 | dB |
| power amplifier | $G_{v2}$ | typ. | 29 | dB |
| total amplifier | $G_{v\,tot}$ | typ. | 52 | dB |
| | | | 49 to 55 | dB |
| Total harmonic distortion at $P_o$ = 1,5 W | $d_{tot}$ | typ. | 0,3 | % |
| | | < | 1,0 | % |
| Frequency response; −3 dB (note 3) | B | | 60 Hz to 15 | kHz |
| Input impedance: | | | | |
| preamplifier (note 4) | $\|Z_{i1}\|$ | > | 100 | kΩ |
| | | typ. | 200 | kΩ |
| power amplifier | $\|Z_{i2}\|$ | typ. | 20 | kΩ |
| Output impedance preamplifier | $\|Z_{o1}\|$ | typ. | 1 | kΩ |
| Output voltage preamplifier (r.m.s. value) | | | | |
| $d_{tot}$ < 1% (note 2) | $V_{o(rms)}$ | typ. | 0,8 | V |
| Noise output voltage (r.m.s. value; note 5) | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,2 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,5 | mV |
| Noise output voltage at f = 500 kHz (r.m.s. value) | | | | |
| B = 5 kHz; $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 8 | μV |
| Ripple rejection (note 6) | | | | |
| f = 100 Hz | RR | typ. | 38 | dB |

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at $P_o$ = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

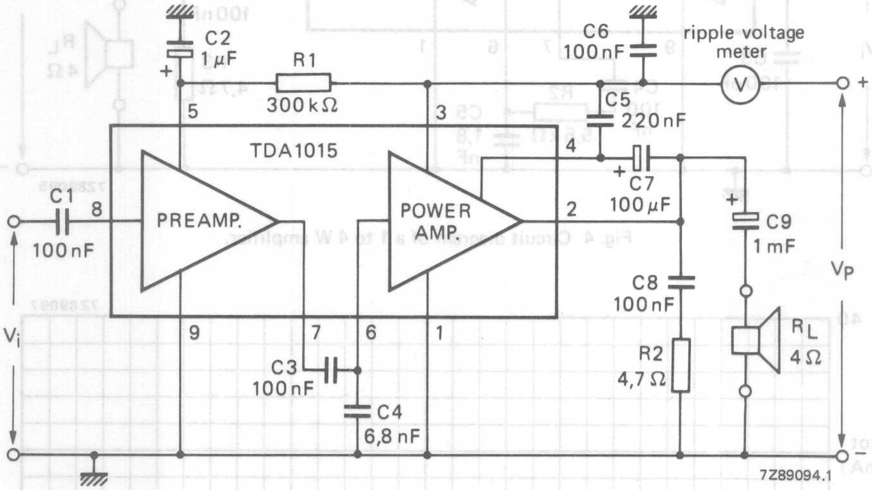



Fig. 3 Test circuit.

## APPLICATION INFORMATION

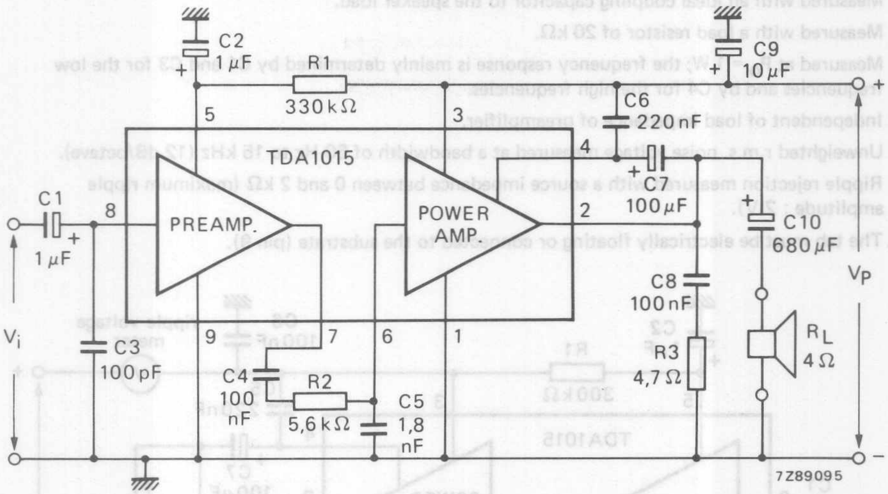



Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

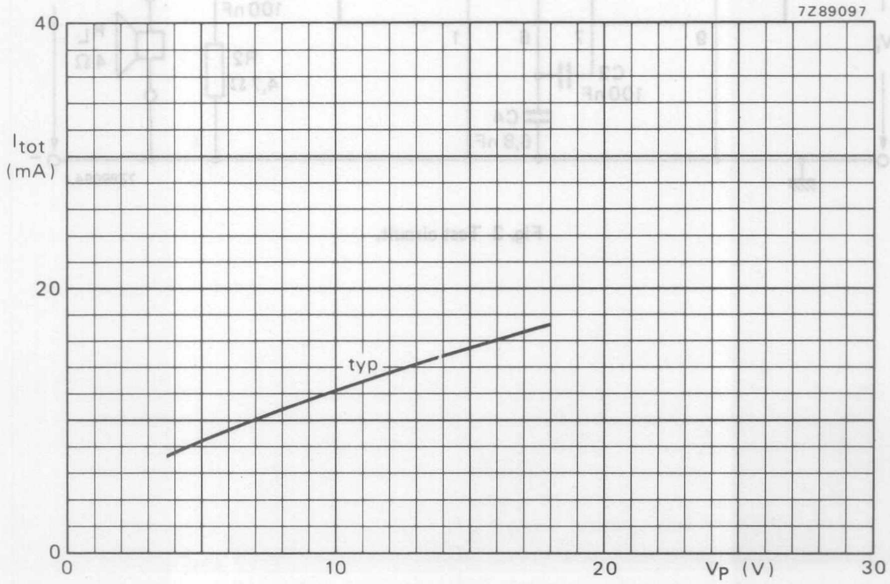



Fig. 5 Total quiescent current as a function of supply voltage.

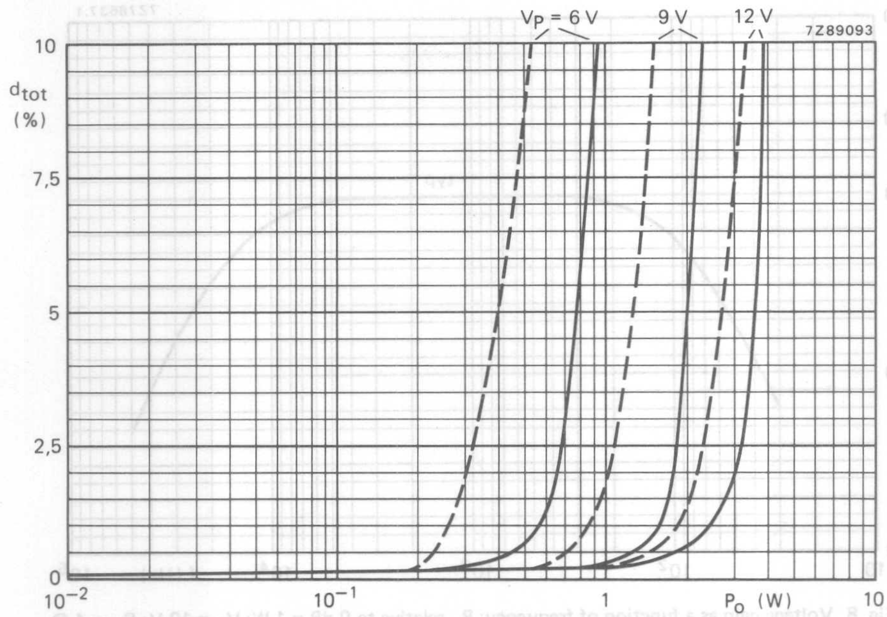



Fig. 6 Total harmonic distortion as a function of output power across $R_L$; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

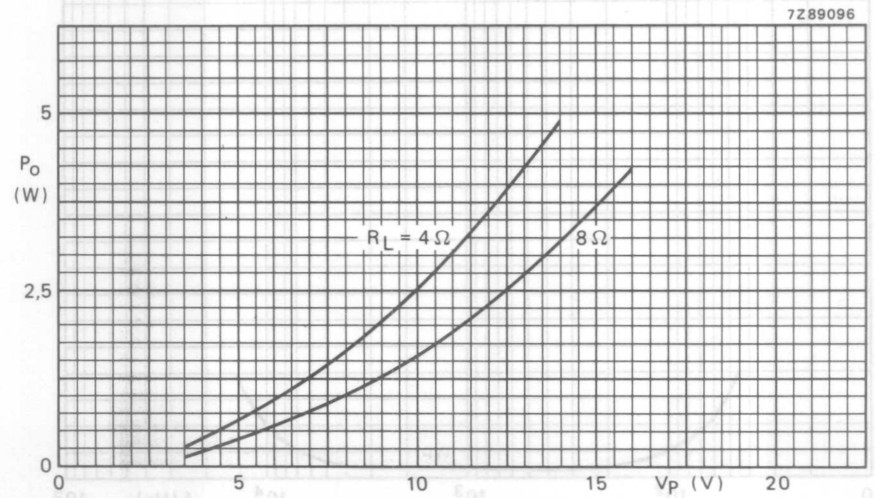



Fig. 7 Output power across $R_L$ as a function of supply voltage with bootstrap; $d_{tot}$ = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

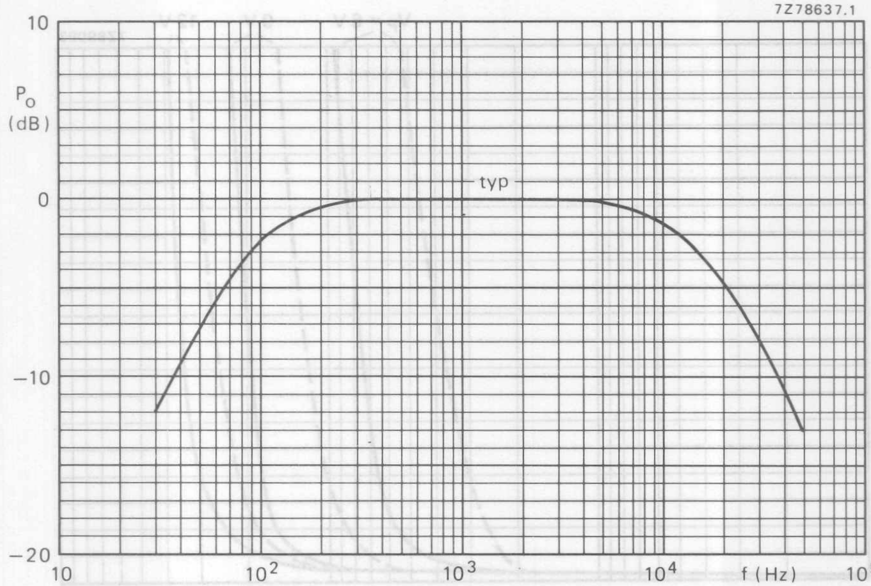



Fig. 8 Voltage gain as a function of frequency; $P_o$ relative to 0 dB = 1 W; $V_P$ = 12 V; $R_L$ = 4 Ω.

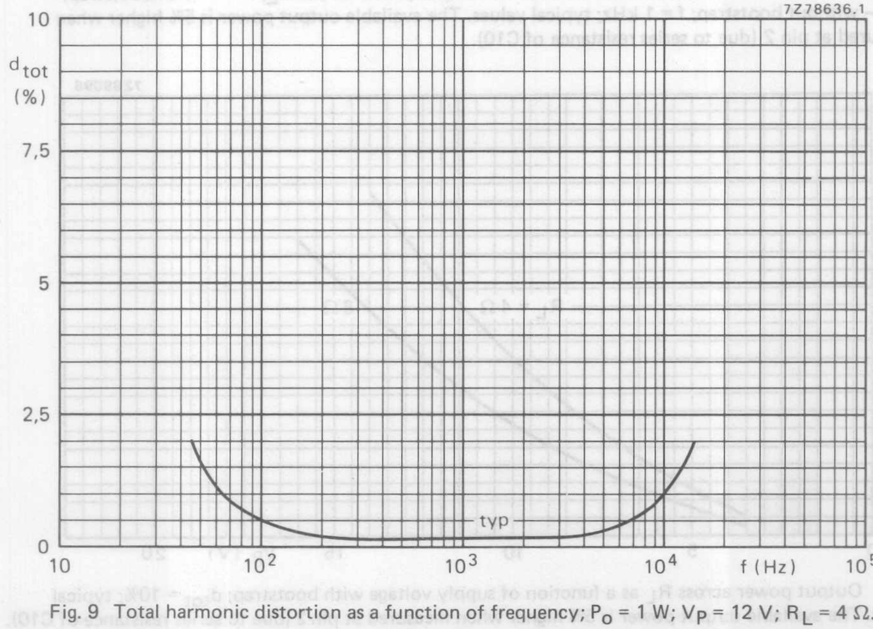



Fig. 9 Total harmonic distortion as a function of frequency; $P_o$ = 1 W; $V_P$ = 12 V; $R_L$ = 4 Ω.

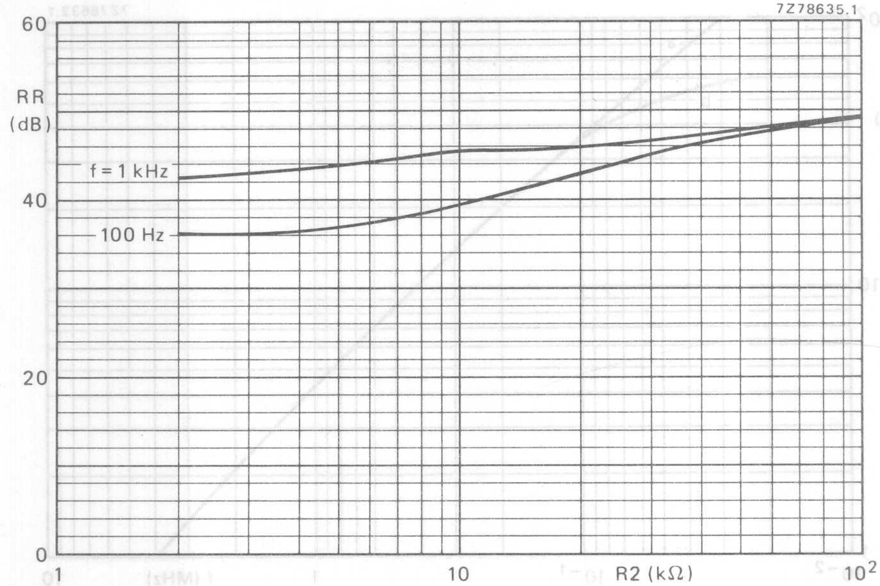



Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S$ = 0; typical values.

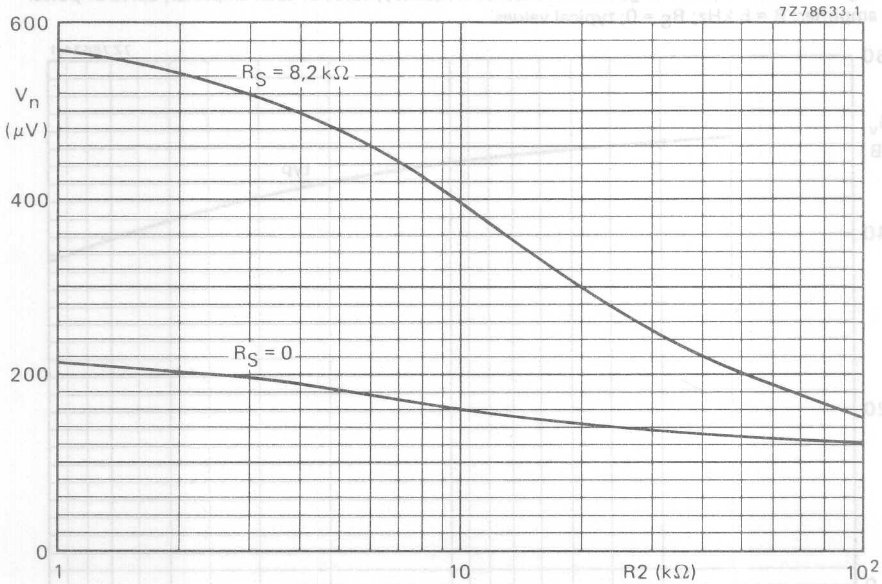



Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

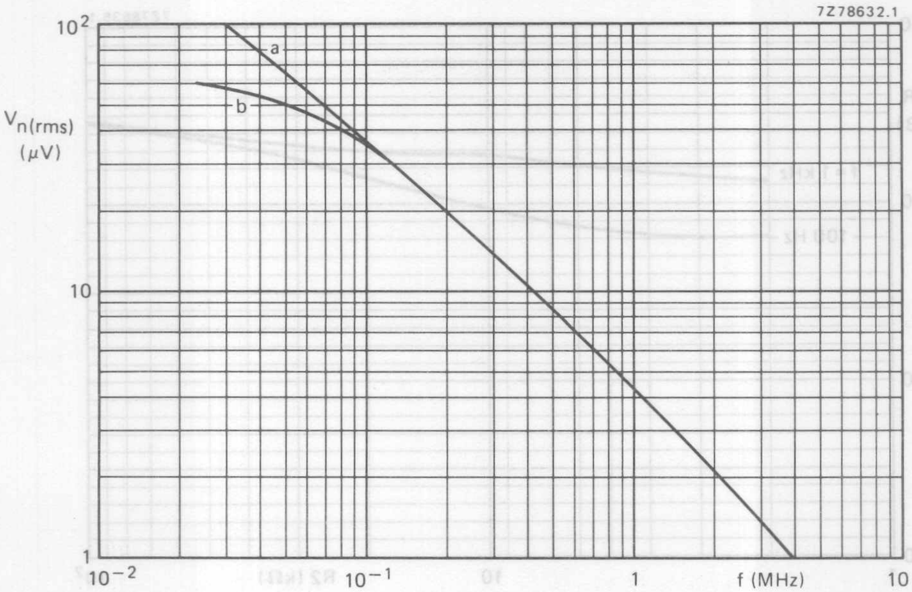



Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; $R_S$ = 0; typical values.

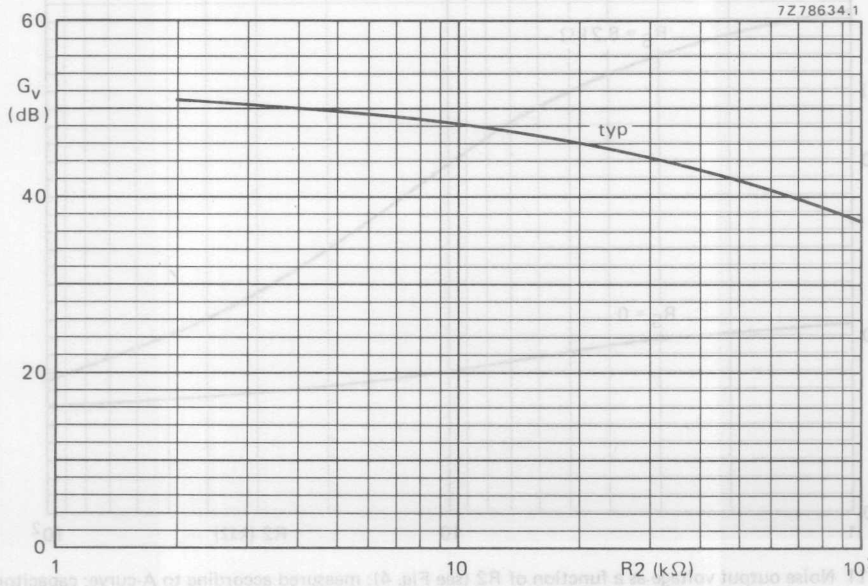



Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

# RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

## GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

**Features**

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 3,6 to 15 | V |
| Supply current; total quiescent at $V_P$ = 6 V | $I_{tot}$ | typ. | 10 | mA |
| Operating ambient temperature range | $T_{amb}$ | | −25 to 150 | °C |
| **Power amplifier** | | | | |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 6 V; $R_L$ = 4 Ω | $P_o$ | typ. | 1 | W |
| $V_P$ = 9 V; $R_L$ = 4 Ω | $P_o$ | typ. | 2 | W |
| Closed loop gain | $G_c$ | typ. | 36 | dB |
| **Preamplifier** | | | | |
| Open loop gain | $G_o$ | min. | 70 | dB |
| Minimum closed loop voltage gain | $G_{c\ min}$ | min. | 35 | dB |
| Output voltage at $d_{tot}$ = 1% | $V_o$ | min. | 1 | V |
| **Automatic Level Control (A.L.C.)** | | | | |
| Gain variation for $\Delta V_i$ = 40 dB | $\Delta G_v$ | typ. | 2 | dB |
| **Stabilized supply voltage** | | | | |
| Output voltage | $V_{5\text{-}16}$ | typ. | 2,6 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT-38WE-2).

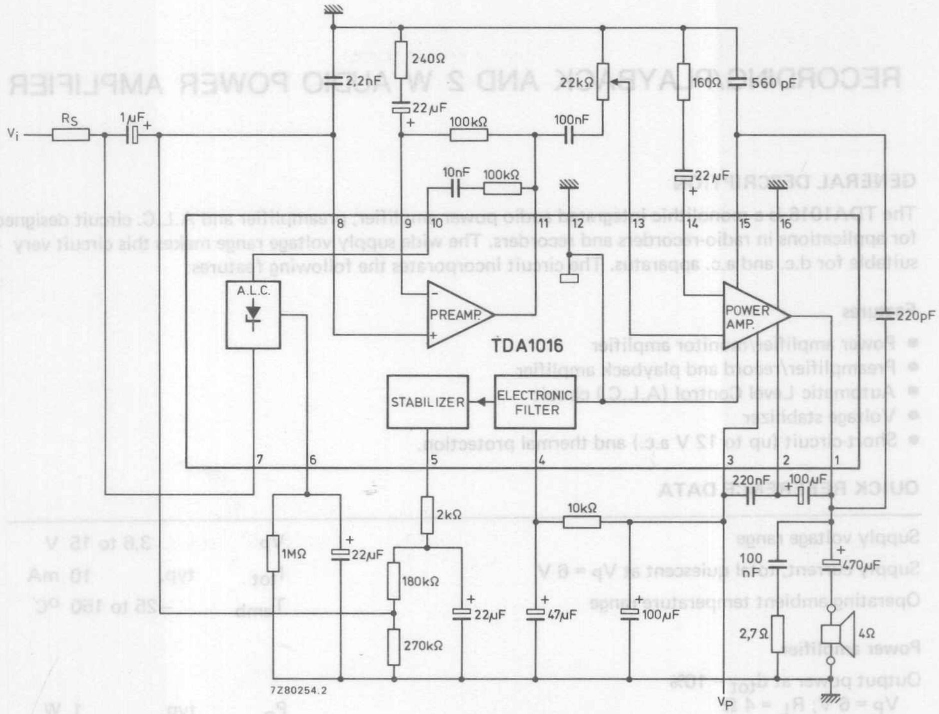



Fig. 1 Block diagram with external components; also used as test circuit.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 3) | $V_P$ | max. | 18 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 1 A |
| Non-repetitive peak output current (pin 1) | $I_{OSM}$ | max. | 2 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| A.C. short-circuit duration of load during sinewave drive; $V_P$ = 12 V | $t_{sc}$ | max. | 100 hours |
| Crystal temperature | $T_c$ | max. | 150 °C |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 150 °C |

## THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient $R_{th\ j\text{-}a}$ = 55 K/W

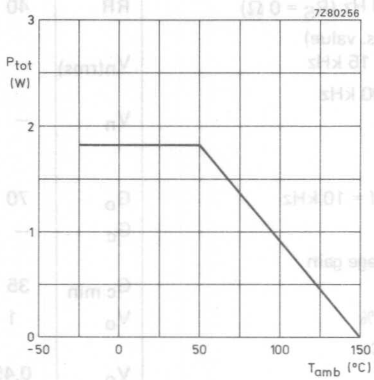



Fig. 2 Power derating curve.

## CHARACTERISTICS

$V_P$ = 6 V; $R_L$ = 4 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; measured in test circuit Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 3) | | | | | |
| Supply voltage | $V_P$ | 3,6 | 6 | 15 | V |
| Supply current; total quiescent at $V_P$ = 6 V | $I_{tot}$ | – | 10 | – | mA |
| **Power amplifier** | | | | | |
| Output power at $d_{tot}$ = 10%* | | | | | |
| $V_P$ = 6 V | $P_o$ | – | 1 | – | W |
| $V_P$ = 9 V | $P_o$ | – | 2 | – | W |
| Closed loop voltage gain | $G_c$ | – | 36 | – | dB |
| Total harmonic distortion at $P_o$ = 0,5 W | $d_{tot}$ | – | – | 1 | % |
| Input impedance | $\lvert Z_i \rvert$ | 0,5 | – | – | MΩ |
| Ripple rejection at f = 100 Hz ($R_S$ = 0 Ω) | RR | 40 | 50 | – | dB |
| Noise output voltage (r.m.s. value) $R_S$ = 0 Ω; B = 60 Hz to 15 kHz | $V_{n(rms)}$ | – | 90 | 200 | μV |
| Noise output voltage at 500 kHz $R_S$ = 0 Ω; B = 5 kHz | $V_n$ | – | 8 | – | μV |
| **Preamplifier** | | | | | |
| Open loop voltage gain at f = 10 kHz | $G_o$ | 70 | 78 | – | dB |
| Closed loop voltage gain | $G_c$ | – | 52 | – | dB |
| Minimum closed loop voltage gain (when changing $R_f$) | $G_{c\,min}$ | 35 | – | – | dB |
| Output voltage at $d_{tot}$ = 1% | $V_o$ | 1 | – | – | V |
| Output voltage with A.L.C. $V_i$ = 2 mV | $V_o$ | 0,45 | 0,5 | 0,55 | V |
| Total harmonic distortion with A.L.C. | | | | | |
| $V_i$ = 2 mV | $d_{tot}$ | – | – | 1 | % |
| $V_i$ = 360 mV | $d_{tot}$ | – | – | 3 | % |
| Signal-to-noise ratio related to $V_i$ = 1,2 mV; $R_S$ = 1 kΩ; B = 60 Hz to 15 kHz | S/N | – | 60 | – | dB |
| Input impedance | $\lvert Z_i \rvert$ | 100 | – | – | kΩ |
| Ripple rejection at f = 100 Hz; $R_S$ = 0 Ω | RR | 50 | 54 | – | dB |
| Output impedance ** | $\lvert Z_o \rvert$ | – | – | 50 | Ω |

* Measured with an ideal coupling capacitor connected to the speaker load.
** $I_P$ (effective value) must not exceed 1 mA.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Automatic Level Control (A.L.C.)** (see Fig. 3)** | | | | | |
| Gain variation for $\Delta V_i$ = 45 dB | $\Delta G_v$ | – | 2 | 3 | dB |
| Limiting time* | $t_l$ | – | – | 50 | ms |
| Level setting time* | $t_s$ | – | – | 50 | ms |
| Recovery time* ▲ | $t_r$ | – | 100 | – | s |
| **Voltage stabilizer** | | | | | |
| Output voltage | $V_{11\text{-}15}$ | – | 2,6 | – | V |
| Load current | $I_{11}$ | – | – | 1,5 | mA |
| Ripple rejection at f = 100 Hz | RR | 40 | – | – | dB |

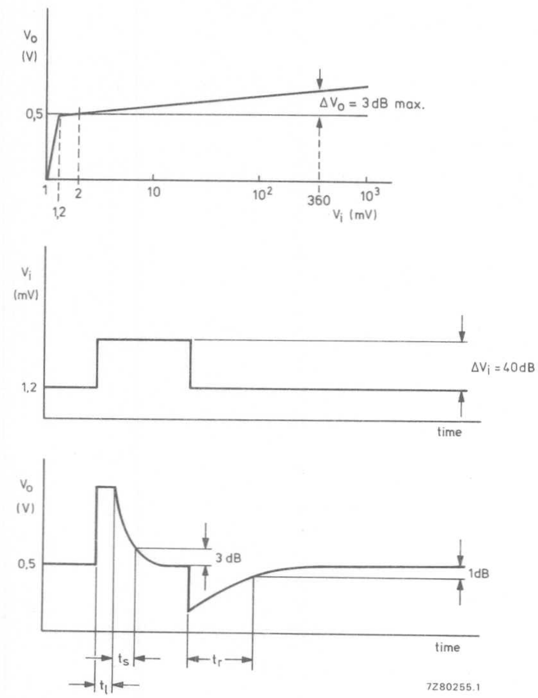



Fig. 3 Typical A.L.C. curve with $R_S$ = 10 kΩ.

* At $\Delta V_i$ = 40 dB with respect to $V_i$ = 1,2 mV.

** A.L.C. tracking in stereo anode pin 6 interconnected to an RC, time constant has a typical spread within 7 dB.

▲ Without a shunt resistor across A.L.C.
With 1 MΩ or 2,2 MΩ across A.L.C. recovery time becomes 22 or 50 seconds.

# 12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of $V_P$ = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 18 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 4 | A |
| Output power at $d_{tot}$ = 10% (with bootstrap) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | > | 10 | W |
| | | typ. | 12 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 7 | W |
| $V_P$ = 14,4 V; $R_L$ = 8 Ω | $P_o$ | typ. | 3,5 | W |
| Output power at $d_{tot}$ = 10% (without bootstrap) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | > | 4,5 | W |
| Input impedance | | | | |
| preamplifier (pin 8) | $\|Z_i\|$ | typ. | 40 | kΩ |
| power amplifier (pin 6) | $\|Z_i\|$ | typ. | 40 | kΩ |
| Total quiescent current at $V_P$ = 14,4 V | $I_{tot}$ | typ. | 30 | mA |
| Stand-by current | $I_{sb}$ | < | 1 | mA |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Crystal temperature | $T_c$ | max. | 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

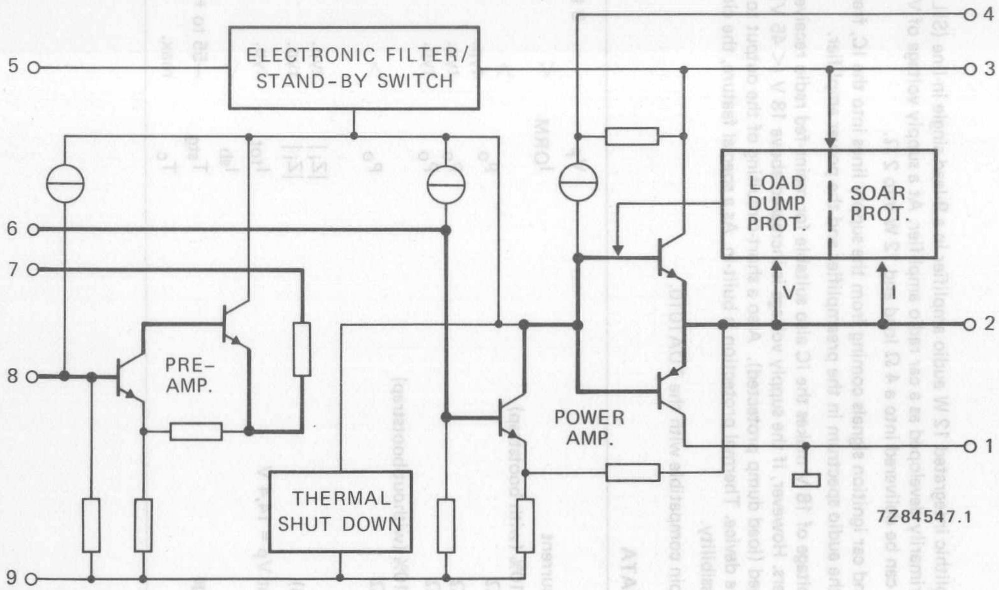



Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

## PINNING

| | | |
|---|---|---|
| 1. Negative supply (substrate) | 4. Bootstrap | 7. Output preamplifier |
| 2. Output power stage | 5. Ripple rejection filter | 8. Input preamplifier |
| 3. Positive supply ($V_P$) | 6. Input power stage | 9. Negative supply |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage; operating (pin 3) | $V_P$ | max. | 18 | V |
| Supply voltage; non-operating | $V_P$ | max. | 28 | V |
| Supply voltage; load dump | $V_P$ | max. | 45 | V |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 6 | A |
| Total power dissipation | see derating curves Fig. 2 | | | |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Crystal temperature | $T_c$ | max. | 150 | °C |
| Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); $V_P$ = 14,4 V | $t_{sc}$ | max. | 100 | hours |

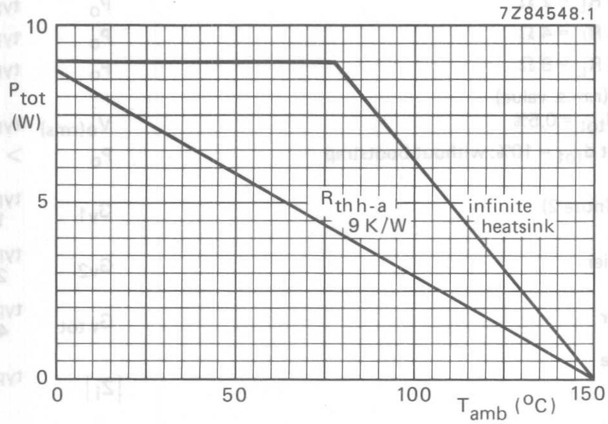



Fig. 2 Power derating curves.

## HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at $V_P$ = 14,4 V
maximum sine-wave dissipation: 5,2 W
$T_{amb}$ = 60 °C maximum

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{5,2} = 17,3\ \text{K/W}$$

Since $R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} = 8$ K/W, $R_{th\ h\text{-}a} = 17,3 - 8 \approx 9$ K/W.

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 3) | $V_P$ | | 6 to 18 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 4 | A |
| Total quiescent current | | | | |
| at $V_P$ = 14,4 V | $I_{tot}$ | typ. | 30 | mA |
| at $V_P$ = 18 V | $I_{tot}$ | typ. | 40 | mA |

## A.C. CHARACTERISTICS

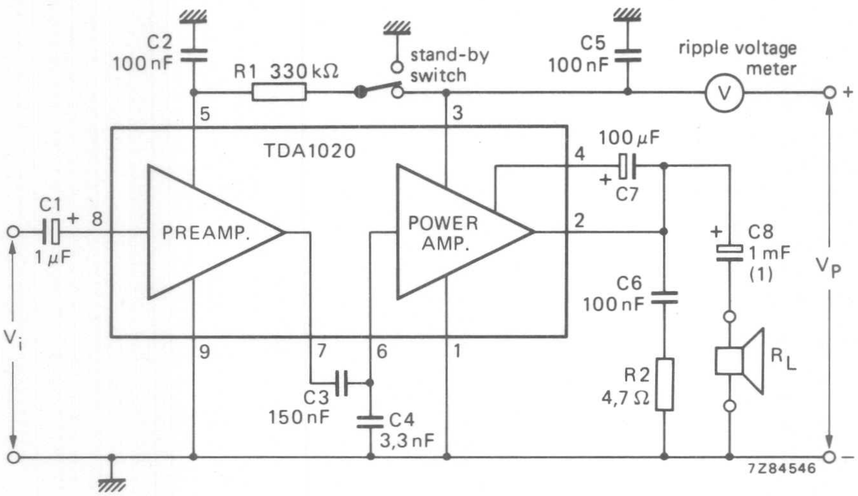
$T_{amb}$ = 25 °C; $V_P$ = 14,4 V; $R_L$ = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

| | | | | |
|---|---|---|---|---|
| Output power at $d_{tot}$ = 10%; with bootstrap (note 1) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | > | 10 | W |
| | | typ. | 12 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | > | 6 | W |
| | | typ. | 7 | W |
| $V_P$ = 14,4 V; $R_L$ = 8 Ω | $P_o$ | typ. | 3,5 | W |
| Output power at $d_{tot}$ = 1%; with bootstrap (note 1) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | typ. | 9,5 | W |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6 | W |
| $V_P$ = 14,4 V; $R_L$ = 8 Ω | $P_o$ | typ. | 3 | W |
| Output voltage (r.m.s. value) | | | | |
| $R_L$ = 1 kΩ; $d_{tot}$ = 0,5% | $V_{o(rms)}$ | typ. | 5 | V |
| Output power at $d_{tot}$ = 10%; without bootstrap | $P_o$ | > | 4,5 | W |
| Voltage gain | | | | |
| preamplifier (note 2) | $G_{v1}$ | typ. | 17,7 | dB |
| | | | 16,7 to 18,7 | dB |
| power amplifier | $G_{v2}$ | typ. | 29,5 | dB |
| | | | 28,5 to 30,5 | dB |
| total amplifier | $G_{v\,tot}$ | typ. | 47 | dB |
| | | | 46,2 to 48,2 | dB |
| Input impedance | | | | |
| preamplifier | $\lvert Z_i \rvert$ | typ. | 40 | kΩ |
| | | | 28 to 52 | kΩ |
| power amplifier | $\lvert Z_i \rvert$ | typ. | 40 | kΩ |
| | | | 28 to 52 | kΩ |
| Output impedance | | | | |
| preamplifier | $\lvert Z_o \rvert$ | typ. | 2,0 | kΩ |
| | | | 1,4 to 2,6 | kΩ |
| power amplifier | $\lvert Z_o \rvert$ | typ. | 50 | mΩ |
| Output voltage (r.m.s. value) at $d_{tot}$ = 1% | | | | |
| preamplifier (note 2) | $V_{o(rms)}$ | > | 1 | V |
| | | typ. | 1,5 | V |
| Frequency response | B | | 50 Hz to 25 | kHz |
| Noise output voltage (r.m.s. value; note 3) | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,3 | mV |
| | | < | 0,5 | mV |
| $R_S$ = 8,2 kΩ | $V_{n(rms)}$ | typ. | 0,5 | mV |
| | | < | 1,0 | mV |

| | | | |
|---|---|---|---|
| Ripple rejection (note 4) | | | |
| at f = 100 Hz; C2 = 1 μF | RR | typ. | 44 dB |
| at f = 1 kHz to 10 kHz | RR | > | 48 dB |
| | | typ. | 54 dB |
| Bootstrap current at onset of clipping (pin 4) | | | |
| $R_L$ = 4 Ω and 2 Ω | $I_4$ | typ. | 40 mA |
| Stand-by current (note 5) | $I_{sb}$ | < | 1 mA |
| Crystal temperature for −3 dB gain | $T_c$ | > | 150 °C |

**Notes**

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).




(1) With $R_L$ = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

# SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 14) | $V_P$ | | 6 to 23 | V |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 | °C |
| Supply voltage (pin 14) | $V_P$ | typ. | 20 | V |
| Current consumption | $I_{14}$ | typ. | 3,5 | mA |
| Maximum input signal handling (r.m.s. value) | $V_{i(rms)}$ | typ. | 6 | V |
| Voltage gain | $G_v$ | typ. | 1 | |
| Total harmonic distortion | $d_{tot}$ | typ. | 0,01 | % |
| Crosstalk | $\alpha$ | typ. | 70 | dB |
| Signal-to-noise ratio | S/N | typ. | 120 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

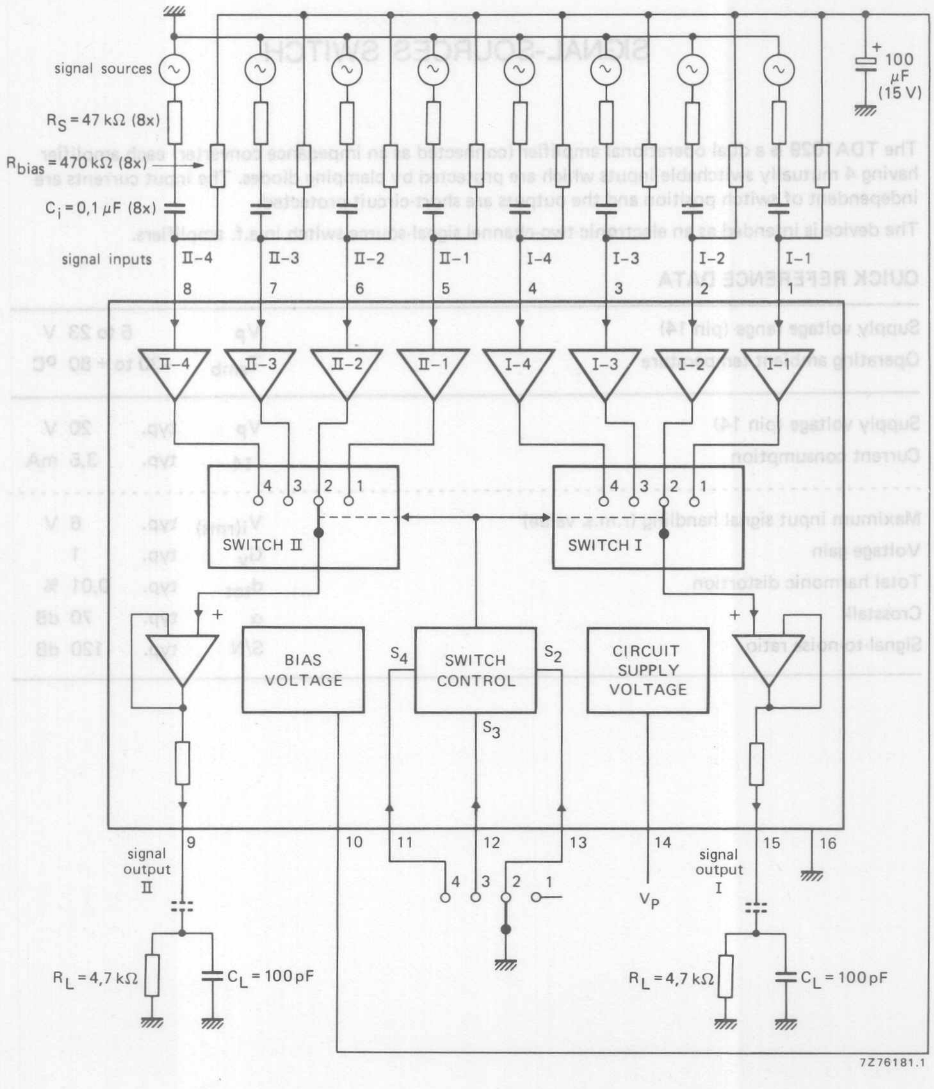



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 14) | $V_P$ | max. | 23 V |
| Input voltage (pins 1 to 8) | $V_I$ | max. | $V_P$ |
| | $-V_I$ | max. | 0,5 V |
| Switch control voltage (pins 11, 12 and 13) | $V_S$ | | 0 to 23 V |
| Input current | $\pm I_I$ | max. | 20 mA |
| Switch control current | $-I_S$ | max. | 50 mA |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 °C |

## CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | |
|---|---|---|---|
| Current consumption without load; $I_9 = I_{15} = 0$ | $I_{14}$ | typ. | 3,5 mA |
| | | | 2 to 5 mA |
| Supply voltage range (pin 14) | $V_P$ | | 6 to 23 V |

**Signal inputs**

| | | | |
|---|---|---|---|
| Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ | $V_{io}$ | typ. | 2 mV |
| | | < | 10 mV |
| Input offset current of switched-on inputs | $I_{io}$ | typ. | 20 nA |
| | | < | 200 nA |
| Input offset current of a switched-on input with respect to a non-switched-on input of a channel | $I_{io}$ | typ. | 20 nA |
| | | < | 200 nA |
| Input bias current independent of switch position | $I_i$ | typ. | 250 nA |
| | | < | 950 nA |
| Capacitance between adjacent inputs | C | typ. | 0,5 pF |
| D.C. input voltage range | $V_I$ | | 3 to 19 V |
| Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ | SVRR | typ. | 100 µV/V |
| Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 3,5 µV |
| Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value) | $I_{n(rms)}$ | typ. | 0,05 nA |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ kΩ; f = 1 kHz | α | typ. | 100 dB |

## CHARACTERISTICS (continued)

**Signal amplifier**

| | | | |
|---|---|---|---|
| Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$ | $G_v$ | typ. | 1 |
| Current gain of a switched-on amplifier | $G_i$ | typ. | $10^5$ |

**Signal outputs**

| | | | |
|---|---|---|---|
| Output resistance (pins 9 and 15) | $R_o$ | typ. | 400 Ω |
| Output current capability at $V_P$ = 6 to 23 V | $\pm I_9; \pm I_{15}$ | typ. | 5 mA |
| Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; $R_S$ = 1 kΩ; $R_L$ = 10 MΩ; $C_L$ = 10 pF | f | typ. | 1,3 MHz |
| Slew rate (unity gain); $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ $R_L$ = 10 MΩ; $C_L$ = 10 pF | S | typ. | 2 V/μs |

**Bias voltage**

| | | | |
|---|---|---|---|
| D.C. output voltage | $V_{10-16}$ | typ. | 11 V * |
| | | | 10,2 to 11,8 V |
| Output resistance | $R_{10-16}$ | typ. | 8,2 kΩ |

**Switch control**

| switched-on inputs | interconnected pins | control voltages | | |
|---|---|---|---|---|
| | | $V_{11-16}$ | $V_{12-16}$ | $V_{13-16}$ |
| I-1, II-1 | 1-15, 5-9 | H | H | H |
| I-2, II-2 | 2-15, 6-9 | H | H | L |
| I-3, II-3 | 3-15, 7-9 | H | L | H |
| I-4, II-4 | 4-15, 8-9 | L | H | H |
| I-4, II-4 | 4-15, 8-9 | L | L | H |
| I-4, II-4 | 4-15, 8-9 | L | H | L |
| I-4, II-4 | 4-15, 8-9 | L | L | L |
| I-3, II-3 | 3-15, 7-9 | H | L | L |

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leq 1{,}5$ V.

**Control inputs** (pins 11, 12 and 13)

| | | | |
|---|---|---|---|
| Required voltage | | | |
| HIGH | $V_{SH}$ | > | 3,3 V ** |
| LOW | $V_{SL}$ | < | 2,1 V |
| Input current | | | |
| HIGH (leakage current) | $I_{SH}$ | < | 1 μA |
| LOW (control current) | $-I_{SL}$ | < | 250 μA |

* $V_{10-16}$ is typically $0{,}5 \cdot V_{14-16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

## APPLICATION INFORMATION

$V_P$ = 20 V; $T_{amb}$ = 25 °C; measured in Fig. 1; $R_S$ = 47 kΩ; $C_i$ = 0,1 μF; $R_{bias}$ = 470 kΩ; $R_L$ = 4,7 kΩ; $C_L$ = 100 pF (unless otherwise specified)

| | | | | |
|---|---|---|---|---|
| Voltage gain | $G_v$ | typ. | −1,5 | dB |
| Output voltage variation when switching the inputs | $\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$ | typ. | 10 | mV |
| | | < | 100 | mV |
| Total harmonic distortion | | | | |
| over most of signal range (see Fig. 4) | $d_{tot}$ | typ. | 0,01 | % |
| $V_i$ = 5 V; f = 1 kHz | $d_{tot}$ | typ. | 0,02 | % |
| $V_i$ = 5 V; f = 20 Hz to 20 kHz | $d_{tot}$ | typ. | 0,03 | % |
| Output signal handling | | | | |
| $d_{tot}$ = 0,1%; f = 1 kHz (r.m.s. value) | $V_{o(rms)}$ | > | 5,0 | V |
| | | typ. | 5,3 | V |
| Noise output voltage (unweighted) | | | | |
| f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 5 | μV |
| Noise output voltage (weighted) | | | | |
| f = 20 Hz to 20 kHz (in accordance with DIN 45405) | $V_n$ | typ. | 12 | μV |
| Amplitude response | | | | |
| $V_i$ = 5 V; f = 20 Hz to 20 kHz; $C_i$ = 0,22 μF | $\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$ | < | 0,1 | dB * |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz | $\alpha$ | typ. | 75 | dB ** |
| Crosstalk between switched-on inputs and the outputs of the other channels | $\alpha$ | typ. | 90 | dB ** |

* The lower cut-off frequency depends on values of $R_{bias}$ and $C_i$.

** Depends on external circuitry and $R_S$. The value will be fixed mostly by capacitive crosstalk of the external components.

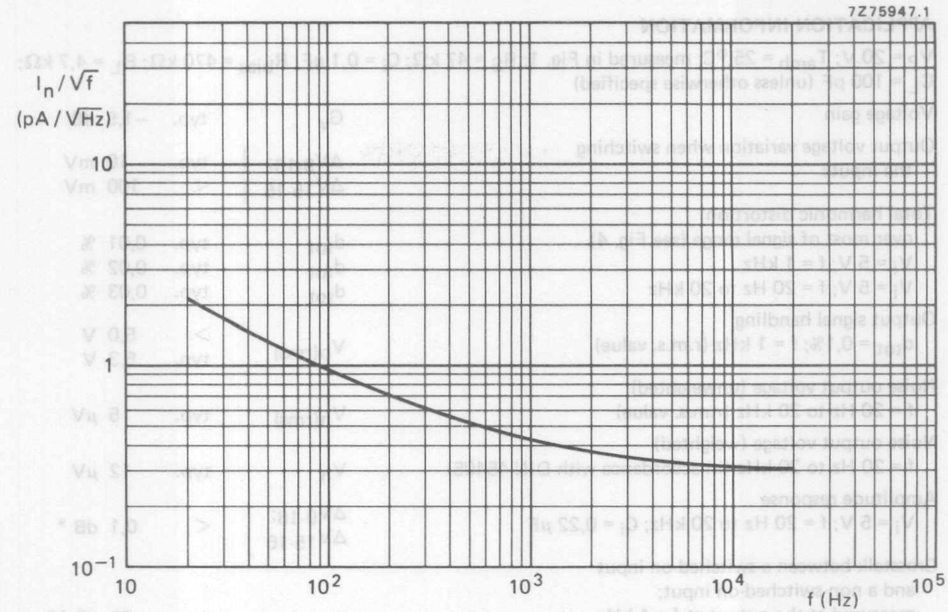



Fig. 2 Equivalent input noise current.

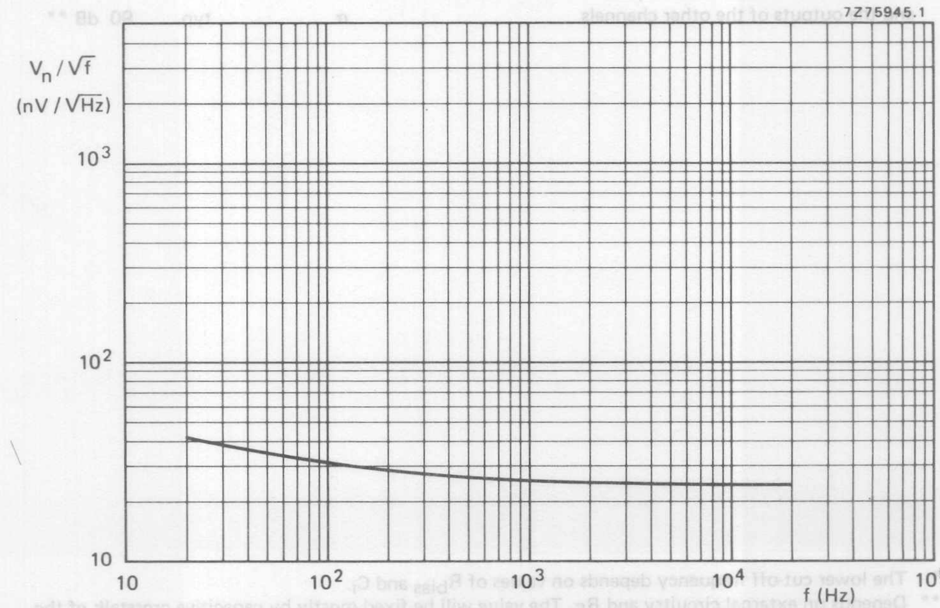



Fig. 3 Equivalent input noise voltage.

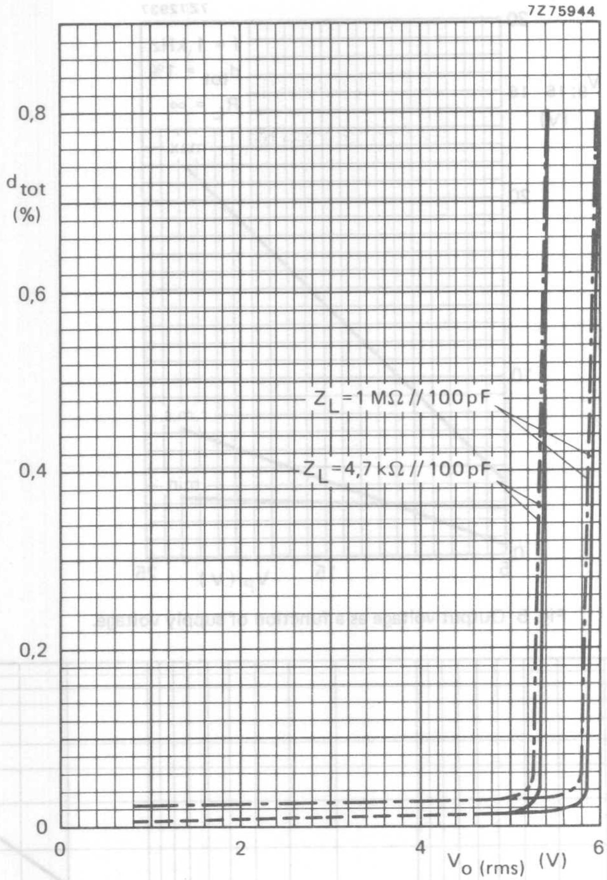



Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; —·— · f = 20 kHz.

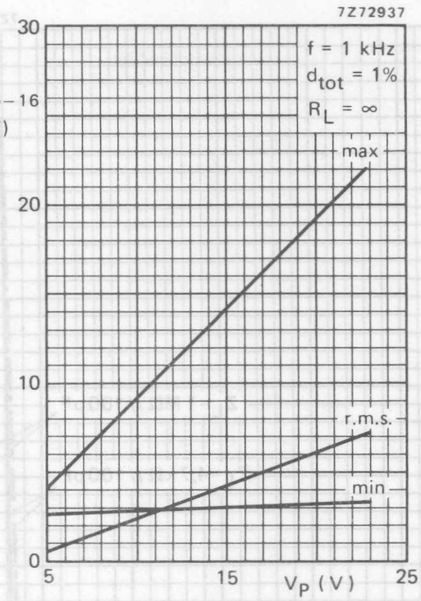



Fig. 5 Output voltage as a function of supply voltage.

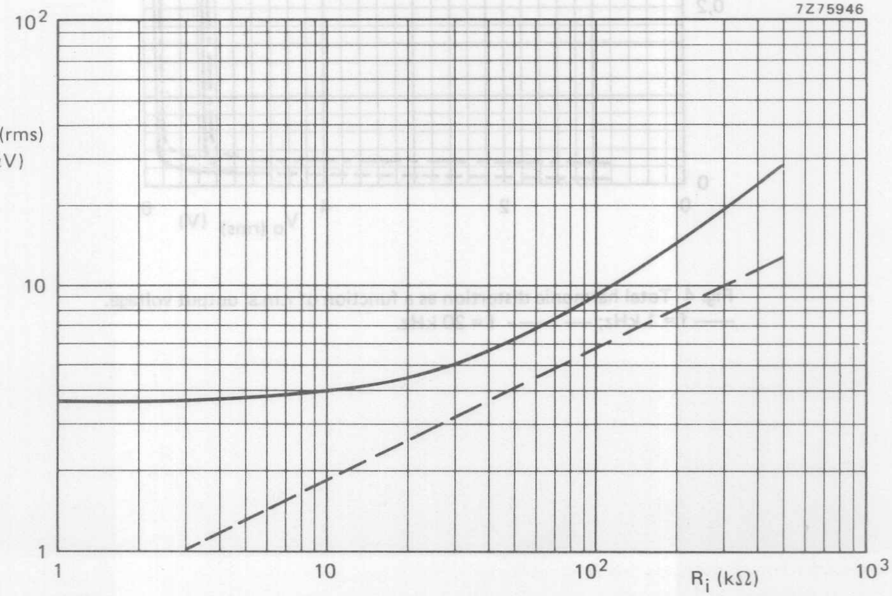



Fig. 6 Noise output voltage as a function of input resistance; $G_v = 1$; f = 20 Hz to 20 kHz.
—— $V_n$ (output); – – – $V_n$ ($R_S$).

## APPLICATION NOTES

### Input protection circuit and indication

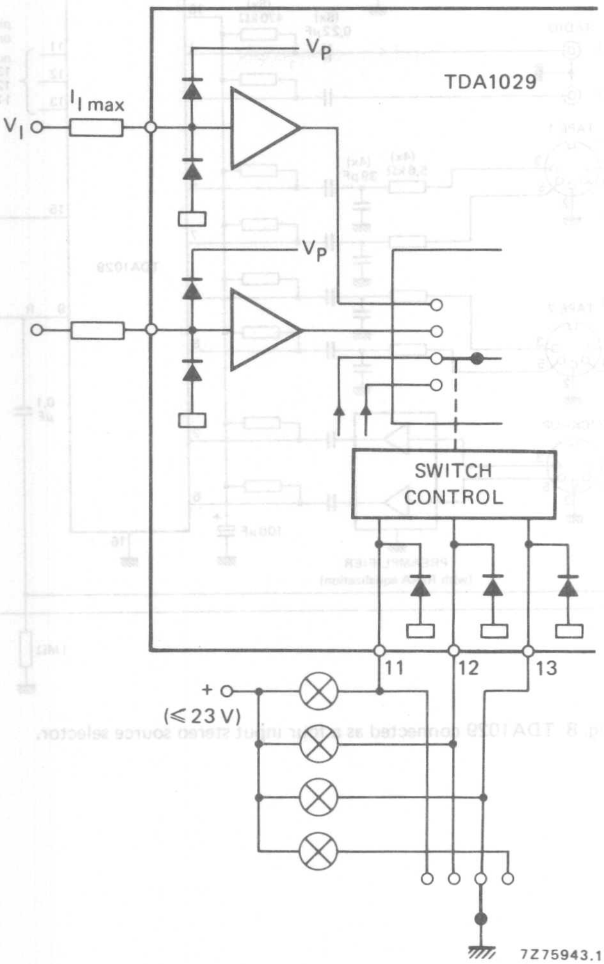



Fig. 7 Circuit diagram showing input protection and indication.

### Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

### Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

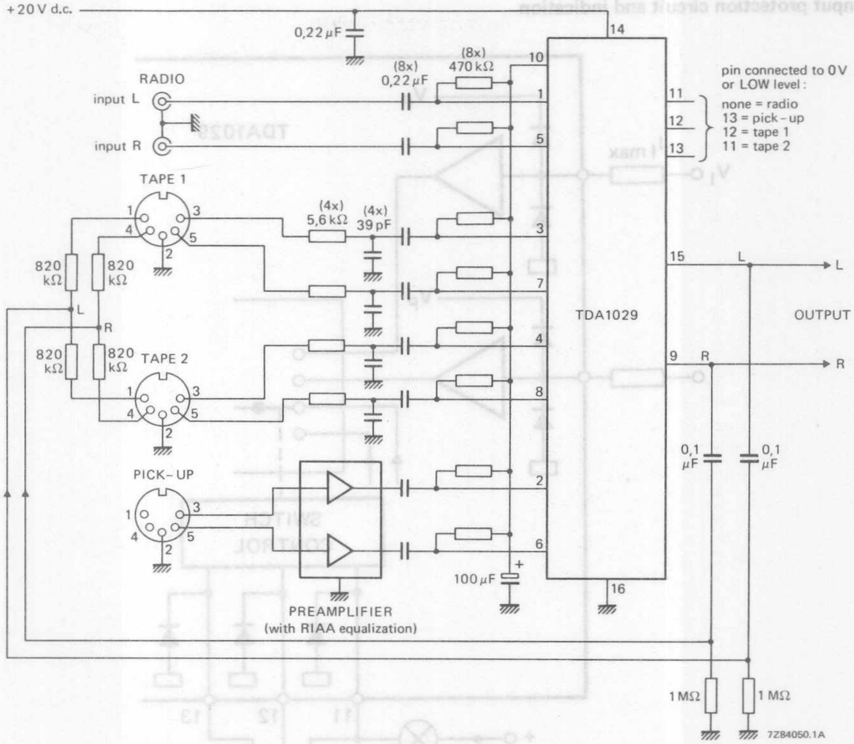



Fig. 8 TDA1029 connected as a four input stereo source selector.

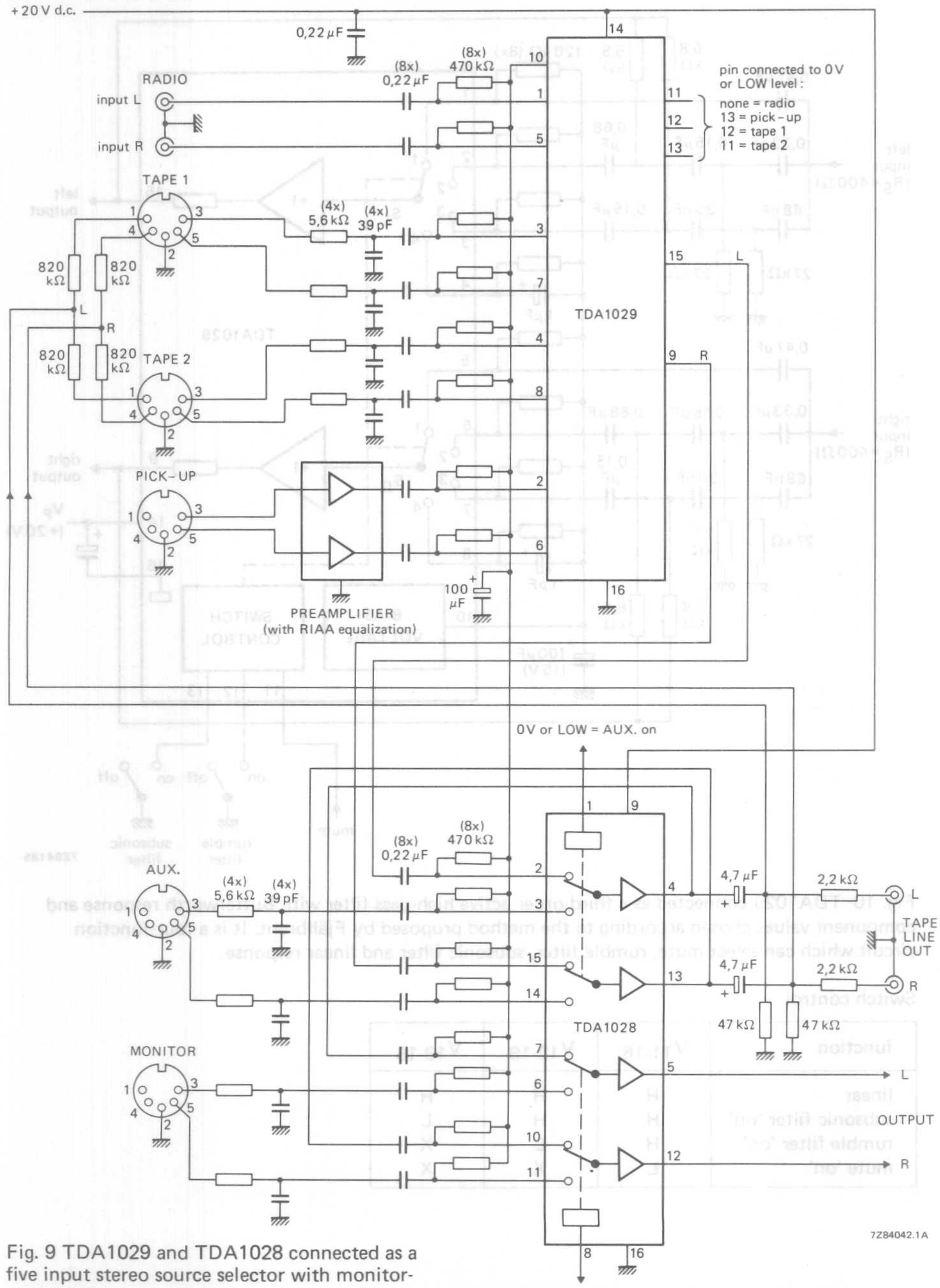



Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

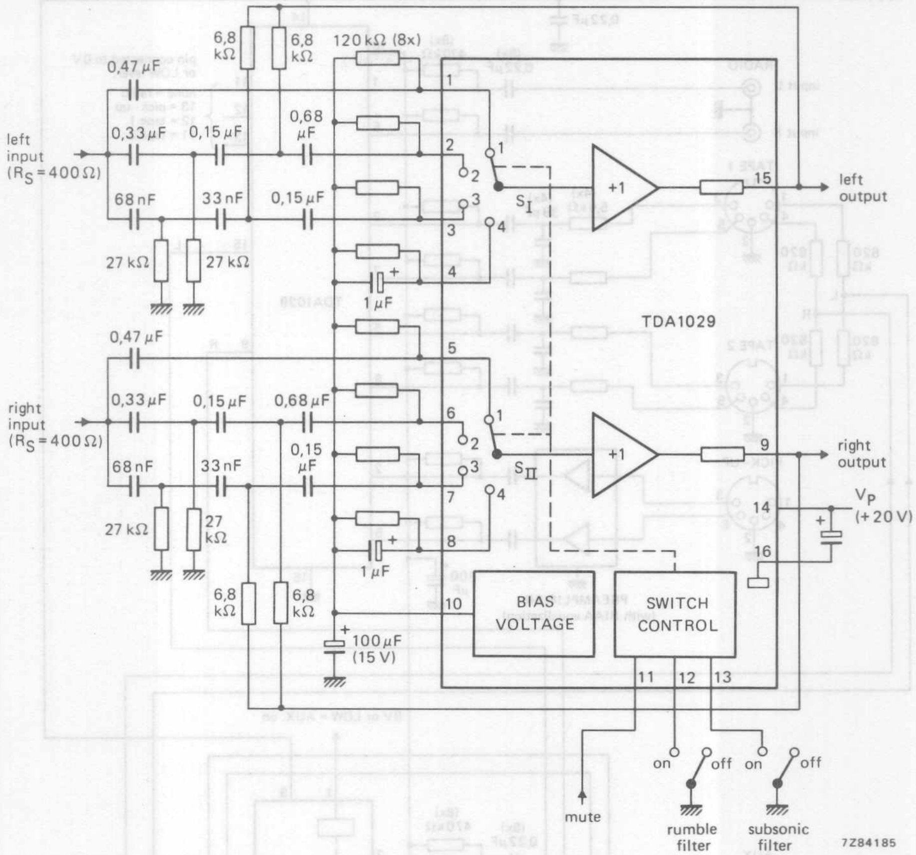



Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

| function | $V_{11\text{-}16}$ | $V_{12\text{-}16}$ | $V_{13\text{-}16}$ |
|---|---|---|---|
| linear | H | H | H |
| subsonic filter 'on' | H | H | L |
| rumble filter 'on' | H | L | X |
| mute 'on' | L | X | X |

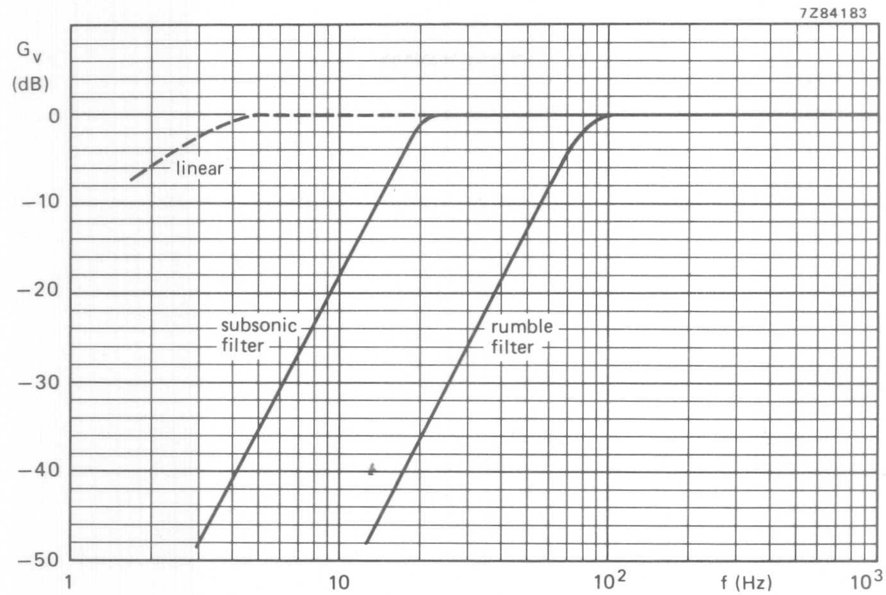



Fig. 11 Frequency response curves for the circuit of Fig. 10.

# MOTOR SPEED REGULATOR WITH THERMAL SHUT-DOWN

The TDA1059B is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

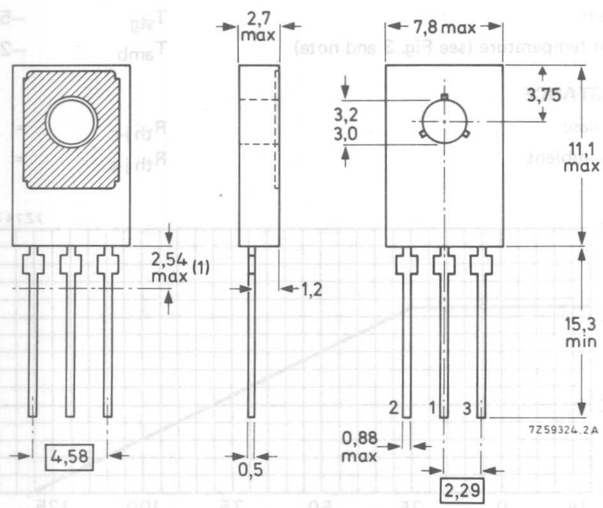
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{2\text{-}1}$ | typ. | 9 | V |
| | | | 3,3 to 16 | V |
| Internal reference voltage | $V_{ref}$ | typ. | 1,3 | V |
| Drop-out voltage | $V_{3\text{-}1}$ | typ. | 1,8 | V |
| Limited output current | $I_{3lim}$ | typ. | 0,6 | A |
| Multiplication coefficient | k | typ. | 9 | |

## PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.




(1) Within this region the cross-section of the leads is uncontrolled.

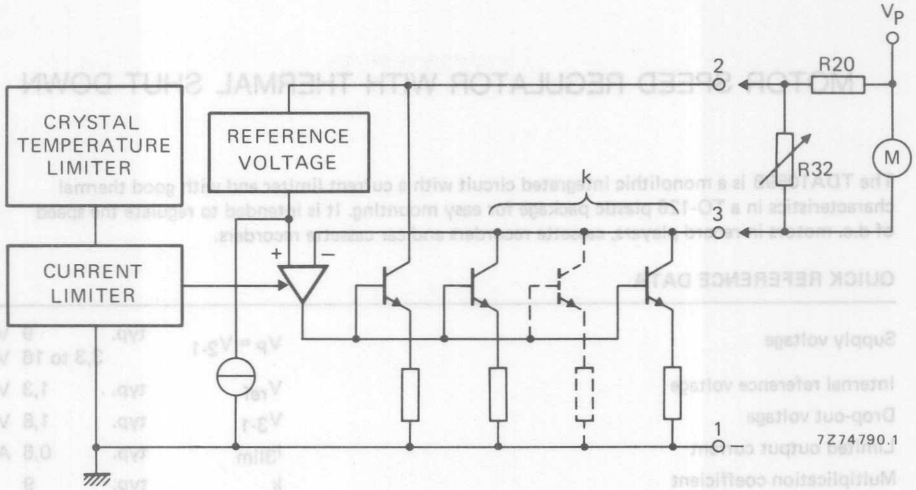



Fig. 2 Functional diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P = V_{2\text{-}1}$ | max. | 16 V |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature (see Fig. 3 and note) | $T_{amb}$ | | −25 to + 130 °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to case | $R_{th\ j\text{-}c}$ | = | 10 K/W |
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 100 K/W |

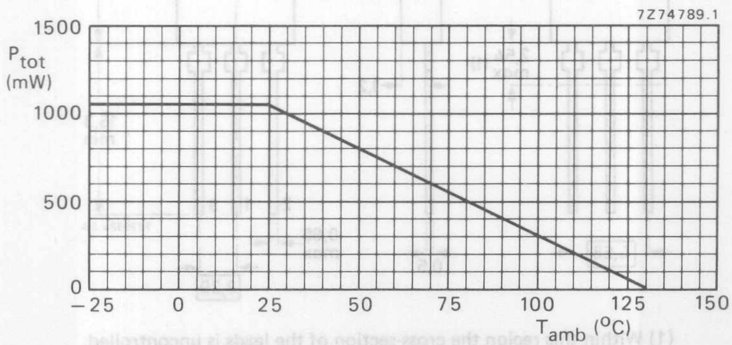



Fig. 3 Power derating curve.

Note

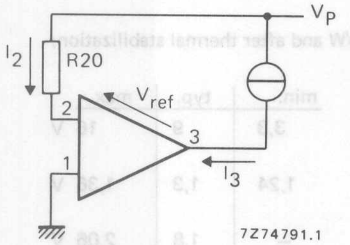
At ambient temperatures above 130 °C, the crystal temperature limiter decreases the internal power consumption.

## CHARACTERISTICS

$V_P$ = 9 V; $T_{amb}$ = 25 °C; R20 = 0; heatsink with $R_{th}$ = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4.

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_P = V_{2\text{-}1}$ | 3,3 | 9 | 16 | V |
| Internal reference voltage<br>$V_P$ = 3,3 V; $I_3$ = 80 mA | $V_{ref}$ | 1,24 | 1,3 | 1,36 | V |
| Drop-out voltage<br>$I_3$ = 80 mA; $\Delta V_{ref}$ = 5% | $V_{3\text{-}1}$ | – | 1,8 | 2,06 | V |
| Quiescent current; $I_3$ = 0 | $I_q$ | 1,8 | 2,3 | 2,8 | mA |
| Limited output current* | $I_{3lim}$ | 0,3 | 0,6 | 1 | A |
| Multiplication coefficient<br>$I_3$ = 50 mA ± 10 mA | $k = \frac{\Delta I_3}{\Delta I_2}$ | 8,5 | 9 | 9,5 | |
| Line regulation<br>$V_P$ = 3,3 to 16 V at $I_3$ = 50 mA | | | | | |
| reference voltage variation | $\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_P$ | –0,115 | 0 | +0,115 | %/V |
| multiplication coefficient variation<br>$I_3$ = 50 ± 10 mA | $\frac{\Delta k}{k} / \Delta V_P$ | – | 0,86 | – | %/V |
| input current variation; $I_3$ = 50 mA | $\frac{\Delta I_2}{\Delta V_P}$ | –15 | 0 | +20 | µA/V |
| Load regulation | | | | | |
| reference voltage variation<br>$I_3$ = 20 to 80 mA | $\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_3$ | 0 | 19 | 38,5 | %/A |
| multiplication coefficient variation<br>$I_3$ = 30 ± 10 to 70 ± 10 mA | $\frac{\Delta k}{k} / \Delta I_3$ | –0,075 | 0 | +0,075 | %/mA |
| Temperature coefficient<br>$I_3$ = 50 mA; $T_{amb}$ = –15 to +65 °C | | | | | |
| reference voltage variation | $\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$ | –0,03 | 0 | +0,03 | %/K |
| multiplication coefficient variation<br>$\Delta I_3$ = ± 10 mA | $\frac{\Delta k}{k} / \Delta T_{amb}$ | – | 0,008 | – | %/K |
| input current variation | $\frac{\Delta I_2}{\Delta T_{amb}}$ | –2 | 0 | +2 | µA/K |

* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059B will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

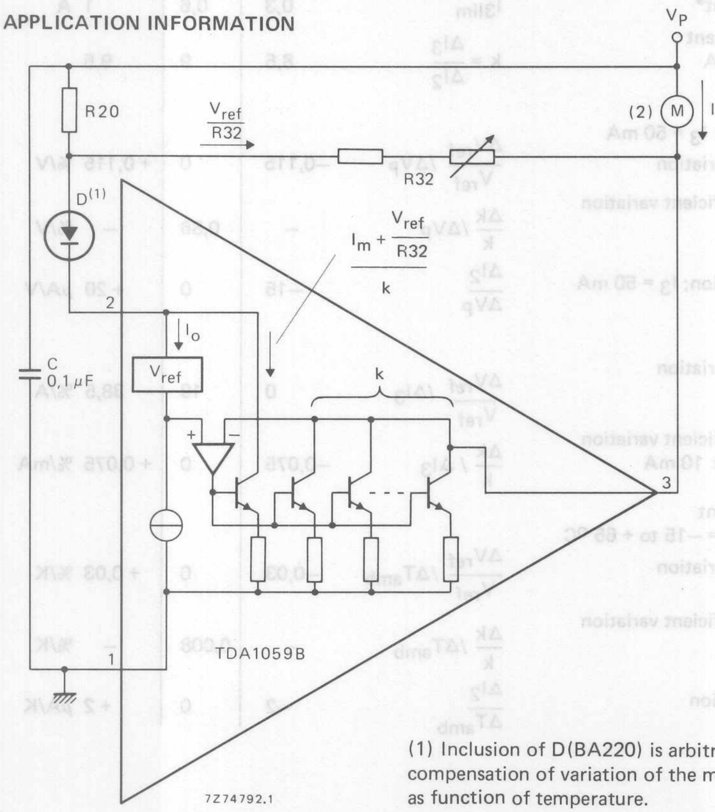



Note

For start operation: $V_{ref}$ must start with final $V_P = 6{,}7$ V and a time constant of $3\tau = 100$ ms in which $\tau$ = R.C; R = source impedance, C = by-pass capacitor.

Fig. 4 Test circuit.

## APPLICATION INFORMATION




(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 100 Ω + 100 Ω (variable).

Fig. 5 Example of using the TDA1059B in a d.c. motor speed regulation circuit.

**Motor equations**

$E_m = \alpha_1 n$ where: $\alpha_1$, $\alpha_2$ = motor constant
$I_m = \alpha_2 r$ n = number of revolutions
$V_m = E_m + R_m I_m$ r = motor torque
$E_m$ = back electromotive force
$R_m$ = motor resistance

The back electromotive force ($E_m$) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left( \frac{R20}{k} - R_m \right) I_m + V_{ref} \left\{ 1 + \frac{R20}{R32} \left( 1 + \frac{1}{k} \right) \right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left( \frac{R20}{k} - R_m \right) I_m + \left( V_{ref} + V_D \right) \left\{ 1 + \frac{R20}{R32} \left( 1 + \frac{1}{k} \right) \right\} + R20.I_o$$

Speed regulation is constant when $E_m$ is independent of $I_m$ variations; this will be obtained when $R20 = kR_m$.

$E_m$, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

# MOTOR SPEED REGULATOR

The TDA1059C is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

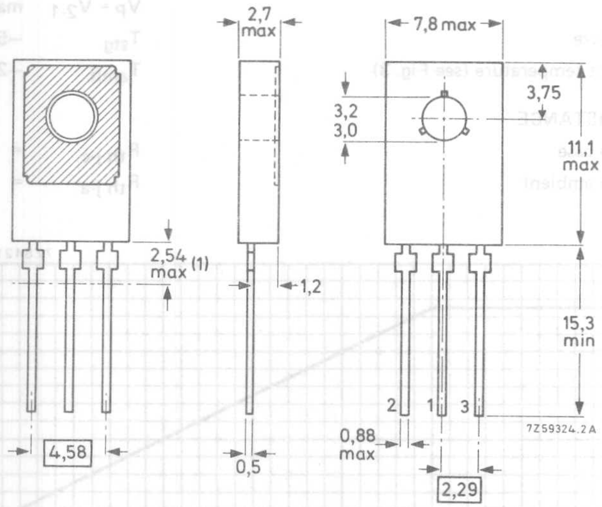
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Suppy voltage | $V_P = V_{2\text{-}1}$ | typ. | 9 | V |
| | | | 2,5 to 16 | V |
| Internal reference voltage | $V_{ref}$ | typ. | 1,1 | V |
| Drop-out voltage | $V_{3\text{-}1}$ | typ. | 1,0 | V |
| Limited output current | $I_{3lim}$ | typ. | 0,6 | A |
| Multiplication coefficient | k | typ. | 9 | |

## PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.




(1) Within this region the cross-section of the leads is uncontrolled.

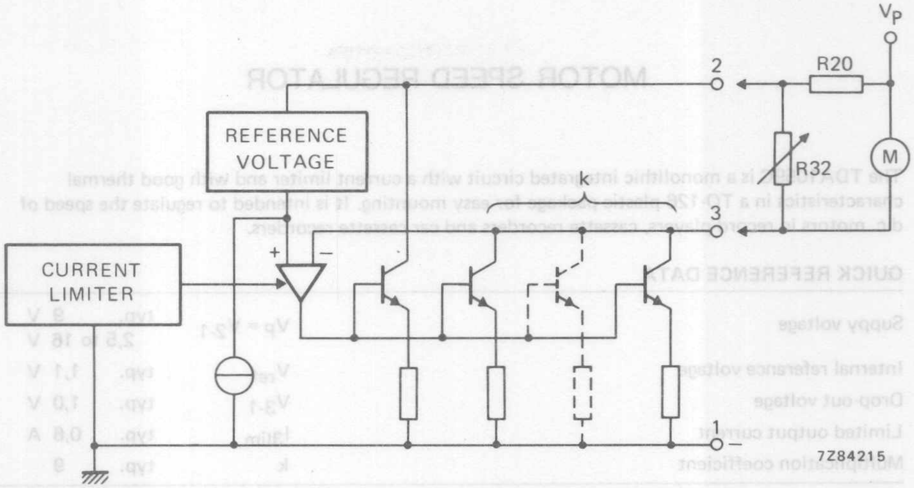



Fig. 2 Functional diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P = V_{2\text{-}1}$ | max. | 16 V |
| Storage temperature | $T_{stg}$ | −55 to + 150 | $^oC$ |
| Operating ambient temperature (see Fig. 3) | $T_{amb}$ | −25 to + 150 | $^oC$ |

## THERMAL RESISTANCE

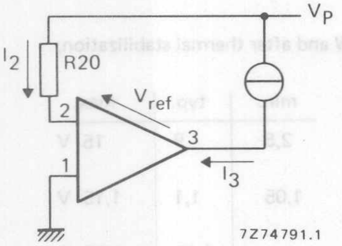
| | | | |
|---|---|---|---|
| From junction to case | $R_{th\ j\text{-}c}$ | = | 10 K/W |
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 100 K/W |


Fig. 3 Power derating curve.

## CHARACTERISTICS

$V_P$ = 9 V; $T_{amb}$ = 25 °C; R20 = 0; heatsink with $R_{th}$ = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_P = V_{2\text{-}1}$ | 2,5 | 9 | 15 | V |
| Internal reference voltage<br>$V_P$ = 2,5 V; $I_3$ = 80 mA | $V_{ref}$ | 1,05 | 1,1 | 1,15 | V |
| Drop-out voltage<br>$I_3$ = 80 mA; $\Delta V_{ref}$ = 2% | $V_{3\text{-}1}$ | – | 1,03 | 1,25 | V |
| Quiescent current; $I_3$ = 0 | $I_q$ | 2,2 | 2,7 | 3,2 | mA |
| Limited output current | $I_{3lim}$ | 0,3 | 0,45 | 1 | A |
| Multiplication coefficient<br>$I_3$ = 50 mA ± 10 mA | $k = \frac{\Delta I_3}{\Delta I_2}$ | 8,5 | 9 | 9,5 | |
| Line regulation<br>$V_P$ = 2,5 to 15 V at $I_3$ = 50 mA | | | | | |
| reference voltage variation | $\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_P$ | 0,04 | 0,18 | 0,22 | %/V |
| multiplication coefficient variation<br>$I_3$ = 50 ± 10 mA | $\frac{\Delta k}{k}/\Delta V_P$ | – | 0,86 | – | %/V |
| input current variation; $I_3$ = 50 mA | $\frac{\Delta I_2}{\Delta V_P}$ | 0 | 15 | 30 | μA/V |
| Load regulation | | | | | |
| reference voltage variation<br>$I_3$ = 20 to 80 mA | $\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_3$ | 0 | 30 | 45,5 | %/A |
| multiplifaction coefficient variation<br>$I_3$ = 30 ± 10 to 70 ± 10 mA | $\frac{\Delta k}{k}/\Delta I_3$ | – | 0,04 | – | %/mA |
| Temperature coefficient<br>$I_3$ = 50 mA; $T_{amb}$ = −15 to + 65 °C | | | | | |
| reference voltage variation | $\frac{\Delta V_{ref}}{V_{ref}}/\Delta T_{amb}$ | −0,036 | 0 | +0,036 | %/K |
| multiplication coefficient variation<br>$\Delta I_3$ = ± 10 mA | $\frac{\Delta k}{k}/\Delta T_{amb}$ | – | 0,008 | – | %/K |
| input current variation | $\frac{\Delta I_2}{\Delta T_{amb}}$ | – | 4 | – | μA/K |

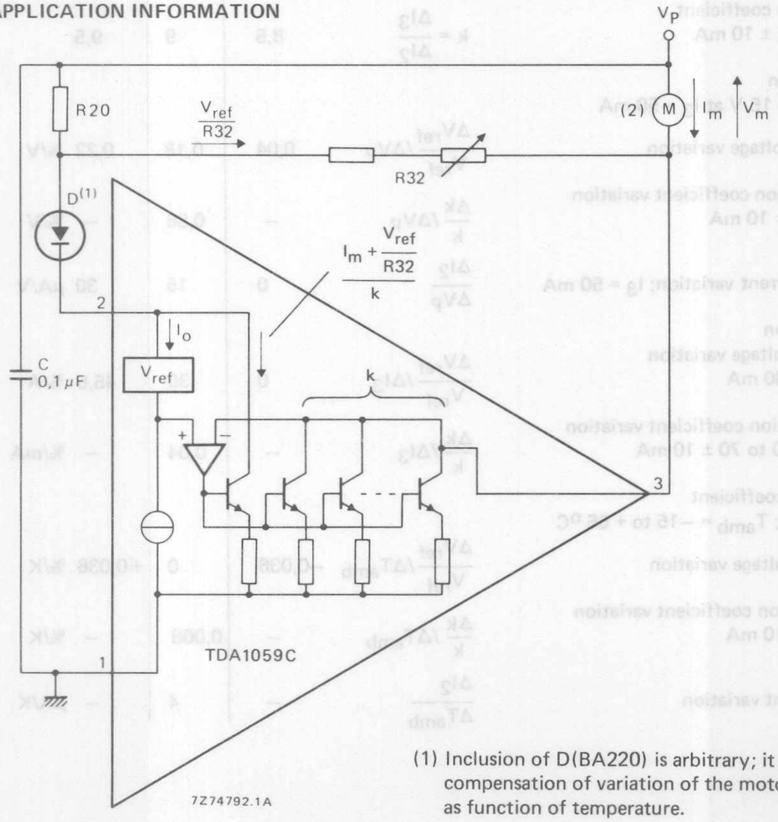



**Note**

For start operation: $V_{ref}$ must start with final $V_P$ = 6 V and a time constant of 3 $\tau$ = 100 ms in which $\tau$ = R.C.; R = source impedance, C = by-pass capacitor.

Fig. 4 Test circuit.

## APPLICATION INFORMATION




(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 39 Ω + 47 Ω (variable).

Fig. 5 Example of using the TDA1059C in a d.c. motor speed regulation circuit.

**Motor equations**

$E_m = \alpha_1 n$ where: $\alpha_1, \alpha_2$ = motor constant

$I_m = \alpha_2 r$ n = number of revolutions

$V_m = E_m + R_m I_m$ r = motor torque

$E_m$ = back electromotive force

$R_m$ = motor resistance

The back electromotive force ($E_m$) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + V_{ref}\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + \left(V_{ref} + V_D\right)\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

Speed regulation is constant when $E_m$ is independent of $I_m$ variations; this will be obtained when $R20 = kR_m$.

$E_m$, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

# AM RECEIVER CIRCUIT

## GENERAL DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

### Features

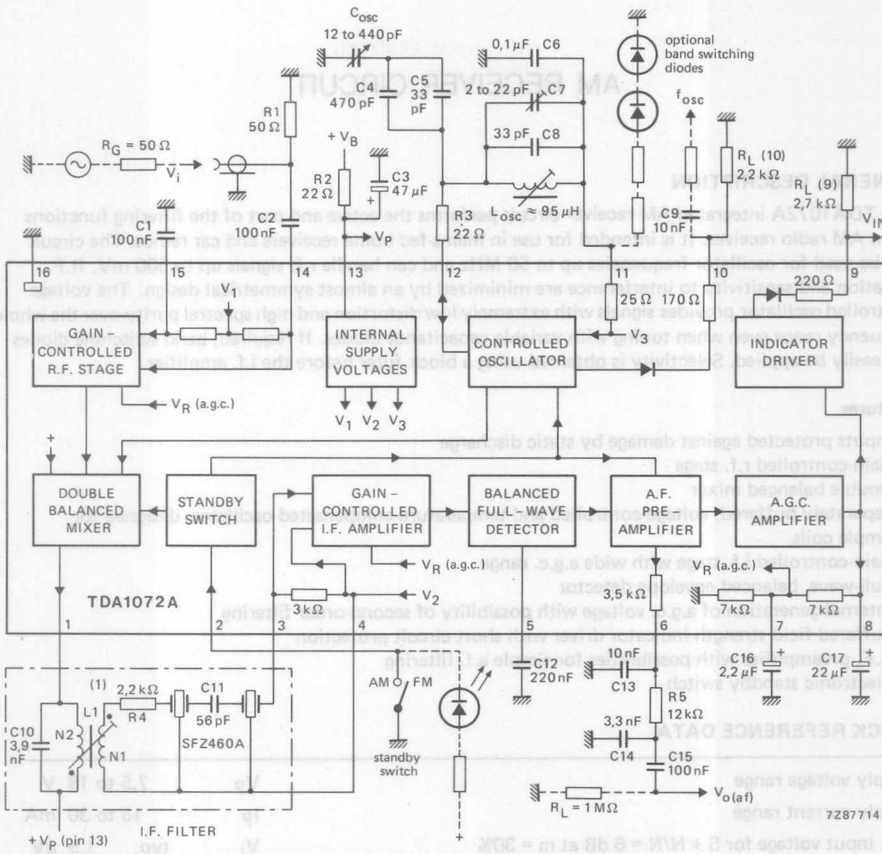
- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 7,5 to 18 | V |
| Supply current range | $I_P$ | | 15 to 30 | mA |
| R.F. input voltage for S + N/N = 6 dB at m = 30% | $V_i$ | typ. | 1,5 | $\mu$V |
| R.F. input voltage for 3% total harmonic distortion (THD) at m = 80% | $V_i$ | typ. | 500 | mV |
| A.F. output voltage with $V_i$ = 2 mV; $f_i$ = 1 MHz; m = 30% and $f_m$ = 400 Hz | $V_{o(af)}$ | typ. | 310 | mV |
| A.G.C. range: change of $V_i$ for 1 dB change of $V_{o(af)}$ | | typ. | 86 | dB |
| Field strength indicator voltage at $V_i$ = 500 mV; $R_{L(9)}$ = 2,7 kΩ | $V_{IND}$ | typ. | 2,8 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).




(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; $Q_o = 65$; $Q_B = 57$.
Filter data: $Z_F = 700\ \Omega$ at $R_{3\text{-}4} = 3\ k\Omega$; $Z_I = 4,8\ k\Omega$.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

## FUNCTIONAL DESCRIPTION

### Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

### Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

### Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

### Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

### A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

### A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

### Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

### Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

### Short-circuit protection

All pins have short-circuit protection to ground.

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{13\text{-}16}$ | max. | 20 | V |
| Total power dissipation | $P_{tot}$ | max. | 875 | mW |
| Input voltage | $\lvert V_{14\text{-}15} \rvert$ | max. | 12 | V |
| | $-V_{14\text{-}16}, -V_{15\text{-}16}$ | max. | 0,6 | V |
| | $V_{14\text{-}16}, V_{15\text{-}16}$ | max. | $V_P$ | V |
| Input current | $\lvert I_{14} \rvert, \lvert I_{15} \rvert$ | max. | 200 | mA |
| Operating ambient temperature range | $T_{amb}$ | −40 to | + 80 | °C |
| Storage temperature range | $T_{stg}$ | −55 to | + 150 | °C |
| Junction temperature | $T_j$ | max. | + 125 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 80 | K/W |

## DEVICE CHARACTERISTICS

$V_P = V_{13\text{-}16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supplies** | | | | | |
| Supply voltage | $V_P = V_{13\text{-}16}$ | 7,5 | 8,5 | 18 | V |
| Supply current | $I_P = I_{13}$ | 15 | 23 | 30 | mA |
| **R.F. stage and mixer** | | | | | |
| Input voltage (d.c. value) | $V_{14\text{-}16}, V_{15\text{-}16}$ | – | $V_P/2$ | – | V |
| R.F. input impedance at $V_i < 300\ \mu V$ | $R_{14\text{-}16}, R_{15\text{-}16}$ | – | 5,5 | – | kΩ |
| | $C_{14\text{-}16}, C_{15\text{-}16}$ | – | 25 | – | pF |
| R.F. input impedance at $V_i > 10$ mV | $R_{14\text{-}16}, R_{15\text{-}16}$ | – | 8 | – | kΩ |
| | $C_{14\text{-}16}, C_{15\text{-}16}$ | – | 22 | – | pF |
| I.F. output impedance | $R_{1\text{-}16}$ | 500 | – | – | kΩ |
| | $C_{1\text{-}16}$ | – | 6 | – | pF |
| Conversion transconductance before start of a.g.c. | $I_1/V_i$ | – | 6,5 | – | mA/V |
| Maximum i.f. output voltage, inductive coupling to pin 1 | $V_{1\text{-}13(p\text{-}p)}$ | – | 5 | – | V |
| D.C. value of output current (pin 1) at $V_i = 0$ V | $I_1$ | – | 1,2 | – | mA |
| A.G.C. range of input stage | | – | 30 | – | dB |
| R.F. signal handling capability: input voltage for THD = 3% at m = 80% | $V_{i(rms)}$ | – | 500 | – | mV |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Oscillator** | | | | | |
| Frequency range | $f_{osc}$ | 0,6 | – | 60 | MHz |
| Oscillator amplitude (pins 11 to 12) | $V_{11\text{-}12}$ | – | 130 | 150 | mV |
| External load impedance | $R_{12\text{-}11(ext)}$ | 0,5 | – | 200 | kΩ |
| External load impedance for no oscillation | $R_{12\text{-}11(ext)}$ | – | – | 60 | Ω |
| Ripple rejection at $V_{P(rms)}$ = 100 mV; $f_p$ = 100 Hz (RR = 20 log [$V_{13\text{-}16}/V_{11\text{-}16}$]) | RR | – | 55 | – | dB |
| Source voltage for switching diodes (6 x $V_{BE}$) | $V_{11\text{-}16}$ | – | 4,2 | – | V |
| D.C. output current (for switching diodes) | $-I_{11}$ | 0 | – | 20 | mA |
| Change of output voltage at $\Delta I_{11}$ = 20 mA (switch to maximum load) | $\Delta V_{11\text{-}16}$ | – | 0,5 | – | V |
| **Buffered oscillator output** | | | | | |
| D.C. output voltage | $V_{10\text{-}16}$ | – | 0,7 | – | V |
| Output signal amplitude | $V_{10\text{-}16(p\text{-}p)}$ | – | 320 | – | mV |
| Output impedance | $R_{10}$ | – | 170 | – | Ω |
| Output current | $-I_{10(peak)}$ | – | – | 3 | mA |
| **I.F., a.g.c. and a.f. stages** | | | | | |
| D.C. input voltage | $V_{3\text{-}16}$, $V_{4\text{-}16}$ | – | 2,0 | – | V |
| I.F. input impedance | $R_{3\text{-}4}$ | 2,4 | 3 | 3,9 | kΩ |
| | $C_{3\text{-}4}$ | – | 7 | – | pF |
| I.F. input voltage for THD = 3% at m = 80% | $V_{3\text{-}4}$ | – | 90 | – | mV |
| Voltage gain before start of a.g.c. | $V_{3\text{-}4}/V_{6\text{-}16}$ | – | 68 | – | dB |
| A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV | $\Delta V_{3\text{-}4}$ | – | 55 | – | dB |
| A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV | $V_{o(af)}$ | – | 130 | – | mV |
| A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV | $V_{o(af)}$ | – | 310 | – | mV |
| A.F. output impedance (pin 6) | $\lvert Z_o \rvert$ | – | 3,5 | – | kΩ |
| **Indicator driver** | | | | | |
| Output voltage at $V_i$ = 0 mV; $R_{L(9)}$ = 2,7 kΩ | $V_{9\text{-}16}$ | – | 20 | 150 | mV |
| Output voltage at $V_i$ = 500 mV; $R_{L(9)}$ = 2,7 kΩ | $V_{9\text{-}16}$ | 2,5 | 2,8 | 3,1 | V |
| Load resistance | $R_{L(9)}$ | 1,5 | – | – | kΩ |

DEVICE CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Standby switch** | | | | | |
| Switching threshold at $V_P$ = 7,5 to 18 V; $T_{amb}$ = −40 to + 80 °C | | | | | |
| on-voltage | $V_{2\text{-}16}$ | 0 | – | 2,0 | V |
| off-voltage | $V_{2\text{-}16}$ | 3,5 | – | 20 | V |
| on-current at $V_{2\text{-}16}$ = 0 V | $-I_2$ | – | – | 200 | μA |
| off-current at $V_{2\text{-}16}$ = 20 V | $\lvert I_2 \rvert$ | – | – | 10 | μA |

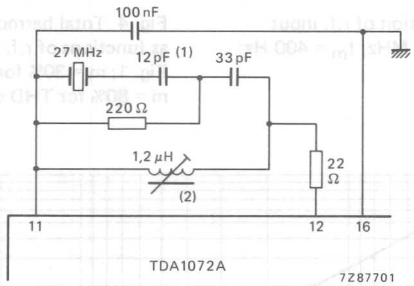
OPERATING CHARACTERISTICS

$V_P$ = 8,5 V; $f_i$ = 1 MHz; m = 30%; $f_m$ = 400 Hz; $T_{amb}$ = 25 °C; measured in Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **R.F. sensitivity** | | | | | |
| R.F. input required for S + N/N = 6 dB | $V_i$ | – | 1,5 | – | μV |
| R.F. input required for S + N/N = 26 dB | $V_i$ | – | 15 | – | μV |
| R.F. input required for S + N/N = 46 dB | $V_i$ | – | 150 | – | μV |
| R.F. input at start of a.g.c. | $V_i$ | – | 30 | – | μV |
| **R.F. large signal handling** | | | | | |
| R.F. input at THD = 3%; m = 80% | $V_i$ | – | 500 | – | mV |
| R.F. input at THD = 3%; m = 30% | $V_i$ | – | 700 | – | mV |
| R.F. input at THD = 10%; m = 30% | $V_i$ | – | 900 | – | mV |
| **A.G.C. range** | | | | | |
| Change of $V_i$ for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV | $\Delta V_i$ | – | 86 | – | dB |
| Change of $V_i$ for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV | $\Delta V_i$ | – | 91 | – | dB |
| **Output signal** | | | | | |
| A.F. output voltage at $V_i$ = 4 μV; m = 80% | $V_{o(af)}$ | – | 130 | – | mV |
| A.F. output voltage at $V_i$ = 1 mV | $V_{o(af)}$ | 240 | 310 | 390 | mV |
| THD at $V_i$ = 1 mV; m = 80% | $d_{tot}$ | – | 0,5 | – | % |
| THD at $V_i$ = 500 mV; m = 30% | $d_{tot}$ | – | 1 | – | % |
| Signal-to-noise ratio at $V_i$ = 100 mV | (S + N)/N | – | 58 | – | dB |
| Ripple rejection at $V_i$ = 2 mV; $V_{P(rms)}$ = 100 mV; $f_P$ = 100 Hz (RR = 20 log [$V_P/V_{o(af)}$]) | RR | – | 38 | – | dB |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Unwanted signals** | | | | | |
| Suppression of i.f. whistles at $V_i$ = 15 $\mu$V; m = 0% related to a.f. signal of m = 30% | | | | | |
| at $f_i \approx 2 \times f_{if}$ | $\alpha_{2if}$ | – | 37 | – | dB |
| at $f_i \approx 3 \times f_{if}$ | $\alpha_{3if}$ | – | 44 | – | dB |
| I.F. suppression at r.f. input | | | | | |
| for symmetrical input | $\alpha_{if}$ | – | 40 | – | dB |
| for asymmetrical input | $\alpha_{if}$ | – | 40 | – | dB |
| Residual oscillator signal at mixer output | | | | | |
| at $f_{osc}$ | $I_{1(osc)}$ | – | 1 | – | $\mu$A |
| at 2 x $f_{osc}$ | $I_{1(2osc)}$ | – | 1,1 | – | $\mu$A |

## APPLICATION INFORMATION




(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o$ = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

APPLICATION INFORMATION (continued)

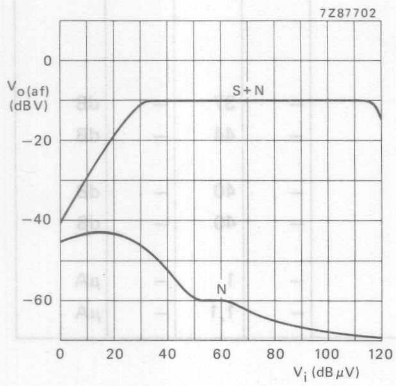



Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; $f_i$ = 1 MHz; $f_m$ = 400 Hz; m = 30%.

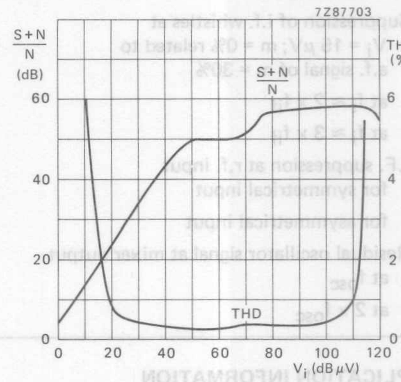



Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

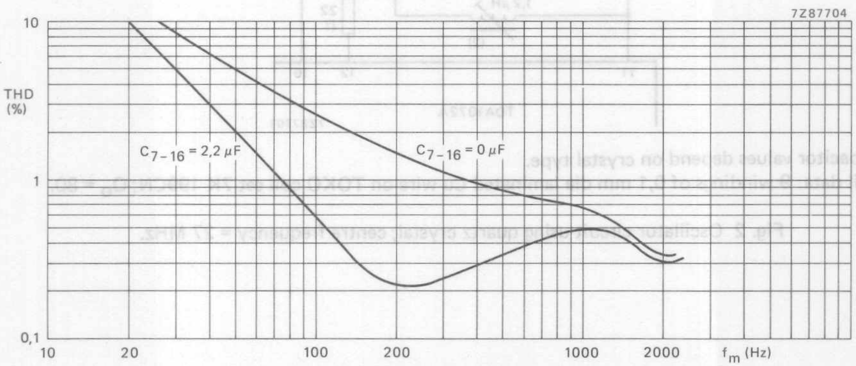



Fig. 5 Total harmonic distortion as a function of modulation frequency at $V_i$ = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2,2 μF.

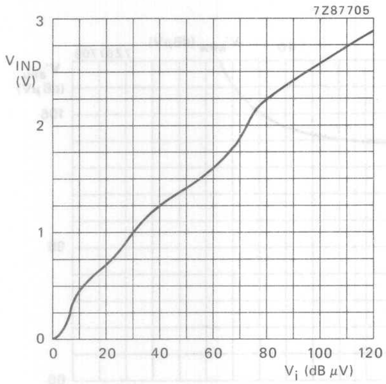



Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

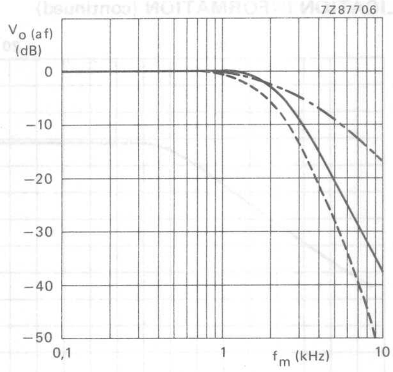



Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:
——— with i.f. filter;
—·—·—· with a.f. filter;
— — — with i.f. and a.f. filters.

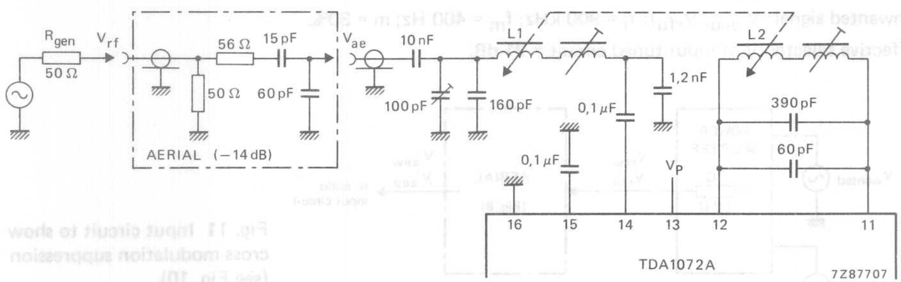



Fig. 8 Car radio application with inductive tuning.

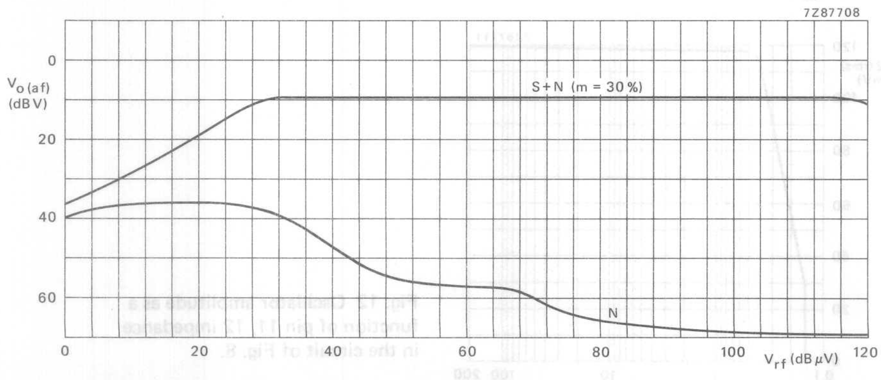



Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

APPLICATION INFORMATION (continued)

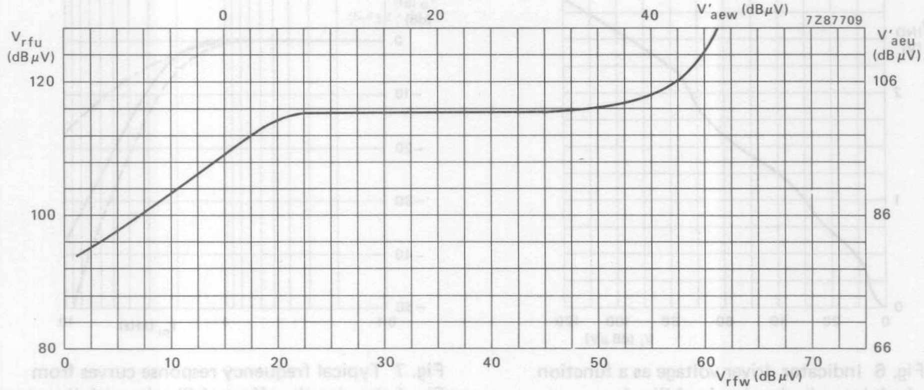



Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; $V_{rfw}$, $V_{rfu}$ are signals at the aerial input, $V'_{aew}$, $V'_{aeu}$ are signals at the unloaded output of the aerial.

Wanted signal ($V'_{aew}$, $V_{rfw}$): $f_i$ = 1 MHz; $f_m$ = 400 Hz; m = 30%.

Unwanted signal ($V'_{aeu}$, $V_{rfu}$): $f_i$ = 900 kHz; $f_m$ = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

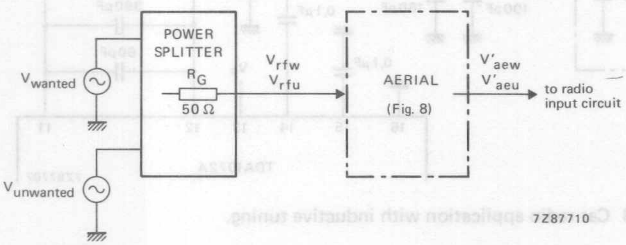



Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

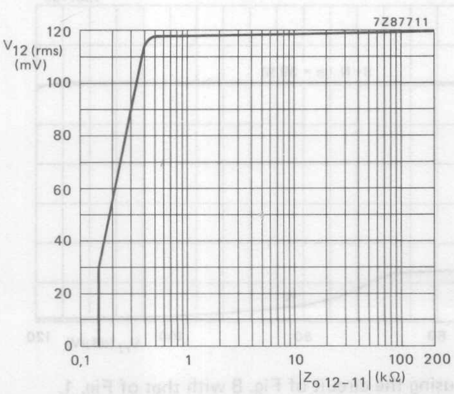



Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

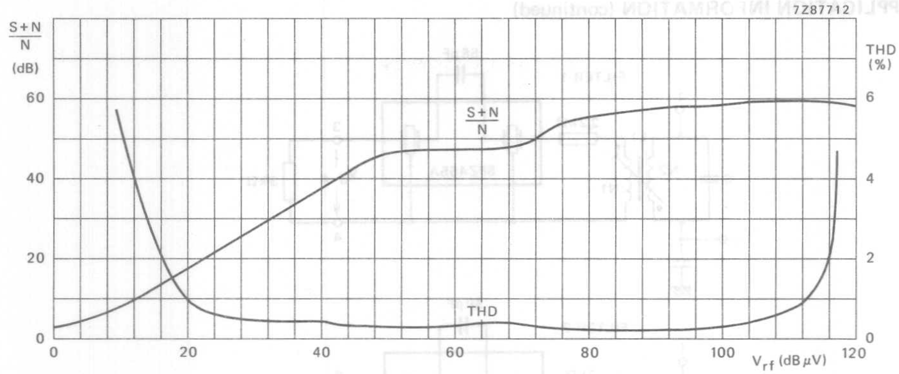



Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

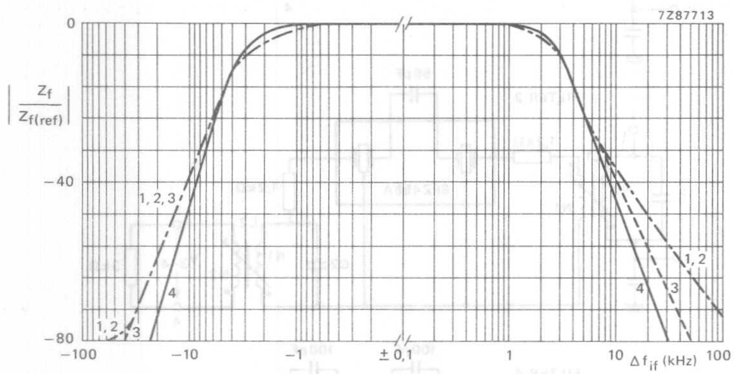



Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

APPLICATION INFORMATION (continued)

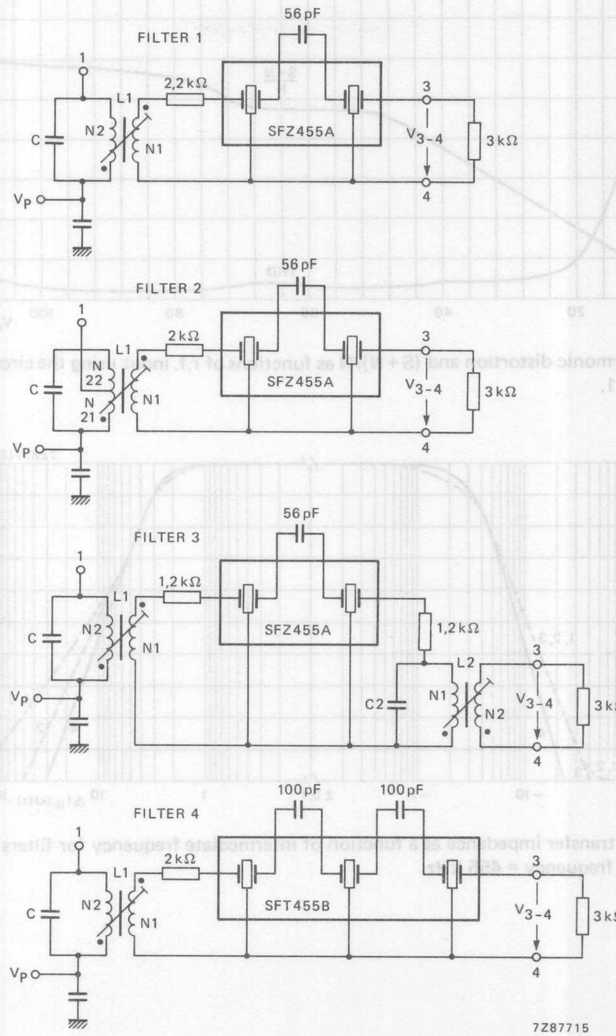



Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

**Table 1** Data for I.F. filters shown in Fig. 15. Criterium for adjustment is $Z_F$ = maximum (optimum selectivity curve at centre frequency $f_0$ = 455 kHz). See also Fig. 14.

| filter no. | 1 | 2 | 3 | | 4 | unit |
|---|---|---|---|---|---|---|
| **Coil data** | L1 | L1 | L1 | L2 | L1 | |
| Value of C | 3900 | 430 | 3900 | 4700 | 3900 | pF |
| N1: N2 | 12 : 32 | 13 : (33 + 66) | 15 : 31 | 29 : 29 | 13 : 31 | |
| Diameter of Cu laminated wire | 0,09 | 0,08 | 0,09 | 0,08 | 0,09 | mm |
| $Q_o$ | 65 (typ.) | 50 | 75 | 60 | 75 | |
| Schematic* of windings | 12 32 | 13 66 33 | 15 31 | 29 29 (N1) (N2) | 13 31 | |
| Toko order no. | 7XNS-A7523DY | L7PES-A0060BTG | 7XNS-A7518DY | 7XNS-A7521AIH | 7XNS-A7519DY | |
| **Resonators** | | | | | | |
| Murata type | SFZ455A | SFZ455A | SFZ455A | | SFT455B | |
| D (typical value) | 4 | 4 | 4 | | 6 | dB |
| $R_G$, $R_L$ | 3 | 3 | 3 | | 3 | kΩ |
| Bandwidth (−3 dB) | 4,2 | 4,2 | 4,2 | | 4,5 | kHz |
| $S_{9kHz}$ | 24 | 24 | 24 | | 38 | dB |
| **Filter data** | | | | | | |
| $Z_I$ | 4,8 | 3,8 | 4,2 | | 4,8 | kΩ |
| $Q_B$ | 57 | 40 | 52 (L1) | 18 (L2) | 55 | |
| $Z_F$ | 0,70 | 0,67 | 0,68 | | 0,68 | kΩ |
| Bandwidth (−3 dB) | 3,6 | 3,8 | 3,6 | | 4,0 | kHz |
| $S_{9kHz}$ | 35 | 31 | 36 | | 42 | dB |
| $S_{18kHz}$ | 52 | 49 | 54 | | 64 | dB |
| $S_{27kHz}$ | 63 | 58 | 66 | | 74 | dB |

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

APPLICATION INFORMATION (continued)

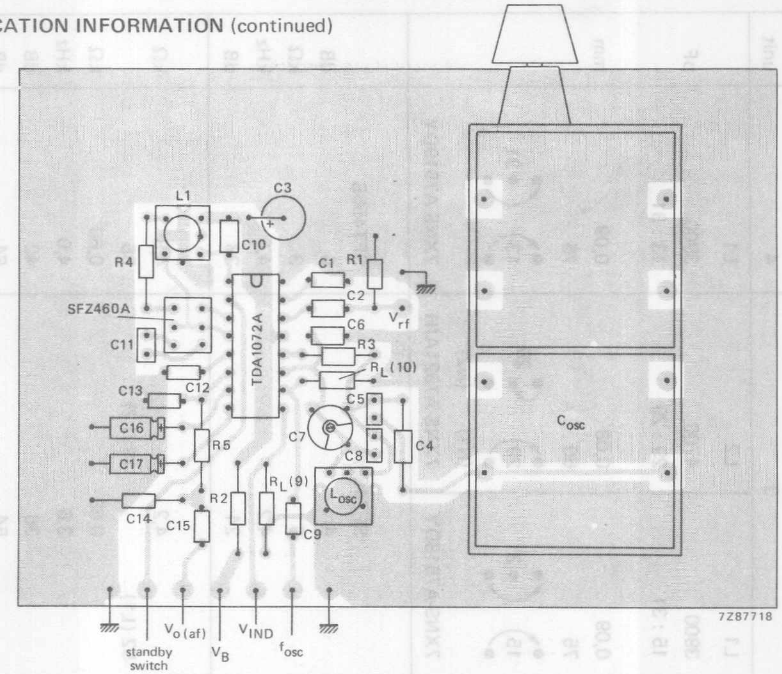



Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

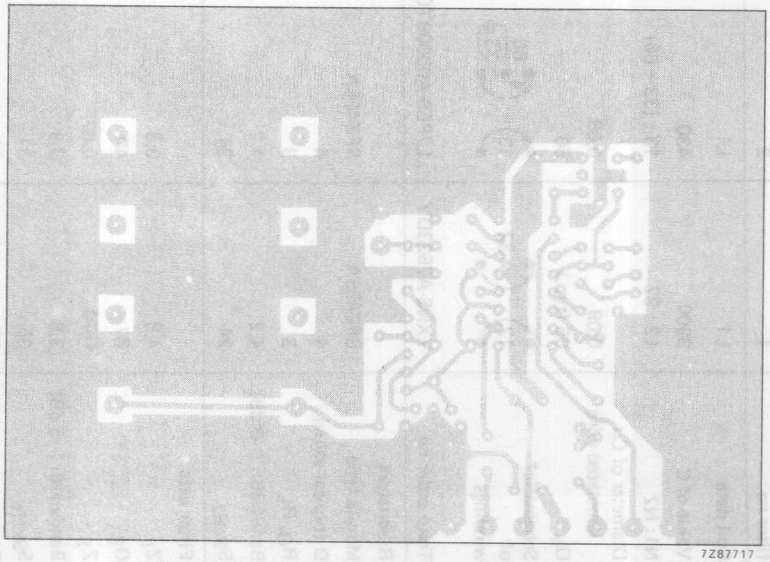
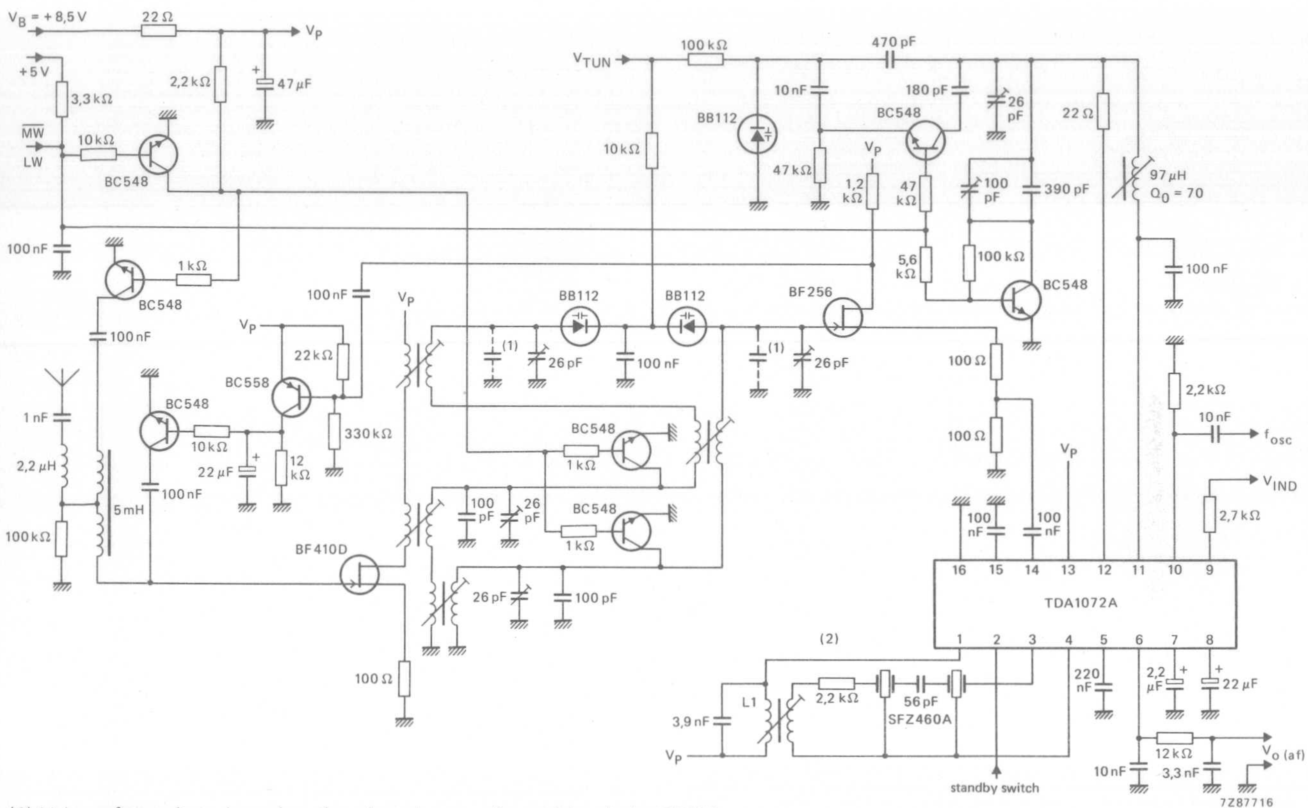



Fig. 17 Printed-circuit board showing track side.




(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

# DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

## GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

### Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_P$ | typ. | 20 | V |
| Supply current (pin 11) | $I_P$ | typ. | 22 | mA |
| Input signal voltage (r.m.s. value) | $V_{i(rms)}$ | max. | 6 | V |
| Output signal voltage (r.m.s. value) | $V_{o(rms)}$ | max. | 6 | V |
| Total harmonic distortion | THD | typ. | 0,05 | % |
| Output noise voltage (r.m.s. value) | $V_{no(rms)}$ | typ. | 50 | $\mu$V |
| Control range | $\Delta\alpha$ | typ. | 110 | dB |
| Cross-talk attenuation (L/R) | $\alpha_{ct}$ | typ. | 80 | dB |
| Ripple rejection (100 Hz) | $\alpha_{100}$ | typ. | 46 | dB |
| Tracking of ganged potentiometers | $\Delta G_v$ | typ. | 0,5 | dB |
| Supply voltage range | $V_P$ | | 7,5 to 23 | V |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

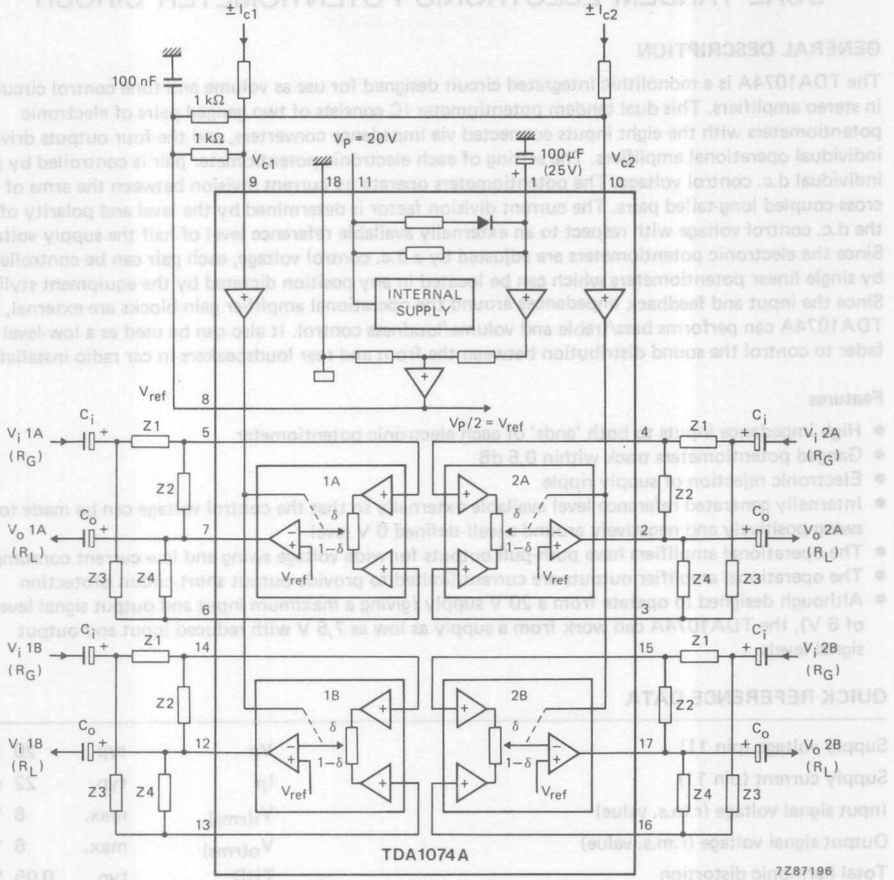



Fig. 1 Block diagram and basic external components; $I_{c1}$ (at pin 9) and $I_{c2}$ (at pin 10) are control input currents; $V_{c1}$ (at pin 9) and $V_{c2}$ (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance $R_G$ = 60 Ω; the output load resistance $R_L$ = 4,7 kΩ; the coupling capacitors at the inputs and outputs are $C_i$ = 2,2 µF and $C_o$ = 10 µF respectively.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 11) | $V_P$ | max. | 23 V |
| Control voltages (pins 9 and 10) | $\pm V_{c1}; \pm V_{c2}$ | max. | 1 V |
| Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16 | $V_i$ | | 0 to $V_P$ V |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From crystal to ambient | $R_{th\ cr\text{-}a}$ | = | 80 K/W |

## REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

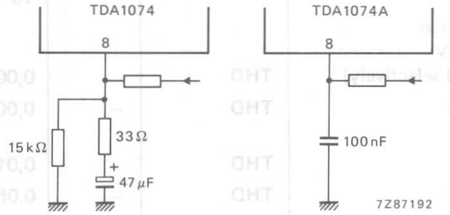



Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

## APPLICATION INFORMATION

**Treble and bass control circuit**

$V_P$ = 20 V; $T_{amb}$ = 25 °C; measured in Fig. 3; $R_G$ = 60 Ω; $R_L$ > 4,7 kΩ; $C_L$ < 30 pF; f = 1 kHz; with a linear frequency response ($V_{c1} = V_{c2}$ = 0 V); unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply current (without load) | $I_P$ | 14 | 22 | 30 | mA |
| Frequency response (−1 dB) $V_{c1} = V_{c2}$ = 0 V | f | 10 | – | 20 000 | Hz |
| Voltage gain at linear frequency response ($V_{c1} = V_{c2}$ = 0 V) | $G_v$* | – | 0 | – | dB |
| Gain variation at f = 1 kHz at maximum bass/treble boost or cut at ± $V_{c1}$ = ± $V_{c2}$ = 120 mV | $\Delta G_v$* | – | ± 1 | – | dB |
| Bass boost at 40 Hz (ref. 1 kHz) $V_{c2}$ = 120 mV | | – | 17,5 | – | dB |
| Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2}$ = 120 mV | | – | 17,5 | – | dB |
| Treble boost at 16 kHz (ref. 1 kHz) $V_{c1}$ = 120 mV | | – | 16 | – | dB |
| Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1}$ = 120 mV | | – | 16 | – | dB |
| Total harmonic distortion at $V_{o(rms)}$ = 300 mV f = 1 kHz (measured selectively) | THD | – | 0,002 | – | % |
| f = 20 Hz to 20 kHz | THD | – | 0,005 | – | % |
| at $V_{o(rms)}$ = 5 V f = 1 kHz | THD | – | 0,015 | 0,1 | % |
| f = 20 Hz to 20 kHz | THD | – | 0,05 | 0,1 | % |
| Signal level at THD = 0,7% (input and output) | $V_{i;\,o(rms)}$ | 5,5 | 6,2 | – | V |
| Power bandwidth at reference level $V_{o(rms)}$ = 5 V (−3 dB); THD = 0,1% | B | – | 40 | – | kHz |
| Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz | $V_{no(rms)}$ | – | 75 | – | μV |
| noise (peak value); weighted to DIN 45 405; CCITT filter | $V_{no(m)}$ | – | 160 | 230 | μV |

* $G_v = V_o/V_i$.

**Treble and bass control circuit**

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Cross-talk attenuation (stereo) | | | | | |
| f = 1 kHz | $\alpha_{ct}$ | – | 86 | – | dB |
| f = 20 Hz to 20 kHz | $\alpha_{ct}$ | – | 80 | – | dB |
| Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV | $-\alpha_{ct}$ | – | 20 | – | dB |
| Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV | $\alpha_{100}$ | – | 46 | – | dB |

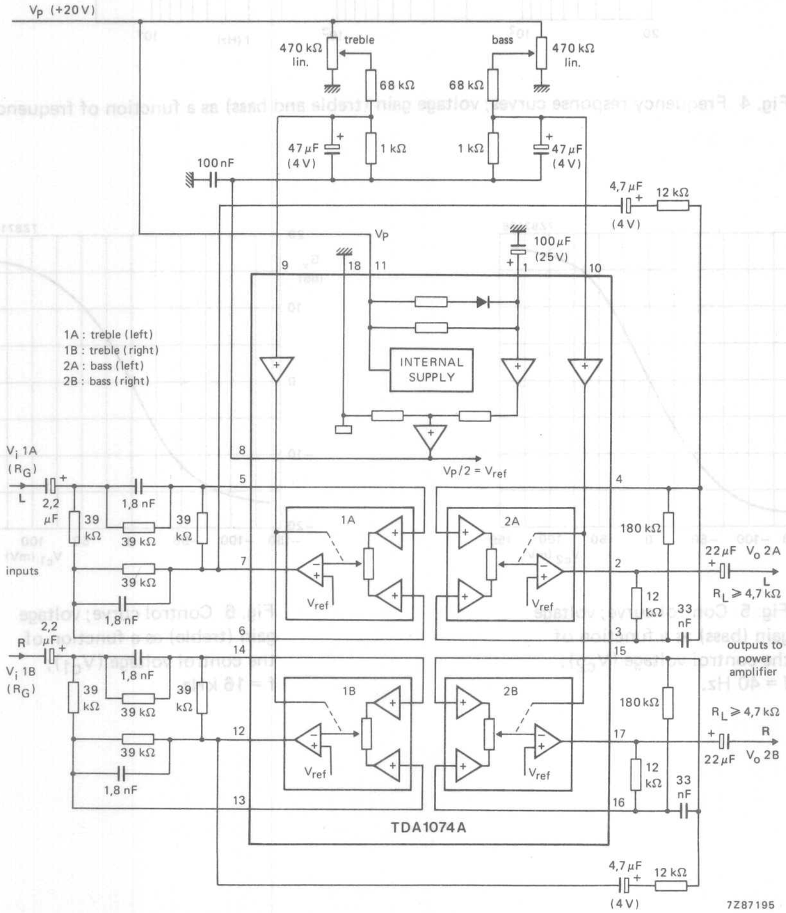



Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

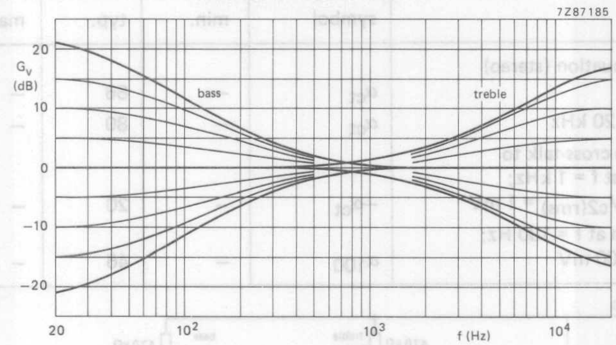



Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

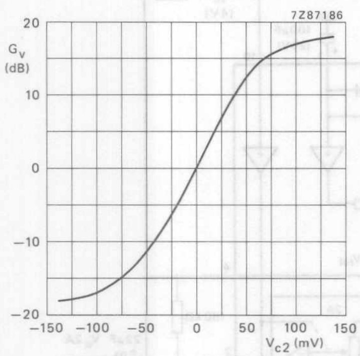



Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage ($V_{c2}$); f = 40 Hz.

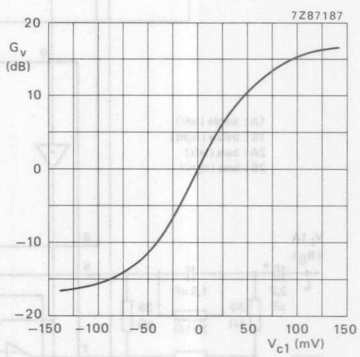
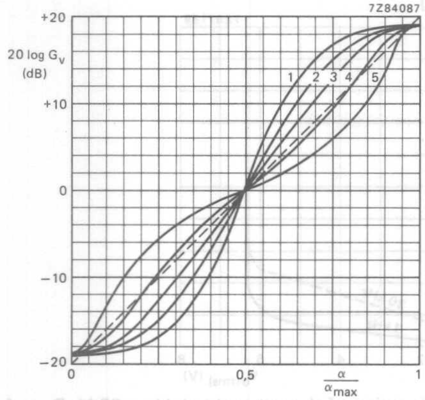



Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage ($V_{c1}$); f = 16 kHz.




| curve no. | value of R |
|---|---|
| 1 | 10 kΩ |
| 2 | 100 kΩ |
| 3 | 220 kΩ |
| 4 | 470 kΩ |
| 5 | 1 MΩ |

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation ($\alpha$) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

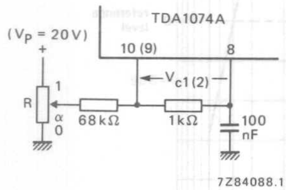



Fig. 8 Circuit diagram for measuring curves in Fig. 7.

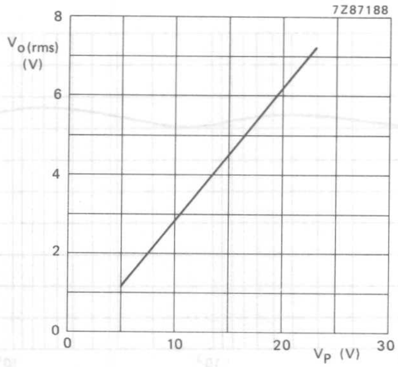



Fig. 9 Output signal level as a function of $V_P$; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

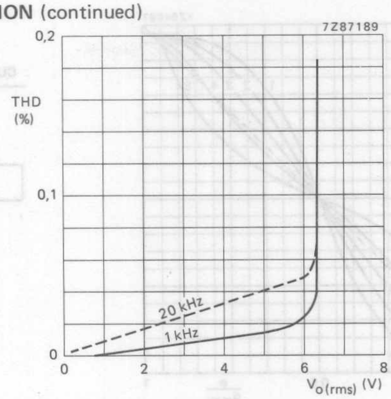



Fig. 10 Total harmonic distortion as a function of the output level; $V_P$ = 20 V; $R_L$ = 4,7 kΩ; $V_{c1}$ = $V_{c2}$ = 0 V (linear, $G_{v\,tot}$ = 1 ). ——— f = 1 kHz; – – – – f = 20 kHz.

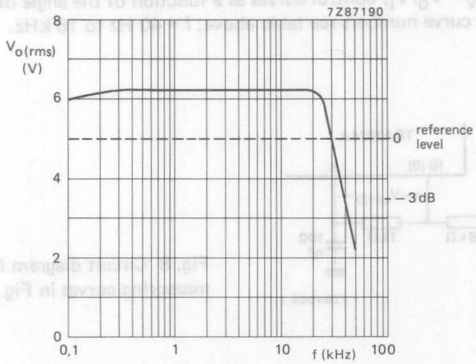



Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

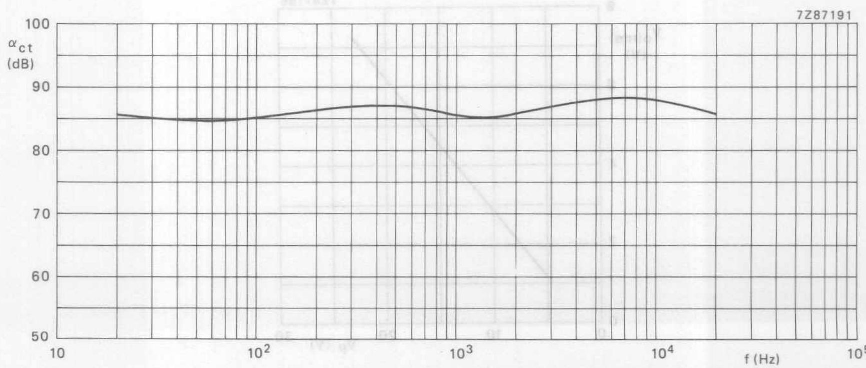
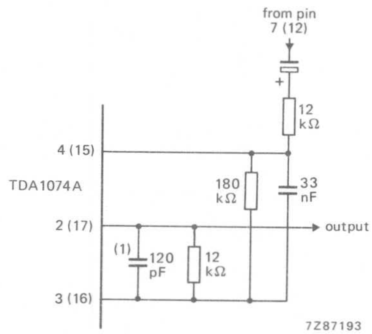



Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1}$ = $V_{c2}$ = 0 V); $V_i$ = 5 V; $R_G$ = 60 Ω; $R_L$ = 4,7 kΩ.

**Application recommendations**

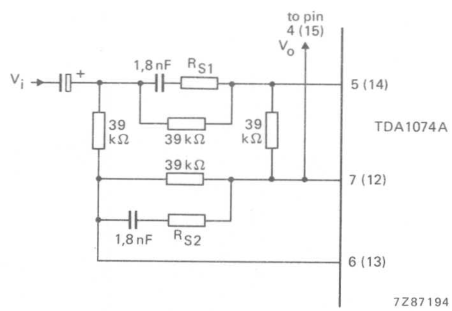
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 ($V_{ref}$).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8($V_{ref}$) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.




(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.




For $R_{S1} = R_{S2} = 3{,}3\ k\Omega$; $f_{-3\,dB} \cong 1$ MHz at linear setting
For $R_{S1} = R_{S2} = 0\ \Omega$; $f_{-3\,dB} \cong 100$ kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

# MOTOR REGULATOR AND FUNCTION CONTROLLER FOR CAR CASSETTE SYSTEMS

The TDA1506 is for car radio/casette players. It incorporates the following functions:

- a motor speed regulator with a multiplication coefficient of k = 20,5.
- an electronic motor stop, controlled by commutator pulses;
- protection circuitry to avoid restarting of the motor after the set is switched to radio reception;
- playback indication;
- tape-end indication with intermittent light;
- fast-wind/rewind circuitry;
- two separately stabilized voltage regulators for the playback amplifier stages;
- a stabilized output voltage for the radio part;
- an automatic switch for switching the preamplifier supply outputs to zero and the radio supply output to a high level at tape-end;
- an output signal for auto-reverse;
- short-circuit protection for all pins to ground at $T_{amb}$ = 30 °C maximum and between output and power supply pin;
- load dump protection.

During fast wind (or rewind) the voltage regulator for the second playback preamplifier is switched off. This feature allows application in an A.P.S.S. (Automatic Program Search System) set. At tape-end and at an externally chosen fixed time before motor stop, the automatic replay output gives a d.c. information signal. This signal may, e.g., be used to control the plunger in an automatic-reverse set. Automatic switching, with all switches to ground.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 10 to 16 | V |
| Operating ambient temperature range | | | | |
| at $V_P$ = 14,4 V | $T_{amb}$ | | −20 to +80 | °C |
| at $V_P$ = 16 V | $T_{amb}$ | | −20 to +60 | °C |
| **Motor regulator** | | | | |
| Regulator supply voltage range | $V_{6\text{-}3}$ | | 3,2 to 12 | V |
| Internal reference voltage | $V_{ref} = V_{6\text{-}5}$ | typ. | 1,38 | V |
| Drop-out voltage | $V_{4\text{-}3}$ | < | 1,8 | V |
| Multiplication coefficient ($\Delta I_4/\Delta I_6$) | k | typ. | 20,5 | |
| **Stabilization radio** | | | | |
| Output voltage | $V_{11\text{-}8}$ | > | 8,5 | V |
| Limited output current | $I_{11\ lim}$ | > | 45 | mA |
| **Stabilization preamplifier I** | | | | |
| Output voltage | $V_{10\text{-}8}$ | > | 7,7 | V |
| Limited output current | $I_{10\ lim}$ | > | 2 | mA |
| **Stabilization preamplifier II** | | | | |
| Output voltage | $V_{9\text{-}8}$ | > | 8,7 | V |
| Limited output current | $I_{9\ lim}$ | > | 20 | mA |
| **Lamp driver** | | | | |
| Output voltage | $V_{2\text{-}8}$ | > | 13 | V |
| Limited output current | $I_{2\ lim}$ | > | 20 | mA |

**PACKAGE OUTLINE** 16-lead DIL; plastic power (SOT-38).

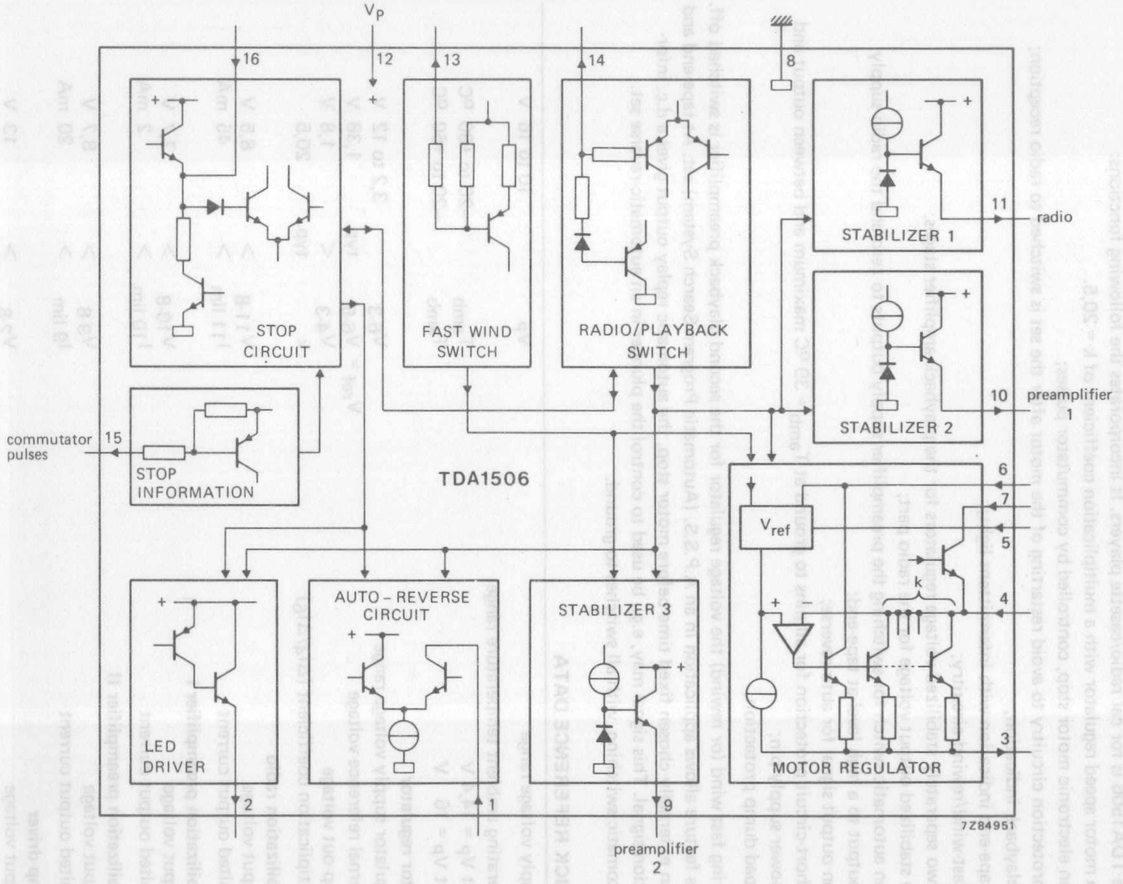



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 24 V |
| Limited output current | $I_{4\ lim}$ | max. | 1 A |
| Power dissipation | see Fig. 2 | | |
| Storage temperature range | $T_{stg}$ | | −65 to + 150 °C |
| Junction temperature | $T_j$ | max. | 150 °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 55 K/W |

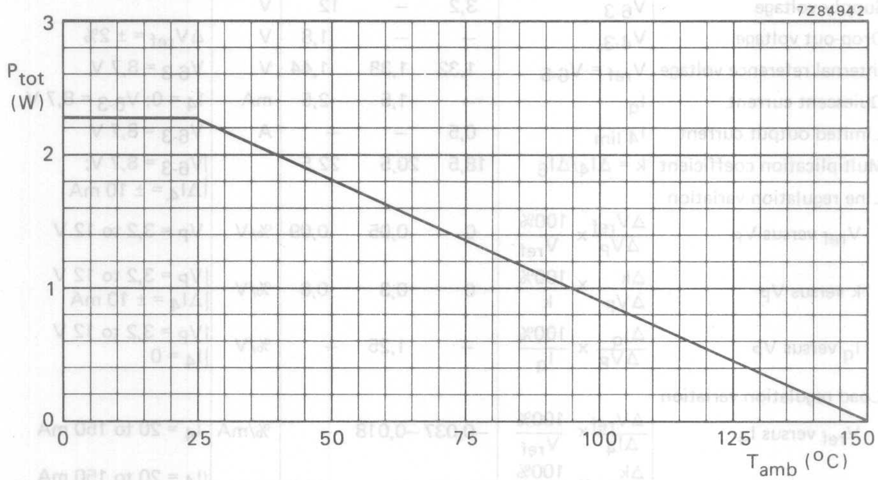



Fig. 2 Power derating curve.

**Note to Fig. 2**

$$P_{tot} = \frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}}$$

$P_{tot}$ in playback position (see Figure 3):

$$P_{tot} \approx I_{12} \times V_P + V_{4\text{-}3}\left(I_m + \frac{V_{ref}}{R_2}\right) + \left(V_{4\text{-}3} + V_{ref}\right)\left(\frac{I_4}{k} + I_q\right) - I_2 \times V_{2\text{-}8} - I_9 \times V_{9\text{-}8} - I_{10} \times V_{10\text{-}8}$$

$P_{tot}$ in radio reception is much lower than $P_{tot}$ in playback.

## CHARACTERISTICS

$V_P$ = 14,4 V; $T_{amb}$ = 25 °C; $I_4$ = 70 mA; $I_{11}$ = 45 mA; $I_{10}$ = 0,3 mA; $I_2$ = 18 mA; $I_9$ = 2 mA; unless otherwise specified; see test circuit Fig. 3.

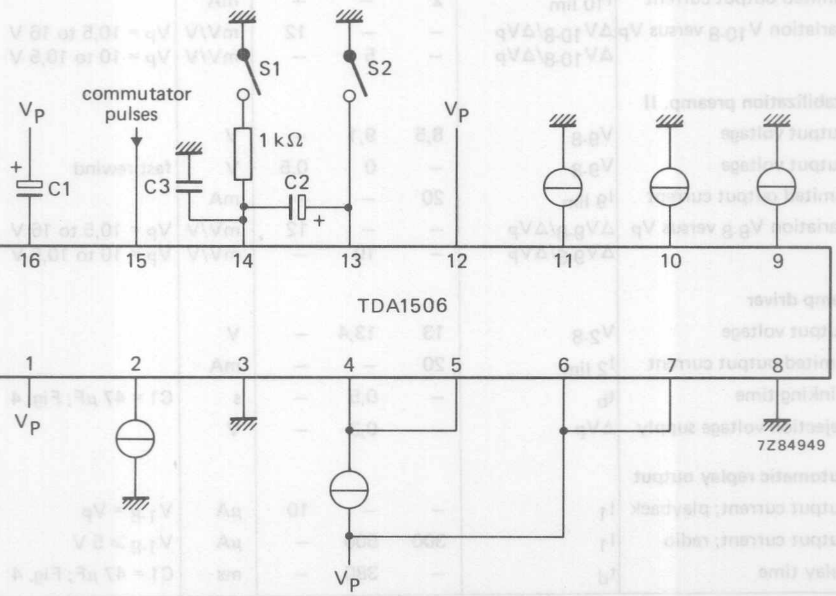
| | symbol | min. | typ. | max. | unit | conditions |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Supply voltage | $V_P$ | 10 * | – | 16 | V | |
| Current consumption | | | | | | |
| at playback | $I_{12}$ | – | – | 38 | mA | $I_4 = 0$ |
| at radio | $I_{12}$ | – | – | 64 | mA | |
| **Motor regulator** | | | | | | |
| Supply voltage | $V_{6\text{-}3}$ | 3,2 | – | 12 | V | |
| Drop-out voltage | $V_{4\text{-}3}$ | – | – | 1,8 | V | $\Delta V_{ref} = \pm 2\%$ |
| Internal reference voltage | $V_{ref} = V_{6\text{-}5}$ | 1,32 | 1,38 | 1,44 | V | $V_{6\text{-}3}$ = 8,7 V |
| Quiescent current | $I_q$ | – | 1,5 | 2,5 | mA | $I_4 = 0$; $V_{6\text{-}3}$ = 8,7 V |
| Limited output current | $I_{4\,lim}$ | 0,5 | – | – | A | $V_{6\text{-}3}$ = 8,7 V |
| Multiplication coefficient | $k = \Delta I_4/\Delta I_6$ | 18,5 | 20,5 | 22,5 | | $V_{6\text{-}3}$ = 8,7 V; $\Delta I_4 = \pm$ 10 mA |
| Line regulation variation | | | | | | |
| $V_{ref}$ versus $V_P$ | $\frac{\Delta V_{ref}}{\Delta V_P} \times \frac{100\%}{V_{ref}}$ | 0 | 0,05 | 0,09 | %/V | $V_P$ = 3,2 to 12 V |
| k versus $V_P$ | $\frac{\Delta k}{\Delta V_P} \times \frac{100\%}{k}$ | 0 | 0,3 | 0,6 | %/V | $V_P$ = 3,2 to 12 V; $\Delta I_4 = \pm$ 10 mA |
| $I_q$ versus $V_P$ | $\frac{\Delta I_q}{\Delta V_P} \times \frac{100\%}{I_q}$ | – | 1,25 | – | %/V | $V_P$ = 3,2 to 12 V; $I_4 = 0$ |
| Load regulation variation | | | | | | |
| $V_{ref}$ versus $I_4$ | $\frac{\Delta V_{ref}}{\Delta I_4} \times \frac{100\%}{V_{ref}}$ | –0,037 | –0,018 | – | %/mA | $I_4$ = 20 to 150 mA |
| k versus $I_4$ | $\frac{\Delta k}{\Delta I_4} \times \frac{100\%}{k}$ | –0,02 | 0 | +0,02 | %/mA | $I_4$ = 20 to 150 mA; $\Delta I_4 = \pm$ 10 mA |
| Temperature coefficient variation | | | | | | |
| $V_{ref}$ versus $T_{amb}$ | $\frac{\Delta V_{ref}}{\Delta T_{amb}} \times \frac{100\%}{V_{ref}}$ | 0 | 0,025 | 0,045 | %/K | $T_{amb}$ = –20 to +80 °C; $V_{6\text{-}3}$ = 8,7 V |
| k versus $T_{amb}$ | $\frac{\Delta k}{\Delta T_{amb}} \times \frac{100\%}{k}$ | –0,016 | 0,008 | 0,032 | %/K | $T_{amb}$ = –20 to +80 °C; $V_{6\text{-}3}$ = 8,7; $\Delta I_4 = \pm$10 mA |
| $I_q$ versus $T_{amb}$ | $\frac{\Delta I_q}{\Delta T_{amb}} \times \frac{100\%}{I_q}$ | – | 0,13 | – | %/K | $T_{amb}$ = –20 to +80 °C; $V_{6\text{-}3}$ = 8,7 V; $I_4 = 0$ |
| Saturation voltage fast winding | $V_{7\text{-}4\,sat}$ | – | 0,18 | – | V | $I_7$ = 10 mA (max. 50 mA) |
| Input current (pin 5) | $I_5$ | – | 19 | – | µA | $V_{6\text{-}3}$ = 8,7 V |

* For starting conditions: min. 6 V.

| | symbol | min. | typ. | max. | unit | conditions |
|---|---|---|---|---|---|---|
| **Automatic motor stop** | | | | | | |
| Output current (pin 15) | $I_{15}$ | 0,4 | – | 0,9 | mA | |
| Time constant | $t_{st}$ | – | 700 | – | ms | C1 = 47 $\mu$F ± 1%; Fig. 4 |
| Switching level | $V_{16\text{-}8}$ | – | 9 | – | V | |
| **Stabilization radio** | | | | | | |
| Output voltage | $V_{11\text{-}8}$ | 8,5 | 8,9 | 9,3 | V | |
| Limited output current | $I_{11\ lim}$ | 45 | – | – | mA | |
| Variation of $V_{11\text{-}8}$ | $\Delta V_{11\text{-}8}$ | – | – | 200 | mV | $V_P$ = 10,5 to 16 V |
| | | – | 100 | – | mV/V | $V_P$ = 10 to 10,5 V |
| Leakage current | $I_{11}$ | – | – | 0,5 | $\mu$A | $R_{11\text{-}8}$ = 100 kΩ |
| | $I_{11}$ | – | – | 4 | $\mu$A | $R_{11\text{-}8}$ = 100 kΩ<br>$T_{amb}$ = 80 °C |
| Temperature coefficient | $\Delta V_{11\text{-}8}/\Delta T_{amb}$ | −2 | 0 | +2 | mV/K | $T_{amb}$ = −20 to +80 °C |
| **Stabilization preamp. I** | | | | | | |
| Output voltage | $V_{10\text{-}8}$ | 7,7 | 8,1 | – | V | |
| Limited output current | $I_{10\ lim}$ | 2 | – | – | mA | |
| Variation $V_{10\text{-}8}$ versus $V_P$ | $\Delta V_{10\text{-}8}/\Delta V_P$ | – | – | 12 | mV/V | $V_P$ = 10,5 to 16 V |
| | $\Delta V_{10\text{-}8}/\Delta V_P$ | – | 5 | – | mV/V | $V_P$ = 10 to 10,5 V |
| **Stabilization preamp. II** | | | | | | |
| Output voltage | $V_{9\text{-}8}$ | 8,5 | 9,1 | – | V | |
| Output voltage | $V_{9\text{-}8}$ | – | 0 | 0,5 | V | fast rewind |
| Limited output current | $I_{9\ lim}$ | 20 | – | | mA | |
| Variation $V_{9\text{-}8}$ versus $V_P$ | $\Delta V_{9\text{-}8}/\Delta V_P$ | – | – | 12 | mV/V | $V_P$ = 10,5 to 16 V |
| | $\Delta V_{9\text{-}8}/\Delta V_P$ | – | 10 | – | mV/V | $V_P$ = 10 to 10,5 V |
| **Lamp driver** | | | | | | |
| Output voltage | $V_{2\text{-}8}$ | 13 | 13,4 | – | V | |
| Limited output current | $I_{2\ lim}$ | 20 | – | – | mA | |
| Blinking time | $t_b$ | – | 0,5 | – | s | C1 = 47 $\mu$F; Fig. 4 |
| Rejection voltage supply | $\Delta V_P$ | – | 0,3 | – | V | |
| **Automatic replay output** | | | | | | |
| Output current; playback | $I_1$ | – | – | 10 | $\mu$A | $V_{1\text{-}8} = V_P$ |
| Output current; radio | $I_1$ | 300 | 500 | – | $\mu$A | $V_{1\text{-}8} \geq 5$ V |
| Delay time | $t_d$ | – | 380 | – | ms | C1 = 47 $\mu$F; Fig. 4 |

CHARACTERISTICS (continued)

| | symbol | min. | typ. | max. | unit | conditions |
|---|---|---|---|---|---|---|
| **Radio playback switch** | | | | | | |
| Switching levels | | | | | | |
| to playback | $V_{14\text{-}8}$ | – | – | 2 | V | $V_P$ = 10 to 16 V |
| to radio | $V_{14\text{-}8}$ | 3,5 | – | – | V | $T_{amb}$ = –20 to +80 °C |
| Input impedance | $\|Z_{14\text{-}8}\|$ | – | 20 | – | kΩ | |
| Output current | $I_{14}$ | – | 200 | – | μA | $V_{14\text{-}8}$ = 0 |
| **Fast wind switch** | | | | | | |
| Switching levels | | | | | | |
| normal to fast | $V_{13\text{-}8}$ | – | – | 2 | V | $V_P$ = 10 to 16 V |
| fast to normal | $V_{13\text{-}8}$ | 6 | – | – | V | $T_{amb}$ = –20 to +80 °C |
| Output voltage; playback | $V_{13\text{-}8}$ | – | 6,8 | – | V | |
| Output current; fast wind | $I_{13}$ | – | 500 | – | μA | $V_{13\text{-}8}$ = 0 |
| Output impedance | $\|Z_{13\text{-}8}\|$ | – | 13 | – | kΩ | |




S1 closed: playback
S1 open: radio reception
S2 closed: fast speed
S2 open: normal speed

C2 is only used with sets on which a fast rewind key is available (C2 = 2,2 μF).
C1 is 200 μF maximum (typ. 47 μF).
C3 = 100 nF.

Fig. 3 Test circuit.

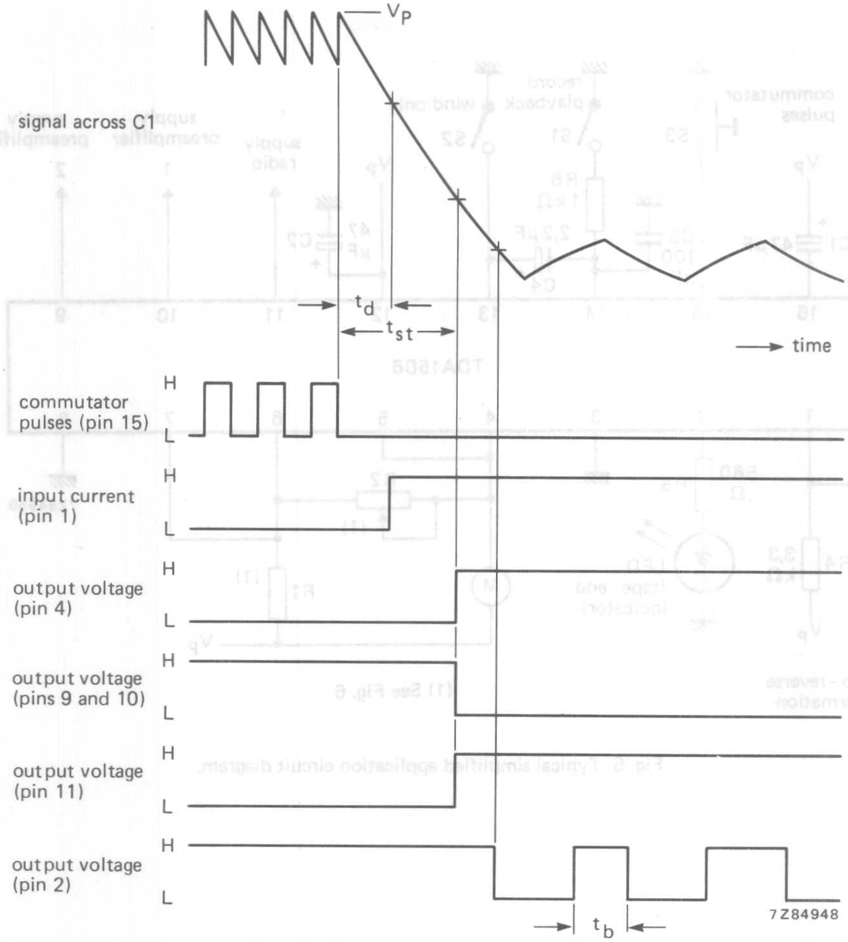



Fig. 4 Waveforms showing signal levels and time constants.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

## APPLICATION INFORMATION

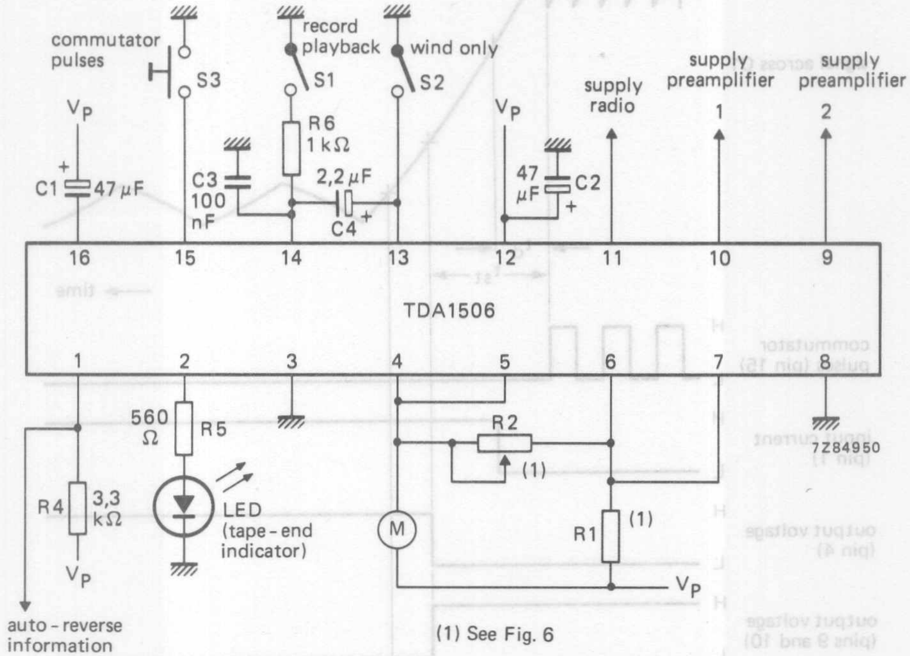
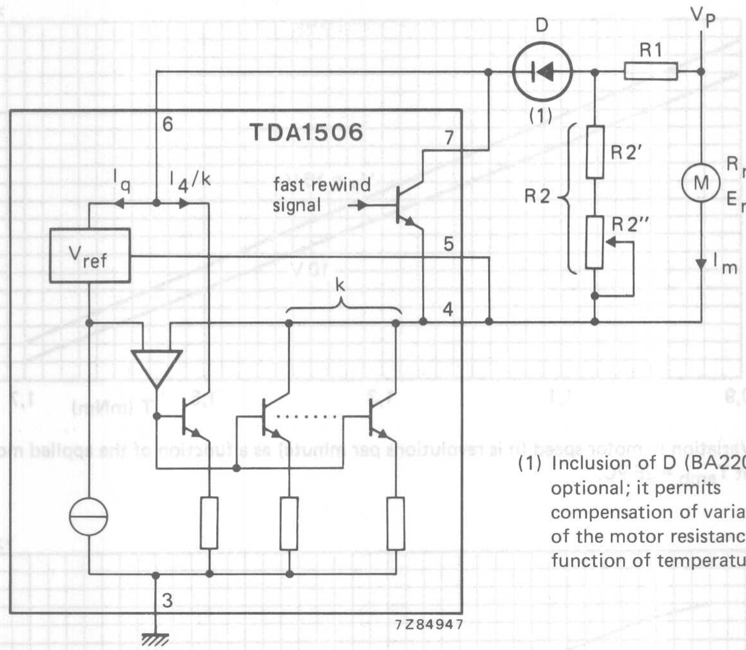



Fig. 5 Typical simplified application circuit diagram.




(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 6 Example of using the TDA1506 (only the motor regulation part is shown) in a d.c. motor speed regulation circuit.

**Notes to Fig. 6**

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$

$I_m = T \times \frac{2\pi}{60} \times \frac{1}{C.\phi}$

where: n = speed in revolutions per minute
C = motor constant
$\phi$ = magnetic flux
$E_n$ = electromotive force
T = motor torque
$R_m$ = motor resistance

**Example:**

$E_n = E_{2400} = 5{,}24$ V(±12,2%)
$R_m = 25{,}6\ \Omega$(±10%)
n = 2400 rev/min
T = 1,3 mNm
R1 = 430 Ω
R2' = 110 Ω
R2'' = 220 Ω

$E_n$ can be expressed (excluding diode D) as:

$$E_n = I_m \left(\frac{R1}{k} - R_m\right) + V_{ref} \left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R1 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m\left(\frac{R1}{k} - R_m\right)}$$

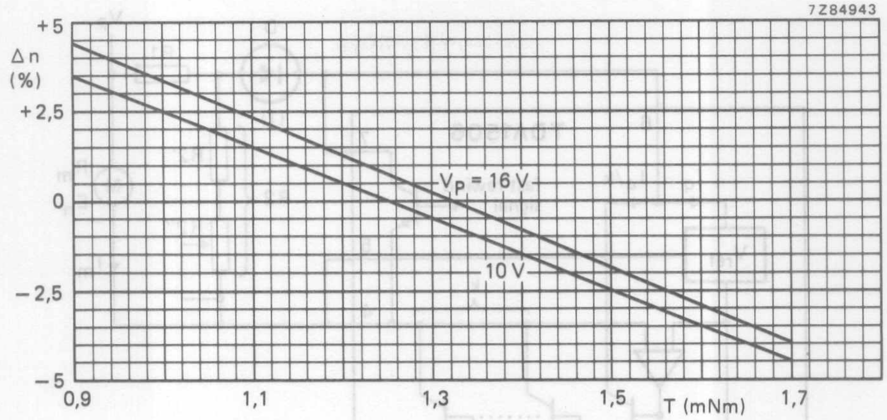



Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at $T_{amb}$ = 25 °C.

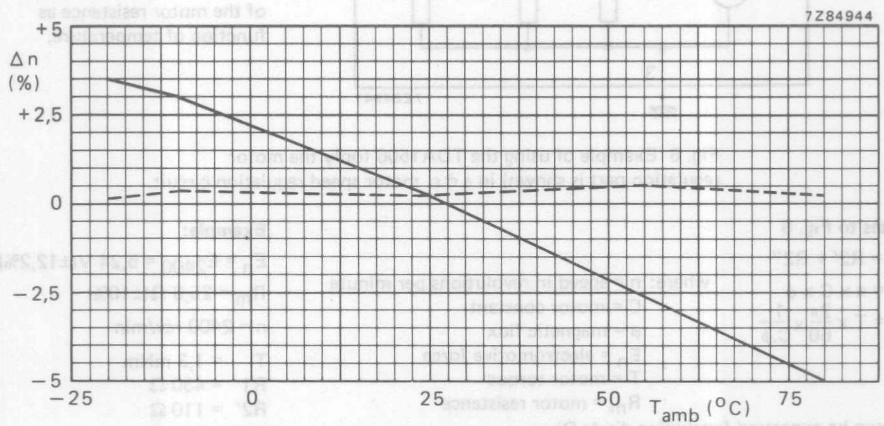



Fig. 8 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1,3 mNm nominal and $V_P$ = 16 V.

————————: with diode D (see Fig. 6).

– – – – – – – –: without diode.

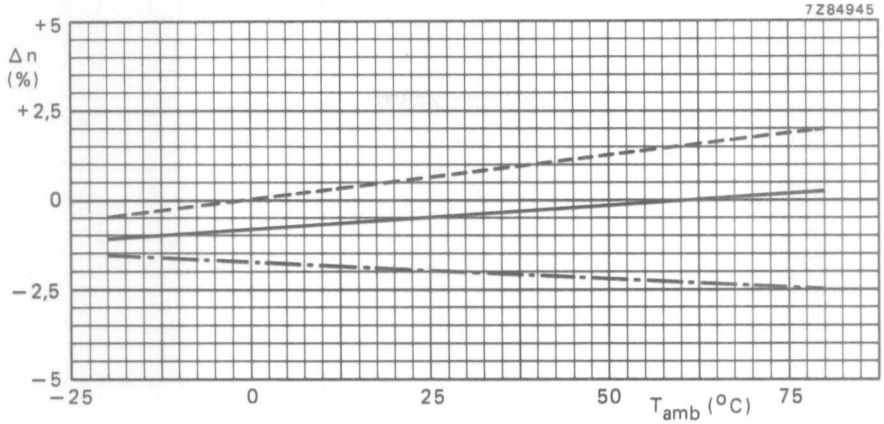



Fig. 9a  $V_P$ = 10 V.

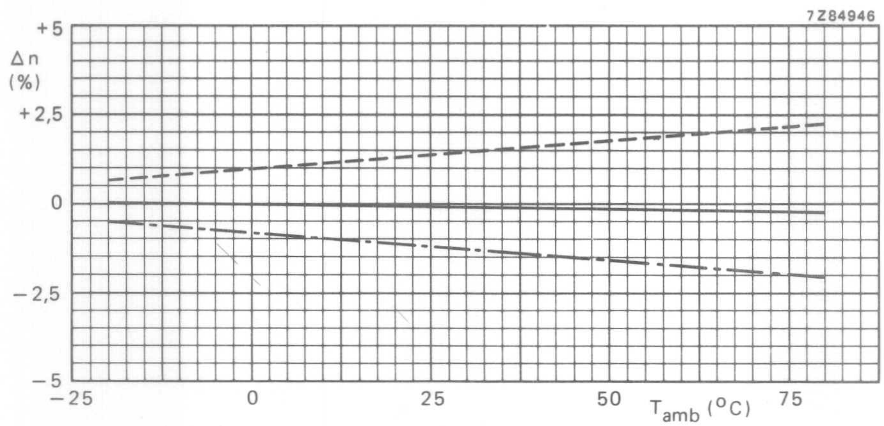



Fig. 9b  $V_P$ = 16 V.

Fig. 9  Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (see Fig. 6).
– – – – – -: T = 1,17 mNm
————: T = 1,30 mNm
—· —· —·-: T = 1,43 mNm

# AUTO–REVERSE CAR RADIO CASSETTE–DECK STEERING CIRCUIT

## GENERAL DESCRIPTION

The TDA1508 is a monolithic integrated circuit generating the steering signals needed for an auto-reverse car radio cassette-deck.

The TDA1508 incorporates the following functions:

- RC-oscillator generating the 250 kHz system clock
- Logic block ($I^2L$)
- Power-on-reset circuit
- Input interface circuits
- Output interface circuits
- Two output voltage stabilizers
- 4 ms motor-pause-pulse
- Fast wind pulse
- Muting pulse
- 1024 ms clock pulse for cassette rotation control.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 7) | $V_P$ | | 10 to 18 | V |
| Supply voltage range, standby (pin 12) | $V_{SB}$ | | 3,5 to 18 | V |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +85 | °C |
| Supply current (pin 7) | $I_P$ | max. | 15 | mA |
| Supply current standby (pin 12) | $I_{SB}$ | typ. | 1,5 | mA |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

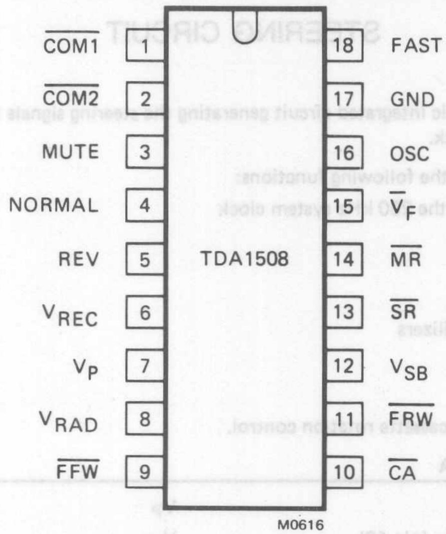



Fig.1 Pinning diagram

**PINNING**

| | | | | | |
|---|---|---|---|---|---|
| 1. | $\overline{COM1}$ | commutator logic input 1 | 10. | $\overline{CA}$ | cassette contact input |
| 2. | $\overline{COM2}$ | commutator logic input 2 | 11. | $\overline{FRW}$ | fast rewind input |
| 3. | MUTE | audio mute output | 12. | $V_{SB}$ | standby supply control input |
| 4. | NORMAL | motor control output | 13. | $\overline{SR}$ | tape-end input |
| 5. | REV | motor control output | 14. | $\overline{MR}$ | manual reverse input |
| 6. | $V_{REC}$ | recording power supply | 15. | $\overline{V_F}$ | radio mode input |
| 7. | $V_P$ | linear part power supply | 16. | OSC | oscillator RC input |
| 8. | $V_{RAD}$ | radio power supply | 17. | GND | ground |
| 9. | $\overline{FFW}$ | fast forward wind input | 18. | FAST | motor control output |

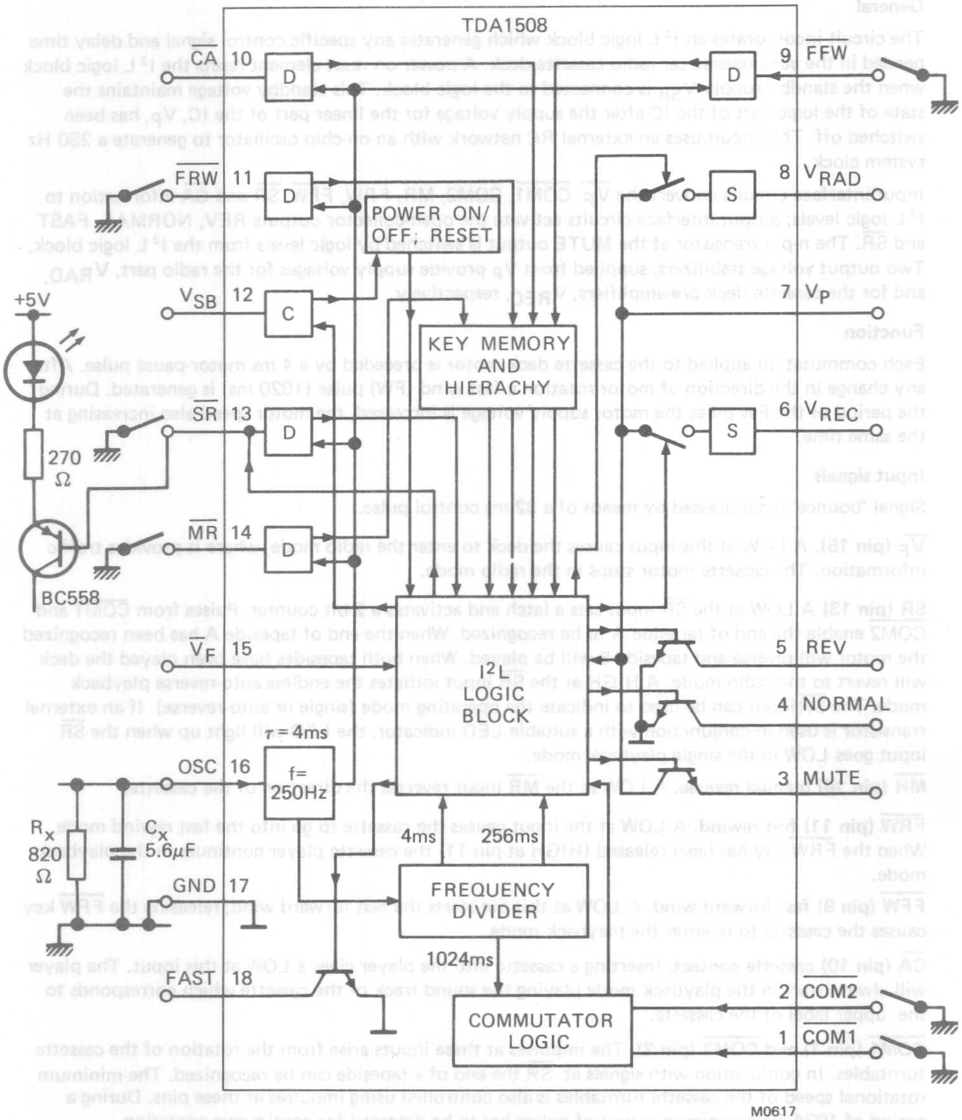



Fig.2 Block diagram

C = control for standby supply;  D = debounce circuit;  S = voltage stabilizer

## FUNCTIONAL DESCRIPTION

### General

The circuit incorporates an $I^2L$ logic block which generates any specific control signal and delay time needed in the auto-reverse car radio cassette-deck. A power-on reset element resets the $I^2L$ logic block when the standby supply $V_{SB}$ is connected to the logic block. This standby voltage maintains the state of the logic part of the IC after the supply voltage for the linear part of the IC, $V_P$, has been switched off. The circuit uses an external RC network with an on-chip oscillator to generate a 250 Hz system clock.

Input interface circuits convert the $\overline{V_F}$, $\overline{COM1}$, $\overline{COM2}$, $\overline{MR}$, $\overline{FRW}$, $\overline{FFW}$, $\overline{SR}$ and $\overline{CA}$ information to $I^2L$ logic levels; output interface circuits activate the open-collector outputs REV, NORMAL, FAST and $\overline{SR}$. The n-p-n transistor at the MUTE output is switched by logic levels from the $I^2L$ logic block. Two output voltage stabilizers, supplied from $V_P$ provide supply voltages for the radio part, $V_{RAD}$, and for the cassette deck pre-amplifiers, $V_{REC}$, respectively.

### Function

Each commutation applied to the cassette deck motor is preceded by a 4 ms motor-pause pulse. After any change in the direction of motor rotation a fast wind (FW) pulse (1020 ms) is generated. During the period of the FW pulse the motor supply voltage is increased, the motor speed also increasing at the same time.

### Input signals

Signal 'bounce' is suppressed by means of a 32 ms control pulse.

**$\overline{V_F}$ (pin 15).** A LOW at this input causes the deck to enter the radio mode, where it provides traffic information. The cassette motor stops in the radio mode.

**$\overline{SR}$ (pin 13)** A LOW at the $\overline{SR}$ input sets a latch and activates a 2-bit counter. Pulses from $\overline{COM1}$ and COM2 enable the end of tapeside A to be recognized. When the end of tapeside A has been recognized the motor will reverse and tapeside B will be played. When both tapesides have been played the deck will revert to the radio mode. A HIGH at the $\overline{SR}$ input initiates the endless auto-reverse playback mode. The $\overline{SR}$ input can be used to indicate the operating mode (single or auto-reverse). If an external transistor is used in conjunction with a suitable LED indicator, the LED will light up when the $\overline{SR}$ input goes LOW in the single playback mode.

**$\overline{MR}$ (pin 14) manual reverse.** A LOW at the $\overline{MR}$ input reverses the direction of the cassette.

**$\overline{FRW}$ (pin 11) fast rewind.** A LOW at the input causes the cassette to go into the fast rewind mode. When the $\overline{FRW}$ key has been released (HIGH at pin 11) the cassette player continues in the playback mode.

**$\overline{FFW}$ (pin 9) fast forward wind.** A LOW at this pin starts the fast forward wind; releasing the $\overline{FFW}$ key causes the cassette to re-enter the playback mode.

**$\overline{CA}$ (pin 10) cassette contact.** Inserting a cassette into the player gives a LOW at this input. The player will always start in the playback mode playing the sound track of the cassette which corresponds to the upper label of the cassette.

**$\overline{COM1}$ (pin 1) and $\overline{COM2}$ (pin 2).** The impulses at these inputs arise from the rotation of the cassette turntables. In conjunction with signals at $\overline{SR}$ the end of a tapeside can be recognized. The minimum rotational speed of the cassette turntables is also controlled using impulses at these pins. During a period of 1024 ms a minimum count of pulses has to be detected for continuous operation.

**$V_P$ (pin 7) supply voltage for linear part.** When $V_P$ is LOW the output functions ($V_{REC}$, $V_{RAD}$, NORMAL, REV, FAST, $\overline{SR}$-indication) are inactive. The switching levels for $V_P$ are shown in Fig. 5. The MUTE transistor remains active independent of the value of $V_P$, when the audio mute is required.

**Output signals**

**FAST (pin 18), NORMAL (pin 4), REV (pin 5).** These open-collector outputs steer the motor control of the cassette deck.

**MUTE (pin 3).** The audio output of the cassette is muted in the radio mode and during any change in motor rotation (reverse, fast forward wind, etc). The n-p-n transistor (Fig.2) is switched to $V_P$ when muting is required. The audio frequency is muted up to 128 ms after the change of mode or motor rotation.

**$V_{REC}$ (pin 6), $V_{RAD}$ (pin 8).** These stabilized supply voltages are derived from $V_P$ and provide power for the recording and radio part of the cassette system respectively When $V_{RAD}$ is active $V_{REC}$ is switched off and when $V_{REC}$ is active $V_{RAD}$ is switched off.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | | |
|---|---|---|---|---|
| Supply voltage linear (pin 7) | $V_P = V_{7-17}$ | max. | 24 | V |
| Supply voltage standby (pin 12) | $V_{SB} = V_{12-17}$ | max. | 24 | V |
| All inputs (pins 1,2,9,10,11,13,14 and 15) | $V_{1,2,9,10,11,13,14,15-17}$ | max. | 24 | V |
| All inputs (pins 3,4,5,6,8,13 and 18) | $V_{3,4,5,6,8,13,18-17}$ | max. | 24 | V |
| Storage temperature range | $T_{stg}$ | | −55 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +85 | °C |

## CHARACTERISTICS

Supply voltage $V_P$ = 14 V; $V_{SB}$ = 18 V; $T_{amb}$ = 25 °C

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Linear supply (pin 7)** | | | | | |
| Supply voltage linear | $V_P$ | 10 | 14 | 18 | V |
| Supply current linear for $I_{(V_{RAD})}$ and $I_{(V_{REC})}$ = 0 | $I_P$ | – | – | 15 | mA |
| **Supply standby (pin 12)** | | | | | |
| Supply voltage standby | $V_{SB}$ | 3,5 | – | 18 | V |
| Supply current standby | $I_{SB}$ | – | 1,5 | 2,5 | mA |
| Power-on-reset | | | see Fig.3 | | |
| Power-off-reset | | | see Fig.4 | | |
| Time constant of RC-combination at $V_{SB}$ for power-on-reset | $\tau$ | 300 | – | – | μs |
| **Oscillator** | | | | | |
| Oscillator frequency ($R_x$ = 820 kΩ; $C_x$ = 5,6 nF) | $f_{osc}$ | – | 250 | – | Hz |
| Oscillator frequency drift over temperature and supply voltage range | $\Delta f_{osc}/f_{osc}$ | −20 | – | +20 | % |
| External components | $R_x$ | 680 | 820 | – | kΩ |
| | $C_x$ | – | 5,6 | 22 | nF |
| Oscillator a.c. voltage (peak-to-peak value) | $V_{osc(p-p)}$ | – | – | 1,0 | V |
| **Inputs** | | | | | |
| $\overline{COM1}$, $\overline{FFW}$, $\overline{FRW}$, $\overline{MR}$ | | | | | |
| $\overline{COM2}$, $\overline{V_F}$ and $\overline{SR}$ | | | | | |
| $\overline{CA}$ | | | | | |
| HIGH (inactive) | $V_{IH}$ | 2,5 | – | $V_P$ | V |
| (for $V_{IH} < V_P - 1.5$ V) | $-I_{IH}$ | 50 | 100 | 200 | μA |
| LOW (active) | $V_{IL}$ | – | – | 0,6 | V |
| | $-I_{IL}$ | 50 | 100 | 200 | μA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Outputs** | | | | | |
| NORMAL, REV (open collector) | | | | | |
| Output active saturation voltage ($I_{sat}$ < 7 mA) | $V_{4-17sat}$ | – | – | 0,3 | V |
| | $V_{5-17sat}$ | – | – | 0,3 | V |
| FAST | | | | | |
| Output active saturation voltage ($I_{sat}$ < 25 mA) | $V_{18-17sat}$ | – | – | 0,3 | V |
| MUTE | | | | | |
| Output voltage (n-p-n transistor switched to $V_P$) | $V_{3-17}$ | – | $V_P-2$ | – | V |
| Output current external resistor | $-I_3$ | 5 | – | – | mA |
| MUTE | | | | | |
| Output inactive voltage | $V_{3-17}$ | 0 | – | – | V |
| Output inactive current | $-I_3$ | – | 0 | 10 | μA |
| $\overline{SR}$ as output stage (open collector) | | | | | |
| Saturation voltage at $I_{sat}$ = 1 mA | $V_{13-17sat}$ | – | – | 0,4 | V |
| Inactive current | $-I_{13}$ | – | – | 10 | μA |
| **Stabilized output voltages** | | | | | |
| $V_{RAD}$ voltage | $V_{6-17}$ | 8,1 | 8,5 | 8,9 | V |
| $V_{REC}$ voltage | $V_{8-17}$ | 8,1 | 8,5 | 8,9 | V |
| Output current (foldback) | $I_6$ | 45 | – | – | mA |
| | $I_8$ | 45 | – | – | mA |
| Ripple rejection, f = 100 Hz $V_P$ = 10 to 18 V | $\frac{V_{6-17}}{V_{7-17}}$ | – | – | 20 | mV/V |
| | $\frac{V_{8-17}}{V_{7-17}}$ | – | – | 20 | mV/V |
| Temperature drift | $\frac{V_{6-17}}{T_{amb}}$ | –2 | – | +2 | mV/K |
| | $\frac{V_{8-17}}{T_{amb}}$ | –2 | – | +2 | mV/K |
| Input resistance (I = 50 mA) | $R_i$ | – | 1 | – | Ω |
| Stabilizer inactive currents | $-I_{RAD}$ | 100 | – | – | μA |
| | $-I_{REC}$ | 100 | – | – | μA |

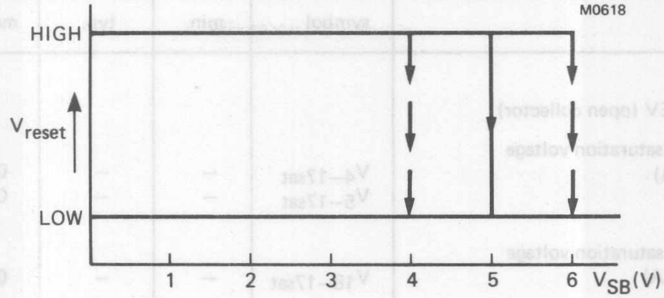



Fig.3 Power-on-reset.

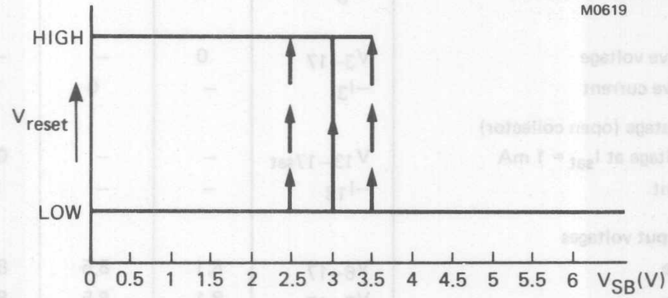



Fig.4 Power-off-reset.

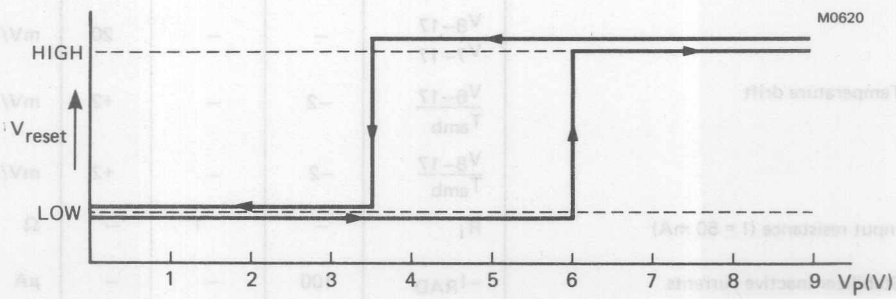



Fig.5 Switching levels for supply voltage monitoring.

# 24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1510 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage $V_P$ = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use — stereo as well as mono BTL
- high output power
- low offset voltage at the output (important for BTL)
- large useable gain variation
- very good ripple rejection
- load dump protection
- a.c. short-circuit safe to ground
- thermal protection
- internal limited bandwidth for high frequencies
- low stand-by current possibility, to simplify required switches
- low number and small sized external components
- high reliability

## QUICK REFERENCE DATA

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range (operating) | $V_P$ | | 6 to 18 | | V |
| Supply voltage (non-operating) | $V_P$ | max. | 28 | | V |
| Supply voltage (non-operating; load dump protection) | $V_P$ | max. | 45 | | V |
| Repetitive peak output current | $I_{ORM}$ | max. | 4 | | A |
| Total quiescent current | $I_{tot}$ | typ. | 75 | | mA |
| Stand-by current | $I_{sb}$ | < | 2 | | mA |
| Switch-on current | $I_{so}$ | typ. | 0,35 | | mA |
| Input impedance | $\|Z_i\|$ | > | 1 | | MΩ |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | | °C |
| Crystal temperature | $T_c$ | max. | 150 | | °C |
| **Bridge tied load application (BTL)** | $V_P$ | = | 14,4 | 13,2 | V |
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | | |
| **$d_{tot}$ = 0,5%** | $P_o$ | typ. | 18 | 15 | W |
| $d_{tot}$ = 10% | $P_o$ | typ. | 24 | 20 | W |
| Supply voltage ripple rejection; $R_S$ = 0; f = 1 kHz | RR | typ. | 50 | 50 | dB |
| D.C. output offset voltage between the outputs | $\|\Delta V_{5\text{-}9}\|$ | < | 50 | 50 | mV |
| **Stereo application** | | | | | |
| Output power at $d_{tot}$ = 10% (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 7 | 6 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 12 | 10 | W |
| Output power at **$d_{tot}$ = 0,5%** (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 | 4,5 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 9,0 | 7,5 | W |
| Channel separation | α | > | 40 | 40 | dB |
| Noise output voltage; $R_S$ = 10 kΩ; according to IEC curve-A | $V_n$ | typ. | 0,2 | 0,2 | mV |

## PACKAGE OUTLINE

13-lead SIL; plastic power (SOT-141B).

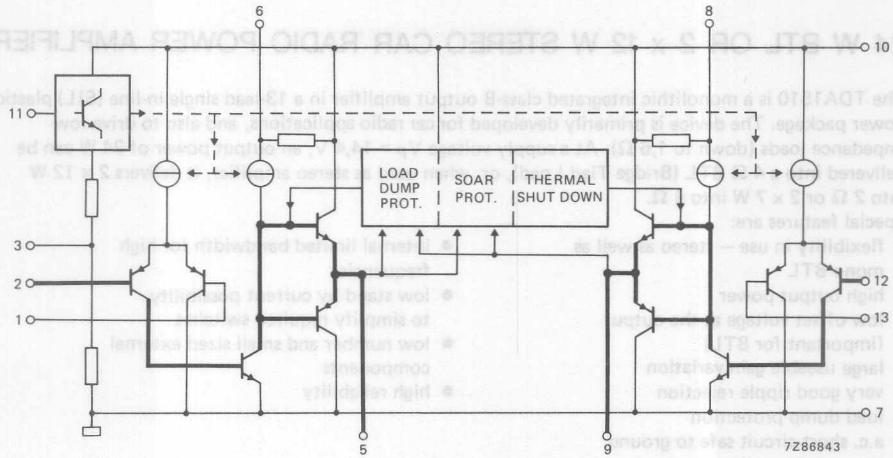



Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.
Pin 4 is internally connected.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage; operating (pin 10) | $V_P$ | max. | 18 | V |
| Supply voltage; non-operating | $V_P$ | max. | 28 | V |
| Supply voltage; during 50 ms (load dump protection) | $V_P$ | max. | 45 | V |
| Peak output current | $I_{OM}$ | max. | 6 | A |
| Total power dissipation | see derating curve Fig. 2 | | | |
| Storage temperature range | $T_{stg}$ | −55 to + 150 | | °C |
| Crystal temperature | $T_c$ | max. | 150 | °C |

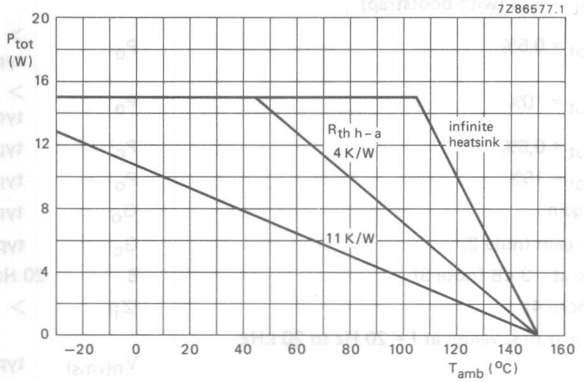



Fig. 2 Power derating curves.

## HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

$T_{amb}$ = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

$T_{amb}$ = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 10) | $V_P$ | | 6 to 18 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 4 | A |
| Total quiescent current | $I_{tot}$ | typ. | 75 | mA |
| | | < | 150 | mA |
| Stand-by current | $I_{sb}$ | < | 2 | mA |
| Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1) | $I_{so}$ | typ. | 0,35 | mA |
| | | < | 0,8 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 14,4 V; f = 1 kHz; unless otherwise specified

**Bridge tied load application (BTL)**; see Fig. 3

| | | | | |
|---|---|---|---|---|
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | |
| $V_P$ = 14,4 V; $\mathbf{d_{tot}}$ **= 0,5%** | $P_o$ | > | 15,5 | W |
| | | typ. | 18,0 | W |
| $V_P$ = 14,4 V; $d_{tot}$ = 10% | $P_o$ | > | 20 | W |
| | | typ. | 24 | W |
| $V_P$ = 13,2 V; $\mathbf{d_{tot}}$ **= 0,5%** | $P_o$ | typ. | 15 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 10% | $P_o$ | typ. | 20 | W |
| Open loop voltage gain | $G_o$ | typ. | 75 | dB |
| Closed loop voltage gain (note 2) | $G_c$ | typ. | 40 (± 0,5) | dB |
| Frequency response at −3 dB (note 3) | B | 20 Hz to | min. 20 | kHz |
| Input impedance (note 4) | $\lvert Z_i \rvert$ | > | 1 | MΩ |
| Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,2 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,35 | mV |
| | | < | 0,8 | mV |
| $R_S$ = 10 kΩ; according to IEC 179 curve A | $V_n$ | typ. | 0,25 | mV |
| Supply voltage ripple rejection (note 5) f = 100 Hz | RR | > | 42 | dB |
| | | typ. | 50 | dB |
| D.C. output offset voltage between the outputs | $\lvert \Delta_{5\text{-}9} \rvert$ | < | 50 | mV |
| | | typ. | 2 | mV |
| Loudspeaker protection (if one of the 2 outputs is short-circuited to ground) maximum d.c. voltage (across the load) | $\lvert \Delta V_{5\text{-}9} \rvert$ | < | 1 | V |
| Power bandwidth; −1 dB; $\mathbf{d_{tot}}$ **= 0,5%** | B | | 30 Hz to 40 | kHz |

**Stereo application**; see Fig. 4

| | | | |
|---|---|---|---|
| Output power at $d_{tot}$ = 10%; with bootstrap (note 6) | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | > <br> typ. | 6 W <br> 7 W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | > <br> typ. | 10 W <br> 12 W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6 W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 10 W |
| Output power at $d_{tot}$ = 0,5%; with bootstrap (note 6) | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | typ. | 9,0 W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,5 W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 7,5 W |
| Output power at $d_{tot}$ = 10%; without bootstrap | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω (notes 6, 8 and 9) | $P_o$ | typ. | 6 W |
| Frequency response; –3 dB (note 3) | B | 40 Hz to min. | 20 kHz |
| Supply voltage ripple rejection (note 5) | | | |
| f = 1 kHz | RR | typ. | 50 dB |
| Channel separation; $R_S$ = 10 kΩ; f = 1 kHz | α | > <br> typ. | 40 dB <br> 50 dB |
| Closed loop voltage gain (note 7) | $G_c$ | typ. | 40 dB |
| Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,15 mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,25 mV |
| $R_S$ = 10 kΩ; according to IEC curve A | $V_n$ | typ. | 0,2 mV |

**Notes**

1. If $V_{11} > V_{10}$, then $I_{11}$ must be ⩽ 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (or 8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

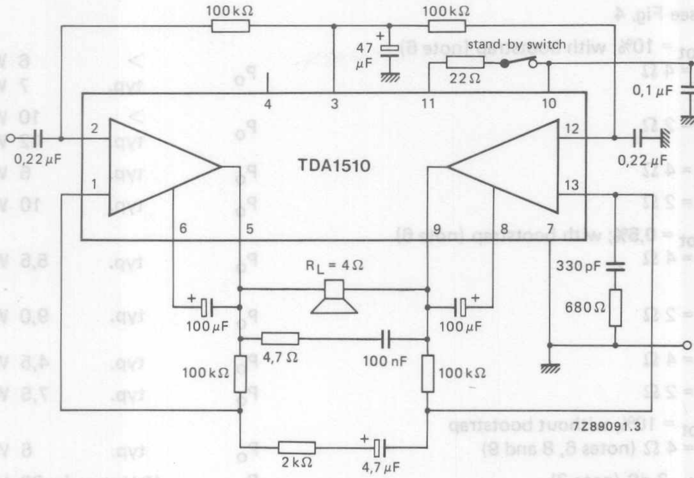



Fig. 3 Test and application circuit bridge tied load (BTL).

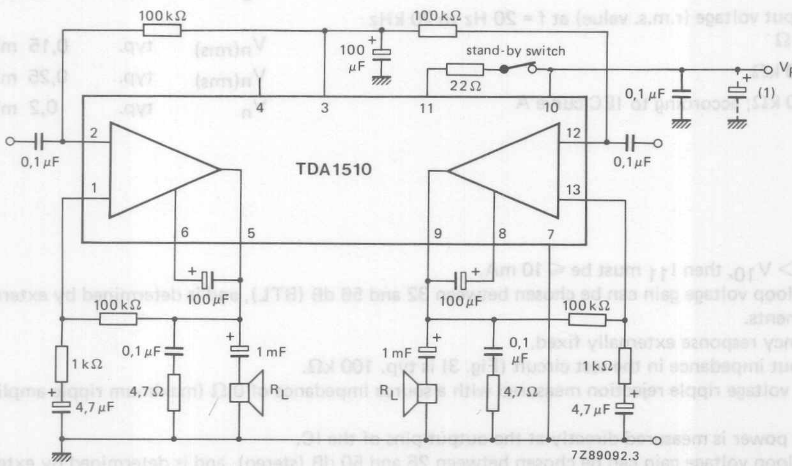



Fig. 4 Test and application circuit stereo mode.

(1) Belongs to power supply.

# 12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 | V |
| Total quiescent current at $V_P$ = 25 V | $I_{tot}$ | typ. | 65 | mA |
| Output power at $d_{tot}$ = 0,7% | | | | |
| sine-wave power | | | | |
| $V_P$ = 25 V; $R_L$ = 4 Ω | $P_o$ | typ. | 13 | W |
| $V_P$ = 25 V; $R_L$ = 8 Ω | $P_o$ | typ. | 7 | W |
| music power | | | | |
| $V_P$ = 32 V; $R_L$ = 4 Ω | $P_o$ | typ. | 21 | W |
| $V_P$ = 32 V; $R_L$ = 8 Ω | $P_o$ | typ. | 12 | W |
| Closed-loop voltage gain (externally determined) | $G_c$ | typ. | 30 | dB |
| Input resistance (externally determined) | $R_i$ | typ. | 20 | kΩ |
| Signal-to-noise ratio at $P_o$ = 50 mW | S/N | typ. | 72 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 50 | dB |

## PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

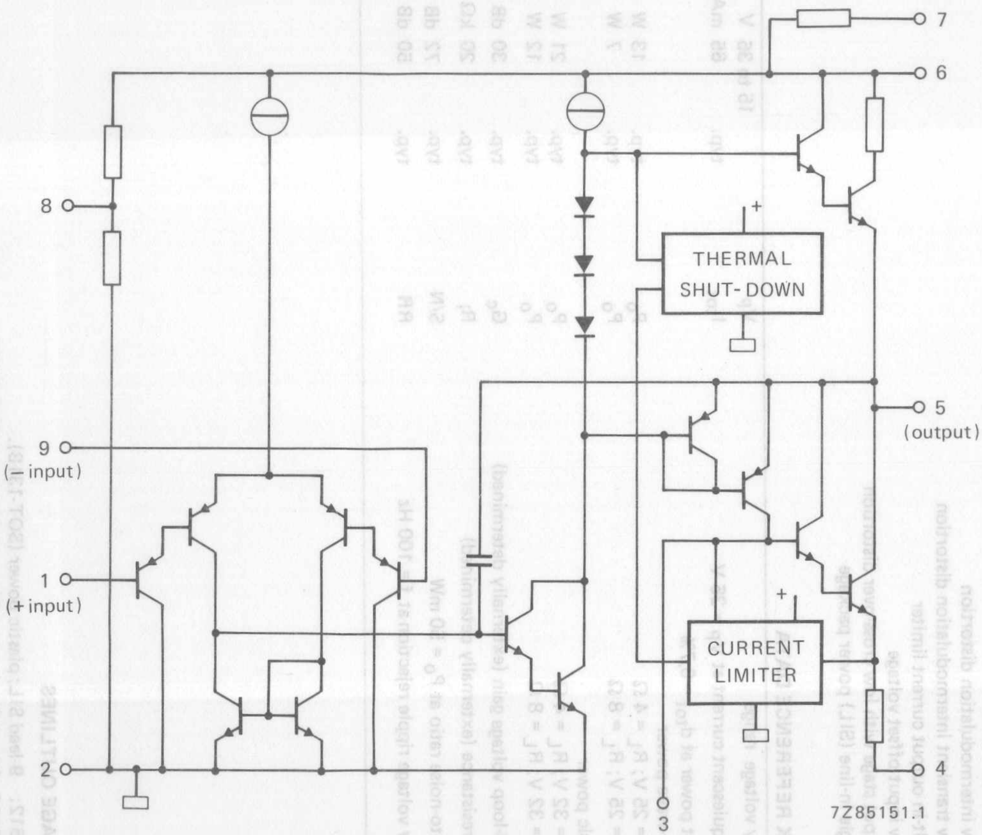



Fig. 1 Simplified internal circuit diagram.

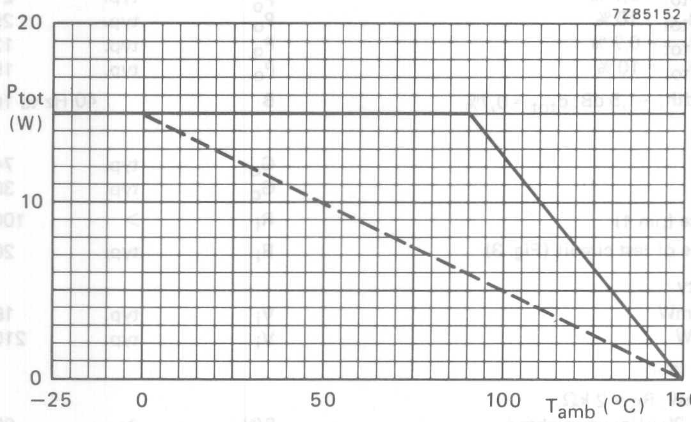
**PINNING**

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply ($V_P$)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 35 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 3,2 A |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 5 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$ | $t_{sc}$ | max. | 100 hours |




——— mounted on infinite heatsink.

– – – – mounted on heatsink of 6 K/W.

Fig. 2 Power derating curves.

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | typ. | 3 K/W |
| | | ≤ | 4 K/W |

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 | V |
| Total quiescent current at $V_P$ = 25 V | $I_{tot}$ | typ. | 65 | mA |

## A.C. CHARACTERISTICS

$V_P$ = 25 V; $R_L$ = 4 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Output power | | | | |
| sine-wave power at $d_{tot}$ = 0,7 % | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 13 | W |
| $R_L$ = 8 Ω | $P_o$ | typ. | 7 | W |
| music power at $V_P$ = 32 V | | | | |
| $R_L$ = 4 Ω; $d_{tot}$ = 0,7 % | $P_o$ | typ. | 21 | W |
| $R_L$ = 4 Ω; $d_{tot}$ = 10 % | $P_o$ | typ. | 25 | W |
| $R_L$ = 8 Ω; $d_{tot}$ = 0,7 % | $P_o$ | typ. | 12 | W |
| $R_L$ = 8 Ω; $d_{tot}$ = 10 % | $P_o$ | typ. | 15 | W |
| Power bandwidth; −1,5 dB; $d_{tot}$ = 0,7% | B | | 40 Hz to 16 | kHz |
| Voltage gain | | | | |
| open-loop | $G_o$ | typ. | 74 | dB |
| closed-loop | $G_c$ | typ. | 30 | dB |
| Input resistance (pin 1) | $R_i$ | > | 100 | kΩ |
| Input resistance of test circuit (Fig. 3) | $R_i$ | typ. | 20 | kΩ |
| Input sensitivity | | | | |
| for $P_o$ = 50 mW | $V_i$ | typ. | 16 | mV |
| for $P_o$ = 10 W | $V_i$ | typ. | 210 | mV |
| Signal-to-noise ratio | | | | |
| at $P_o$ = 50 mW; $R_S$ = 2 kΩ; f = 20 Hz to 20 kHz; unweighted | S/N | > | 68 | dB |
| weighted; measured according to IEC 173 (A-curve) | S/N | typ. | 76 | dB |
| Ripple rejection at f = 100 Hz | RR | typ. | 50 | dB |
| Total harmonic distortion at $P_o$ = 10 W | $d_{tot}$ | typ. | 0,1 | % |
| | | < | 0,3 | % |
| Output resistance (pin 5) | $R_o$ | typ. | 0,1 | Ω |

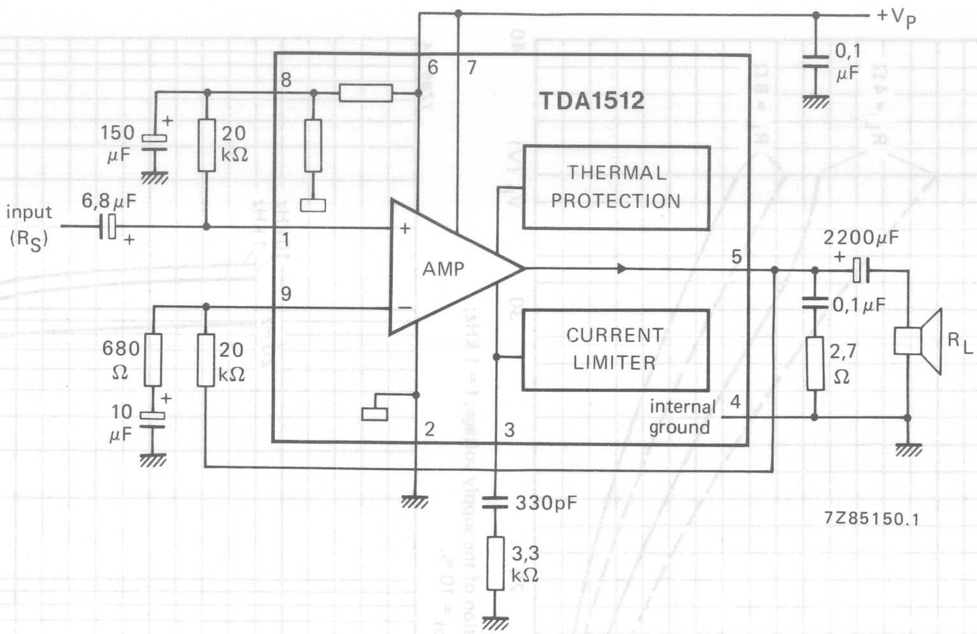



Fig. 3 Test circuit.

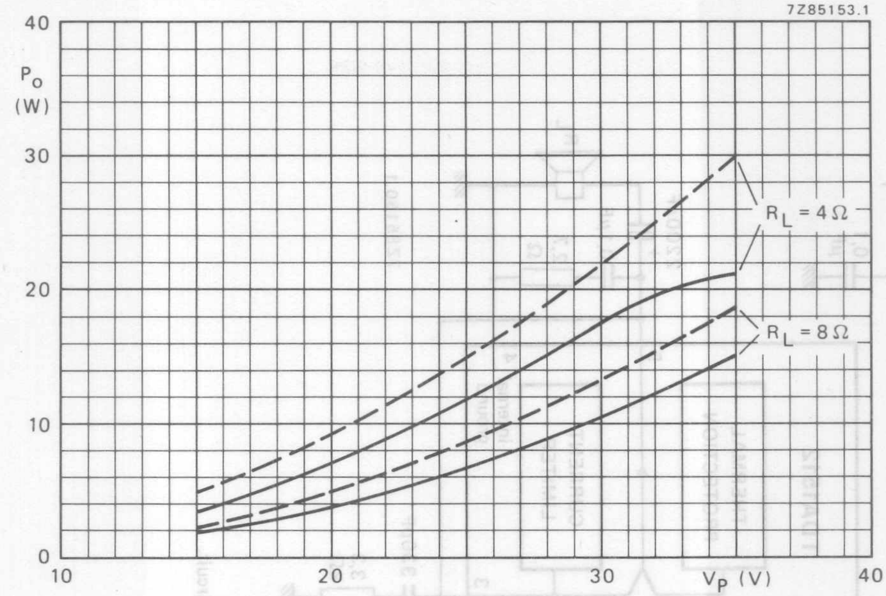



Fig. 4 Output power as a function of the supply voltage; f = 1 kHz; ——— $d_{tot}$ = 0,7 %; — — — $d_{tot}$ = 10 %.

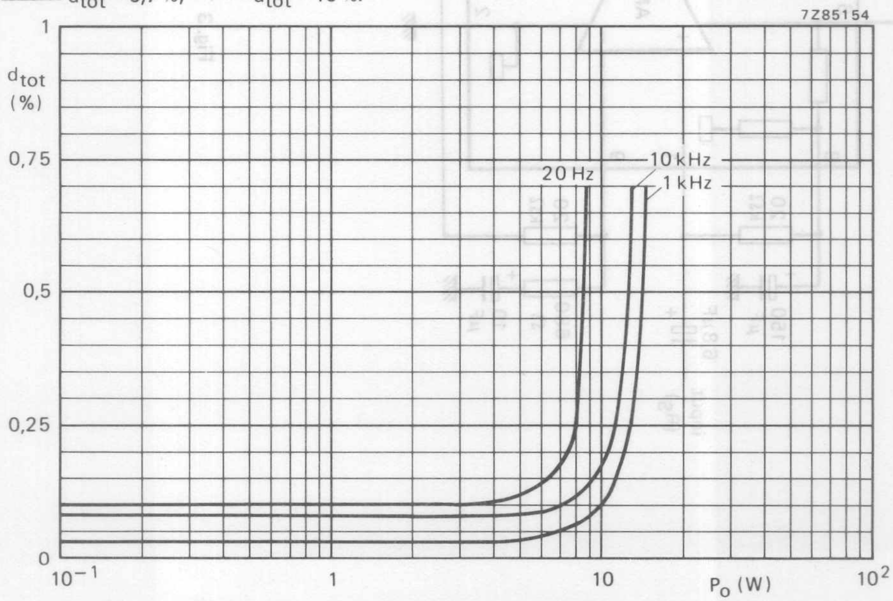



Fig. 5 Total harmonic distortion as a function of the output power.

# 24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515A is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage $V_P$ = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use — mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to $V_P$ = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

## QUICK REFERENCE DATA

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range (operating) | $V_P$ | | 6 to 18 | | V |
| Supply voltage (non-operating) | $V_P$ | max. | 28 | | V |
| Supply voltage (non-operating; load dump protection) | $V_P$ | max. | 45 | | V |
| Repetitive peak output current | $I_{ORM}$ | max. | 4 | | A |
| Total quiescent current | $I_{tot}$ | typ. | 75 | | mA |
| Stand-by current | $I_{sb}$ | typ. | 1 | | μA |
| Switch-on current | $I_{so}$ | < | 100 | | μA |
| Input impedance | $\|Z_i\|$ | > | 1 | | MΩ |
| **Bridge tied load application (BTL)** | $V_P$ | = | 14,4 | 13,2 | V |
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | | |
| **$d_{tot}$ = 0,5%** | $P_o$ | typ. | 18 | 15 | W |
| $d_{tot}$ = 10% | $P_o$ | typ. | 24 | 20 | W |
| Supply voltage ripple rejection; $R_S$ = 0 Ω; f = 100 Hz | RR | typ. | 50 | 50 | dB |
| D.C. output offset voltage between the outputs | $\|\Delta V_{5-9}\|$ | < | 50 | 50 | mV |
| **Stereo application** | | | | | |
| Output power at $d_{tot}$ = 10% (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 7 | 6 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 12 | 10 | W |
| Output power at **$d_{tot}$ = 0,5%** (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 | 4,5 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 9 | 7,5 | W |
| Channel separation | α | > | 40 | 40 | dB |
| Noise output voltage; $R_S$ = 10 kΩ; according to IEC curve-A | $V_n$ | typ. | 0,2 | 0,2 | mV |

**PACKAGE OUTLINE** 13-lead SIL; plastic power (SOT-141B).

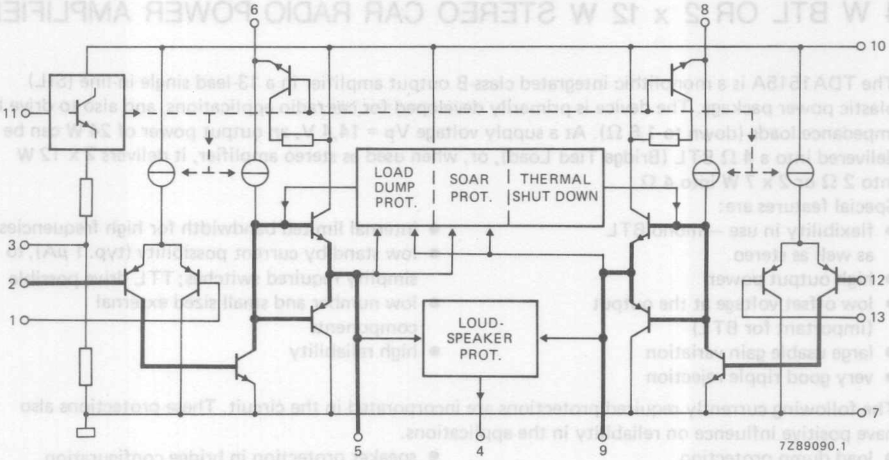



Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage; operating (pin 10) | $V_P$ | max. | 18 | V |
| Supply voltage; non-operating | $V_P$ | max. | 28 | V |
| Supply voltage; during 50 ms (load dump protection) | $V_P$ | max. | 45 | V |
| Peak output current | $I_{OM}$ | max. | 6 | A |
| Total power dissipation | see derating curve Fig. 2 | | | |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Crystal temperature | $T_c$ | max. | 150 | °C |
| A.C. and d.c. short-circuit safe voltage | | max. | 18 | V |
| Reverse polarity | | max. | 10 | V |

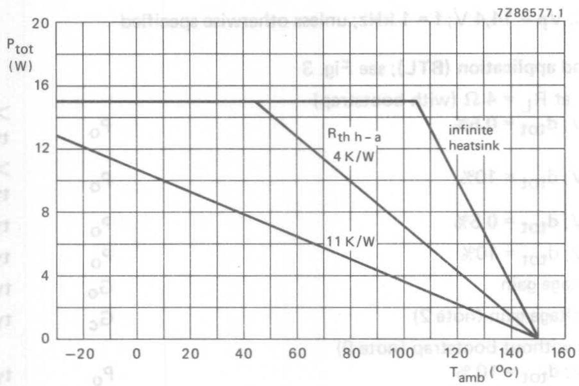



Fig. 2 Power derating curves.

## HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
$T_{amb}$ = 65 °C maximum

$$R_{th\,h\text{-}a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
$T_{amb}$ = 65 °C maximum

$$R_{th\,h\text{-}a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 10) | $V_P$ | | 6 to 18 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 4 | A |
| Total quiescent current | $I_{tot}$ | typ. | 75 | mA |
| Switching level 11 : OFF | $V_{11}$ | < | 1,8 | V |
| ON | $V_{11}$ | > | 3 | V |
| Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1{,}8$ V) | $\lvert Z_{OFF}\rvert$ | > | 100 | kΩ |
| Stand-by current at $V_{11}$ = 0 to 0,8 V | $I_{sb}$ | typ. | 1 | μA |
| | | < | 100 | μA |
| Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1) | $I_{so}$ | typ. | 10 | μA |
| | | < | 100 | μA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 14,4 V; f = 1 kHz; unless otherwise specified

**Bridge tied load application (BTL)**; see Fig. 3

| | | | | |
|---|---|---|---|---|
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | |
| $V_P$ = 14,4 V; $d_{tot}$ = 0,5% | $P_o$ | > | 15,5 | W |
| | | typ. | 18 | W |
| $V_P$ = 14,4 V; $d_{tot}$ = 10% | $P_o$ | > | 20 | W |
| | | typ. | 24 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 0,5% | $P_o$ | typ. | 15 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 10% | $P_o$ | typ. | 20 | W |
| Open loop voltage gain | $G_o$ | typ. | 75 | dB |
| Closed loop voltage gain (note 2) | $G_c$ | typ. | 40 (± 0,5) | dB |
| Output power without bootstrap (note 9) | | | | |
| $V_P$ = 14,4 V; $d_{tot}$ = 10 % | $P_o$ | typ. | 15 | W |
| $V_P$ = 14,4 V; $d_{tot}$ = 0,5 % | $P_o$ | typ. | 12 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 10 % | $P_o$ | typ. | 12 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 0,5 % | $P_o$ | typ. | 9 | W |
| Frequency response at −3 dB (note 3) | B | | 20 Hz to min. 20 | kHz |
| Input impedance (note 4) | $\lvert Z_i\rvert$ | > | 1 | MΩ |
| Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,2 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,35 | mV |
| | | < | 0,8 | mV |
| $R_S$ = 10 kΩ; according to IEC 179 curve A | $V_n$ | typ. | 0,25 | mV |
| Supply voltage ripple rejection (note 5) | | | | |
| f = 100 Hz | RR | > | 42 | dB |
| | | typ. | 50 | dB |
| D.C. output offset voltage between the outputs | $\lvert\Delta V_{5\text{-}9}\rvert$ | < | 50 | mV |
| | | typ. | 2 | mV |
| Loudspeaker protection (all conditions) maximum d.c. voltage (across the load) | $\lvert\Delta V_{5\text{-}9}\rvert$ | < | 1 | V |
| Power bandwidth; −1 dB; $d_{tot}$ = 0,5% | B | | 30 Hz to 40 | kHz |

**Stereo application**; see Fig. 4

| | | | |
|---|---|---|---|
| Output power at $d_{tot}$ = 10%; with bootstrap (note 6) | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | > | 6 W |
| | | typ. | 7 W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | > | 10 W |
| | | typ. | 12 W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6 W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 10 W |
| Output power at $d_{tot}$ = 0,5%; with bootstrap (note 6) | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | typ. | 9 W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,5 W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 7,5 W |
| Output power at $d_{tot}$ = 10%; without bootstrap | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω (notes 6, 8 and 9) | $P_o$ | typ. | 6 W |
| Frequency response at −3 dB (note 3) | B | 40 Hz to min. | 20 kHz |
| Supply voltage ripple rejection (note 5) | RR | typ. | 50 dB |
| Channel separation; $R_S$ = 10 kΩ; f = 1 kHz | α | > | 40 dB |
| | | typ. | 50 dB |
| Closed loop voltage gain (note 7) | $G_c$ | typ. | 40 dB |
| Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,15 mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,25 mV |
| $R_S$ = 10 kΩ; according to IEC 179 curve A | $V_n$ | typ. | 0,2 mV |

**Notes**

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

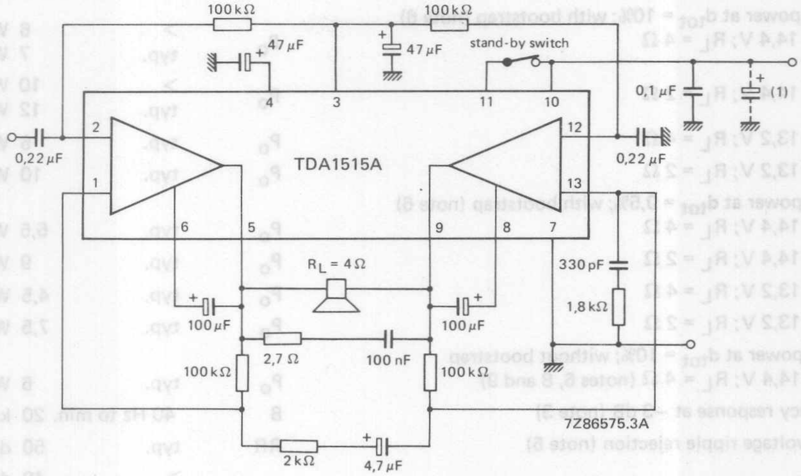



Fig. 3 Test/application circuit bridge tied load (BTL).

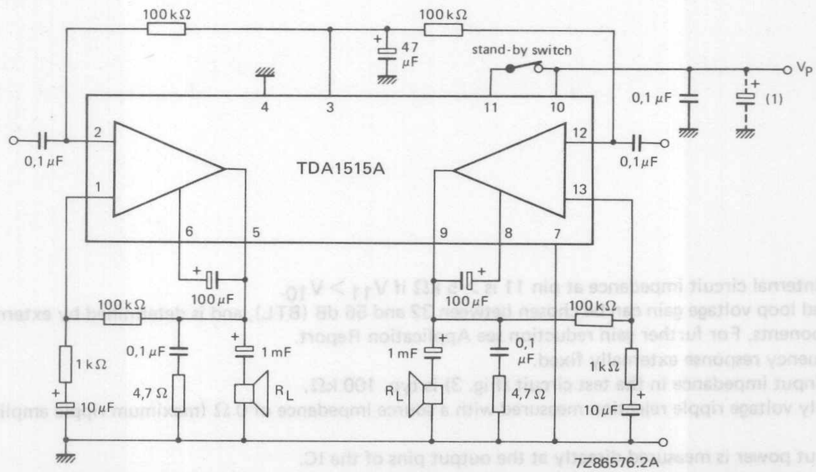



Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

# 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 40 | V |
| Total quiescent current at $V_P$ = 33 V | $I_{tot}$ | typ. | 54 | mA |
| Output power at $d_{tot}$ = 0,5% | | | | |
| sine-wave power | | | | |
| $V_P$ = 33 V; $R_L$ = 4 Ω | $P_o$ | typ. | 22 | W |
| $V_P$ = 33 V; $R_L$ = 4 Ω | $P_o$ | > | 16 | W |
| $V_P$ = 33 V; $R_L$ = 8 Ω | $P_o$ | typ. | 11 | W |
| Closed-loop voltage gain (externally determined) | $G_c$ | typ. | 30 | dB |
| Input resistance (externally determined by $R_{8-1}$) | $R_i$ | typ. | 20 | kΩ |
| Signal-to-noise ratio at $P_o$ = 50 mW | S/N | typ. | 75 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 60 | dB |

## PACKAGE OUTLINE

TDA1520 : 9-lead SIL; plastic power (SOT-131A).
TDA1520Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

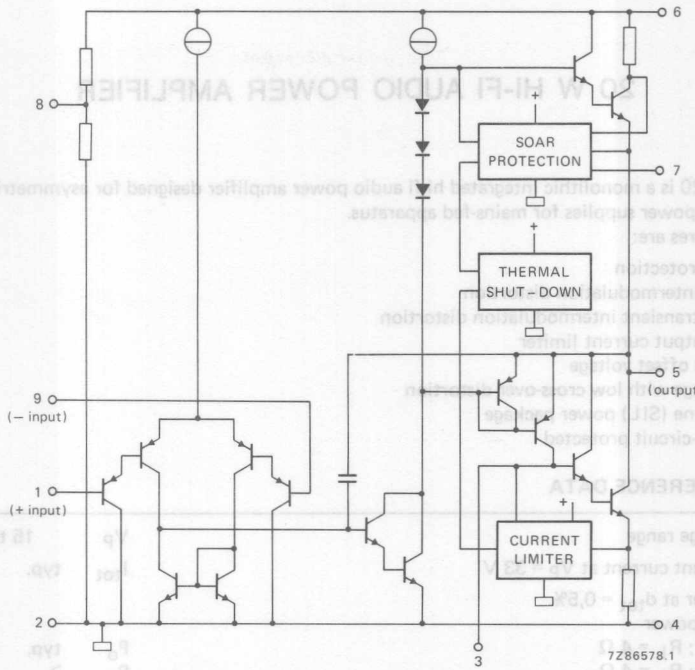



Fig. 1 Simplified internal circuit diagram.

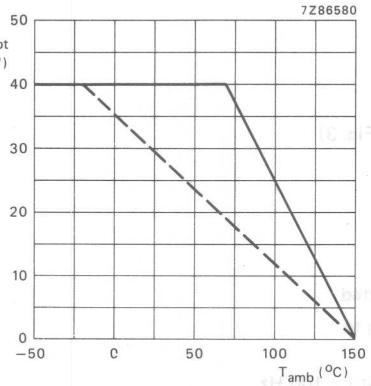
**PINNING**

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply ($V_P$)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 44 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 4 A |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 5 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$ and $f > 20$ Hz | $t_{sc}$ | max. | 1 hour |




—— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | ≤ | 2 K/W |

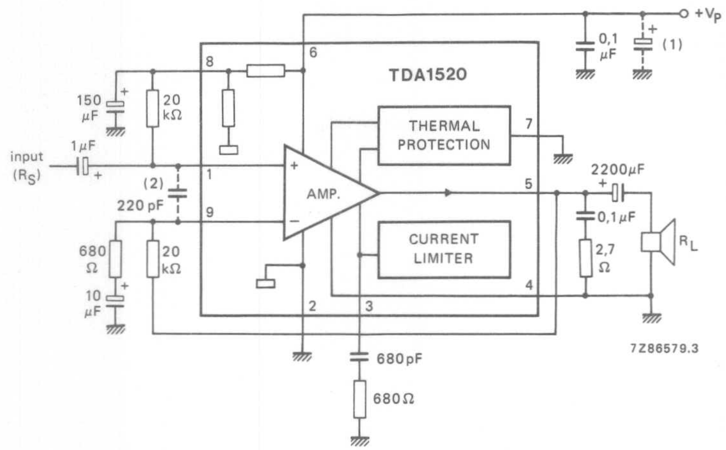
## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 40 | V |
| Total quiescent current at $V_P$ = 33 V | $I_{tot}$ | | 22 to 105 | mA |
| | | typ. | 54 | mA |

## A.C. CHARACTERISTICS

$V_P$ = 33 V; $R_L$ = 4 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Output power | | | | |
| sine-wave power at $d_{tot}$ = 0,5% | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 22 | W |
| $R_L$ = 4 Ω | $P_o$ | > | 16 | W |
| $R_L$ = 8 Ω | $P_o$ | typ. | 11 | W |
| Power bandwidth; −3 dB; $d_{tot}$ = 0,5% | B | | 20 Hz to 20 | kHz |
| Voltage gain | | | | |
| open-loop | $G_o$ | typ. | 74 | dB |
| closed-loop | $G_c$ | typ. | 30 | dB |
| Input resistance (pin 1) | $R_i$ | > | 1 | MΩ |
| Input resistance of test circuit (Fig. 3) | $R_i$ | typ. | 20 | kΩ |
| Input sensitivity | | | | |
| for $P_o$ = 50 mW | $V_i$ | typ. | 16 | mV |
| for $P_o$ = 16 W | $V_i$ | typ. | 260 | mV |
| Signal-to-noise ratio | | | | |
| at $P_o$ = 50 mW; $R_S$ = 2 kΩ; f = 20 Hz to 20 kHz; unweighted | S/N | typ. | 75 | dB |
| weighted; measured according to IEC 179 (A-curve) | S/N | typ. | 80 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 65 | dB |
| Total harmonic distortion at $P_o$ = 16 W | $d_{tot}$ | typ. | 0,01 | % |
| Output resistance (pin 5) | $R_o$ | typ. | 0,01 | Ω |
| | $R_o$ | < | 0,1 | Ω |




(1) Belongs to power supply.
(2) In application to improve radio interference suppression.

Fig. 3 Test circuit/basic application circuit.

# 20 W HI-FI AUDIO POWER AMPLIFIER

## GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

### Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 50 | V |
| Total quiescent current at $V_P$ = 33 V | $I_{tot}$ | typ. | 70 | mA |
| Output power at $d_{tot}$ = 0,5% sine-wave power | | | | |
| $V_P$ = 33 V; $R_L$ = 4 Ω | $P_o$ | typ. | 22 | W |
| $V_P$ = 33 V; $R_L$ = 4 Ω | $P_o$ | > | 20 | W |
| $V_P$ = 42 V; $R_L$ = 8 Ω | $P_o$ | typ. | 20 | W |
| Closed-loop voltage gain (externally determined) | $G_c$ | typ. | 30 | dB |
| Input resistance (externally determined by $R_{8\text{-}1}$) | $R_i$ | typ. | 20 | kΩ |
| Signal-to-noise ratio at $P_o$ = 50 mW | S/N | typ. | 76 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 60 | dB |

## PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).
TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

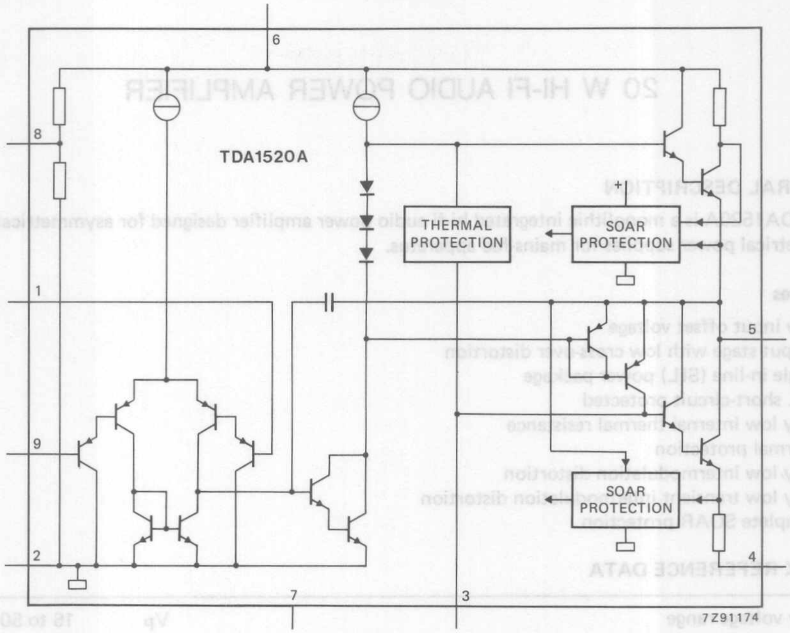



Fig. 1 Simplified internal circuit diagram.

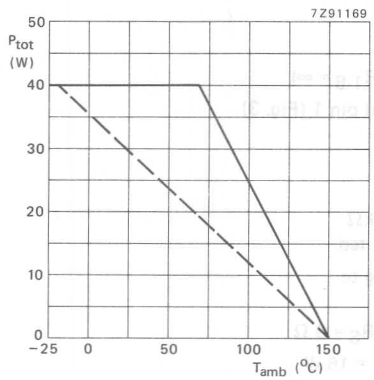
## PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply ($V_P$)
7. Not connected
8. Ripple rejection
9. Inverting input (feedback)

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 50 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 4 A |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 5 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| Duration of a.c. short-circuit of load ($R_L = 0\ \Omega$) during full-load sine-wave drive at: $V_S = \pm 20$ V (symmetrical) and $R_{supply} = 0\ \Omega$; or $V_S = 35$ V (asymmetrical) and $R_{supply} \geq 4\ \Omega$ | $t_{sc}$ | max. | 100 hours |




——— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

## THERMAL RESISTANCE

| | | |
|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ ≤ | 2 K/W |

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 50 | V |
| Total quiescent current at $V_P$ = 33 V | $I_{tot}$ | typ. | 70 | mA |
| | | $\leq$ | 105 | mA |
| Minimum guaranteed output current (peak value) | $I_{ORM}$ | $\geq$ | 3,2 | A |

## A.C. CHARACTERISTICS

$V_P$ = 33 V; $R_L$ = 4 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Output power | | | | |
| sine-wave power at $d_{tot}$ = 0,5% | | | | |
| $R_L$ = 4 Ω (Fig. 4) | $P_o$ | typ. | 22 | W |
| $R_L$ = 4 Ω (Fig. 4) | $P_o$ | > | 20 | W |
| $R_L$ = 8 Ω; $V_P$ = 42 V (Fig. 4) | $P_o$ | typ. | 20 | W |
| Power bandwidth at $d_{tot}$ = 0,5% from $P_o$ = 50 mW to 10 W | B | 20 Hz to | 20 | kHz |
| Voltage gain | | | | |
| open-loop | $G_o$ | typ. | 74 | dB |
| closed-loop | $G_c$ | typ. | 30 | dB |
| Internal resistance of pin 1 (at $R_{1\text{-}8} = \infty$) | $R_i$ | > | 1 | MΩ |
| Input resistance of test circuit at pin 1 (Fig. 3) | $R_i$ | typ. | 20 | kΩ |
| Input sensitivity for $P_o$ = 16 W | $V_i$ | typ. | 260 | mV |
| Signal-to-noise ratio | | | | |
| at $P_o$ = 50 mW; $R_{source}$ = 2 kΩ; f = 20 Hz to 20 kHz; unweighted | S/N | typ. | 76 | dB |
| weighted; measured according to IEC 179 (A-curve) | S/N | typ. | 80 | dB |
| Ripple rejection at f = 100 Hz; $R_S$ = 0 Ω | RR | typ. | 60 | dB |
| Total harmonic distortion at $P_o$ = 16 W | $d_{tot}$ | typ. | 0,01 | % |
| Output resistance (pin 5) | $R_o$ | typ. | 0,01 | Ω |
| Input offset voltage | $V_{5\text{-}8}$ | typ. | 1 | mV |
| | | < | 100 | mV |
| Transient intermodulation distortion at $P_o$ = 10 W | $d_{TIM}$ | typ. | 0,01 | % |
| Intermodulation distortion at $P_o$ = 10 W | $d_{IM}$ | typ. | 0,01 | % |
| Slew rate | SR | typ. | 9 | V/μs |

## APPLICATION INFORMATION

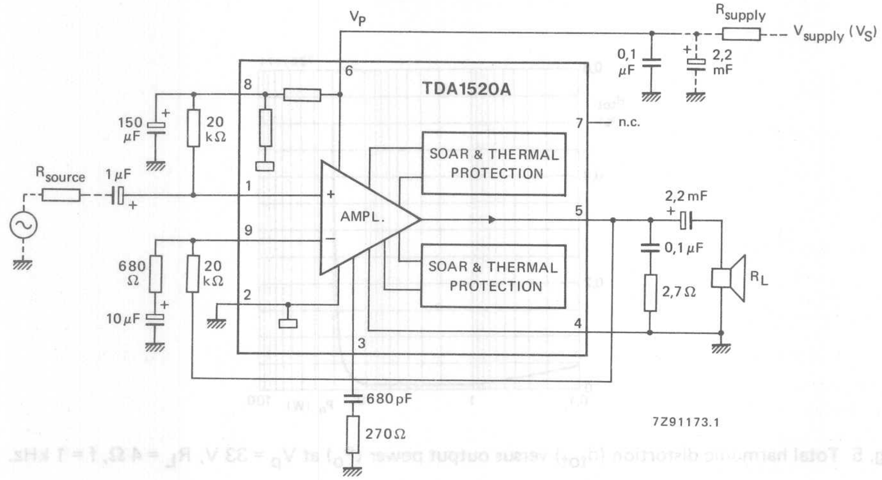



Fig. 3 Test and application circuit.

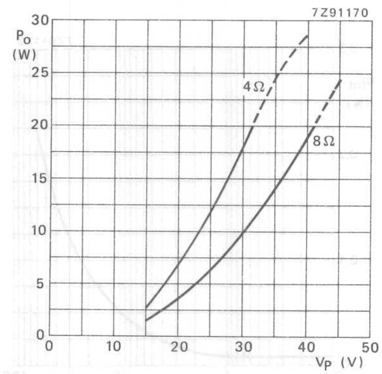



Fig. 4 Output power ($P_o$) versus supply voltage ($V_p$) at f = 1 kHz, $d_{tot}$ = 0,5%, $G_v$ = 30 dB.

APPLICATION INFORMATION (continued)

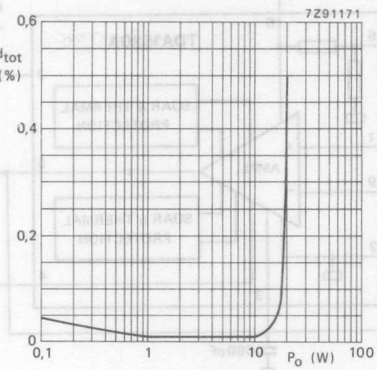



Fig. 5 Total harmonic distortion ($d_{tot}$) versus output power ($P_o$) at $V_p$ = 33 V, $R_L$ = 4 Ω, f = 1 kHz.

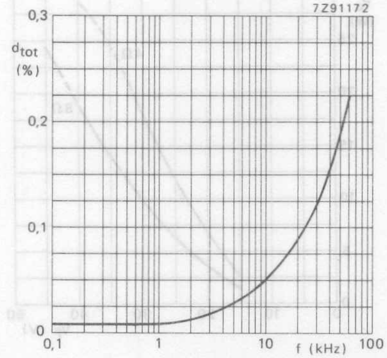



Fig. 6 Total harmonic distortion ($d_{tot}$) versus operating frequency (f) at $V_p$ = 33 V, $R_L$ = 4 Ω, $P_o$ = 10 W (constant).

# STEREO CASSETTE HEAD PREAMPLIFIER AND EQUALIZER

## GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

### Features

- Two independent amplifiers with open loop gain of typ. 90 dB
- Internal d.c. feedback via a 140 kΩ resistor from output to feedback point
- A.C. characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at d.c. ground that eliminates the input coupling capacitor
- Minimal external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- D.C. input current < 2 μA
- Wide supply voltage range

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage range (pin 8) | $V_P$ | 7,5 to 23 | V |
| Supply current (pin 8) | $I_P$ | typ. 5 | mA |
| Operating ambient temperature range | $T_{amb}$ | −30 to +85 | °C |
| Total harmonic distortion | THD | typ. 0,05 | % |
| Channel separation at $R_S$ = 10 kΩ; $L_S$ = 0 | α | min. 45 | dB |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

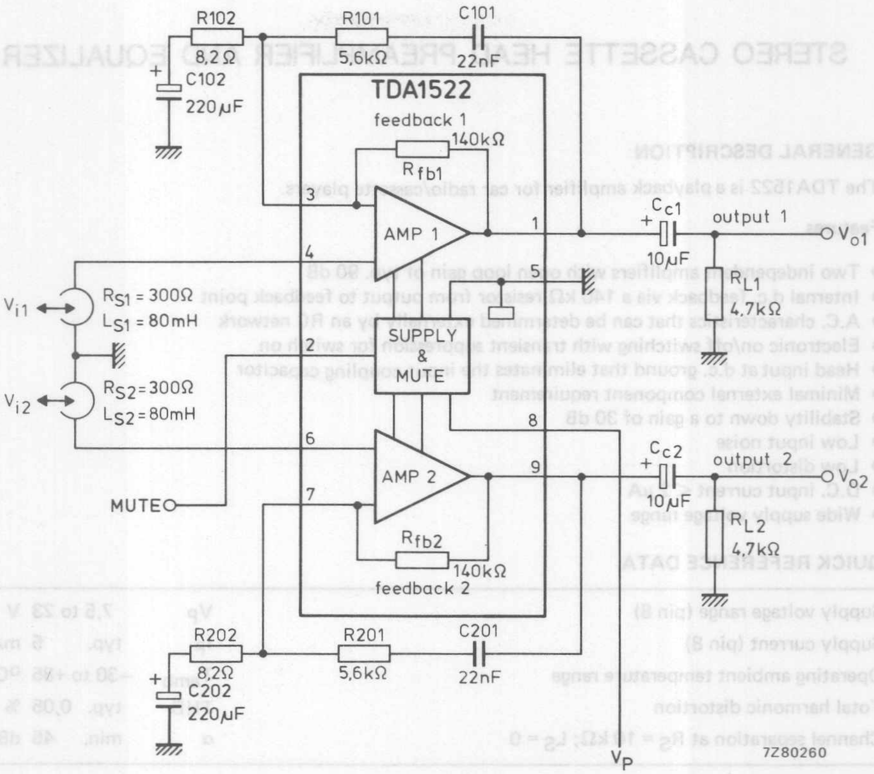



Fig. 1 Block diagram with external components; also used as test circuit.

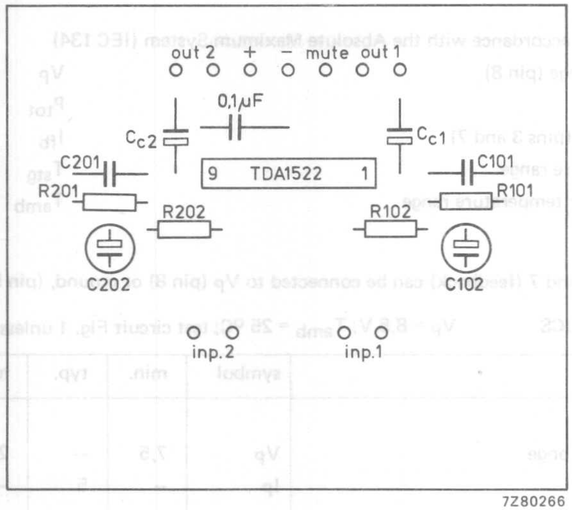



Fig. 2 Printed-circuit board component side, showing component layout for circuit of Figure 1.

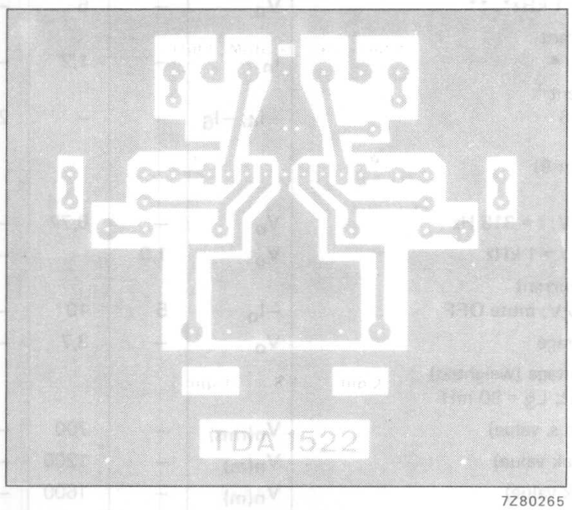



Fig. 3 Printed-circuit board, showing track side. Dimensions 75 mm x 65 mm.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage range (pin 8) | $V_P$ | | 7,5 to 23 V |
| Power dissipation | $P_{tot}$ | max. | 800 mW |
| Feedback current (pins 3 and 7) | $I_{fb}$ | max. | 10 mA |
| Storage temperature range | $T_{stg}$ | | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +85 °C |

**Note**

All pins except 3 and 7 (feedback) can be connected to $V_P$ (pin 8) or ground, (pin 5).

## CHARACTERISTICS

$V_P$ = 8,5 V; $T_{amb}$ = 25 °C; test circuit Fig. 1 unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 8) | | | | | |
| Supply voltage range | $V_P$ | 7,5 | – | 23 | V |
| Supply current | $I_P$ | – | 5 | – | mA |
| **Inputs** (pin 4 or 6) | | | | | |
| Noise input voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz* | $V_{n(rms)}$ | – | 1,6 | – | μV |
| Noise input voltage at $R_S$ = 0; f = 1 kHz*, ** | $V_n$ | – | 5 | – | nV/√Hz |
| Noise input current at f = 1 kHz*, ▲ | $I_n$ | – | 1,2 | – | pA/√Hz |
| D.C. input current at pins 4 and 6 | $-I_4; -I_6$ | – | – | 2 | μA |
| **Outputs** (pin 1 or 9) | | | | | |
| Output voltage at $V_i$ = 0,3 mV; f = 315 Hz | $V_o$ | – | 0,72 | – | V |
| at THD= 1%; f = 1 kHz | $V_o$ | 1,0 | – | – | V |
| Output source current at $V_{2\text{-}5} \geqslant$ 7,5 V; mute OFF | $-I_o$ | 5 | 10 | – | mA |
| D.C. output voltage | $V_o$ | – | 3,7 | – | V |
| Noise output voltage (weighted) at $R_S$ = 300 Ω; $L_S$ = 80 mH | | | | | |
| as DIN A (r.m.s. value) | $V_{n(rms)}$ | – | 700 | – | μV |
| as CCITT (peak value) | $V_{n(m)}$ | – | 1200 | – | μV |
| as CCIR (peak value) | $V_{n(m)}$ | – | 1600 | – | μV |
| Noise output voltage (unweighted) at $R_S$ = 300 Ω; $L_S$ = 80 mH | | | | | |
| as DIN 45405 (peak value) | $V_{n(m)}$ | – | 1800 | – | μV |

* Measured in Fig. 4. ** See also Fig. 6. ▲ See also Fig. 7.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Mute on/off characteristics** (pin 2)* | | | | | |
| Mute ON voltage at mute switch closed | $V_m$ | 0 | – | 1 | V |
| Mute ON current at mute switch closed or $V_{2\text{-}5}$ = 0 V | $I_m$ | – | 2,7 | – | μA |
| Mute OFF voltage at mute switch open | $V_m$ | 7,5 | – | $V_P$ | V |
| **Impedance** | | | | | |
| Input impedance** at f = 1 kHz | $\lvert Z_i \rvert$ | 200 | – | – | kΩ |
| Output impedance** at f = 1 kHz | $\lvert Z_o \rvert$ | – | – | 1 | kΩ |
| **General** | | | | | |
| Internal feedback resistor** | $R_{fb}$ | 100 | 140 | 180 | kΩ |
| Open-loop voltage gain** at f = 315 Hz | $G_v$ | – | 90 | – | dB |
| Channel separation at $R_S$ = 10 kΩ; $L_S$ = 0; (note 1) | $\alpha$ | 45 | – | – | dB |
| Power supply ripple rejection at $V_{P(rms)}$ = 0,1 V; f = 100 Hz (note 2) | RR | 90 | 95 | – | dB |
| Total harmonic distortion at f = 1 kHz; $V_o$ = 0,72 V (note 3) | THD | – | 0,05 | – | % |

**Notes**

1. Frequency range 300 Hz to 20 kHz.
2. Referred to the input.
3. Measured selective.

* See also Fig. 5.
** Applies to each amplifier.

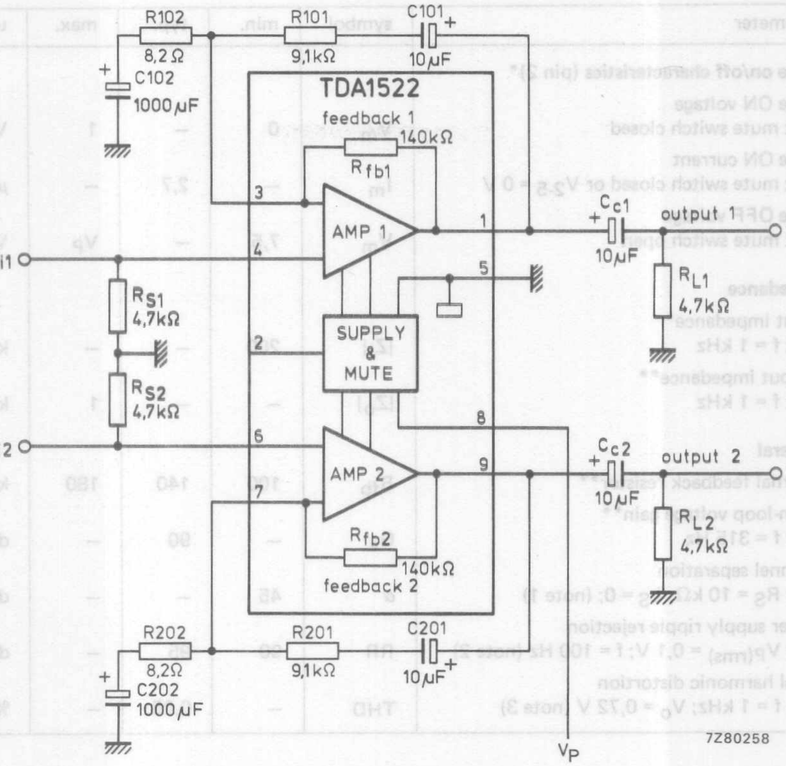



Fig. 4 Test circuit for noise measurement.

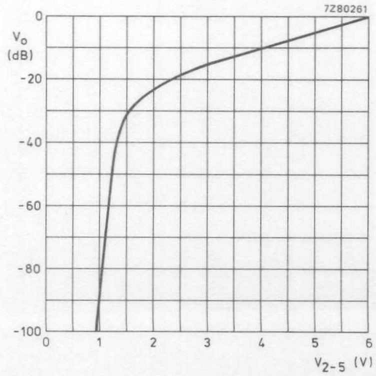



Fig. 5 Muting depth as a function of control voltage at pin 2.

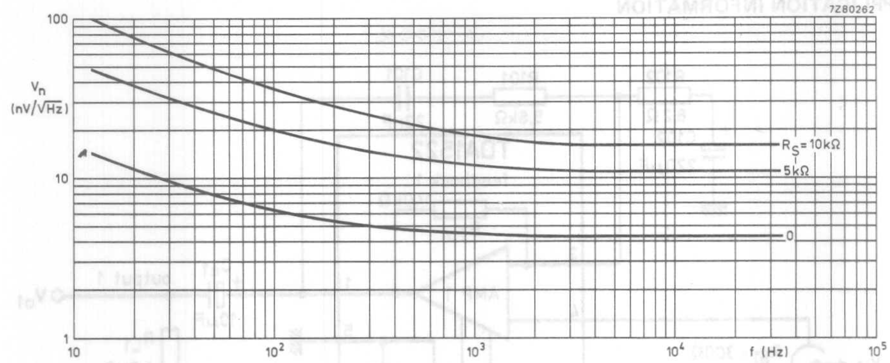



Fig. 6 Noise input voltage as a function of frequency.

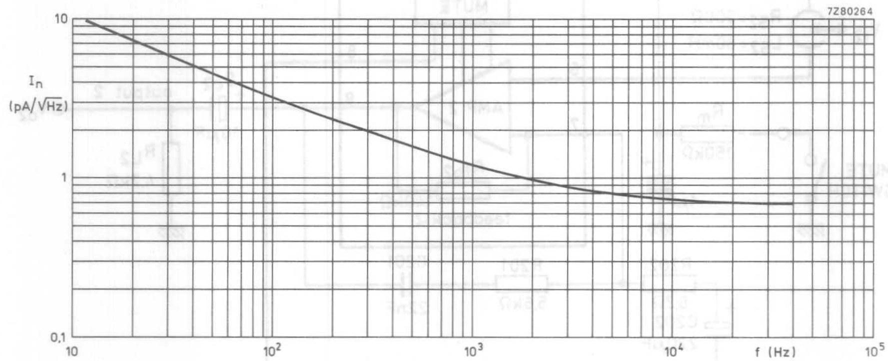



Fig. 7 Noise input current as a function of frequency.

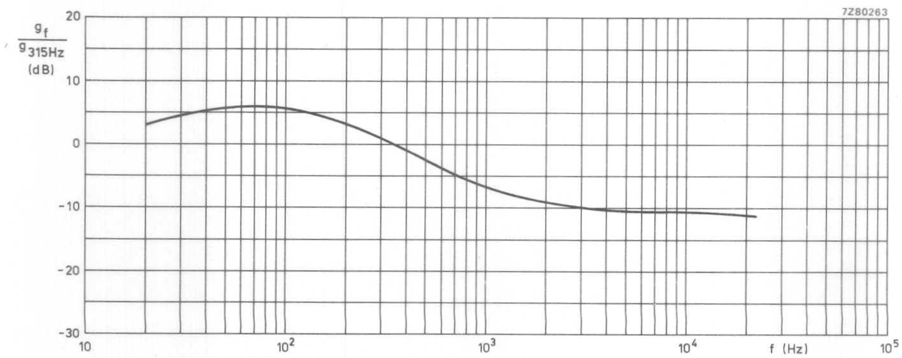



Fig. 8 Frequency response curve for the circuit in Figure 1.

## APPLICATION INFORMATION

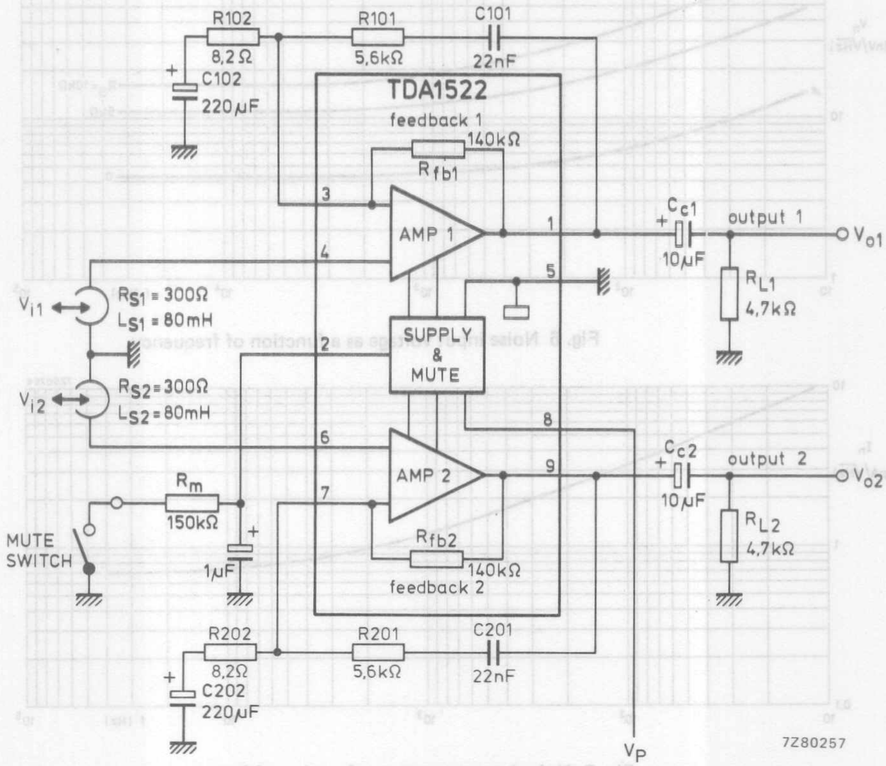



Fig. 9 Simple mute application.

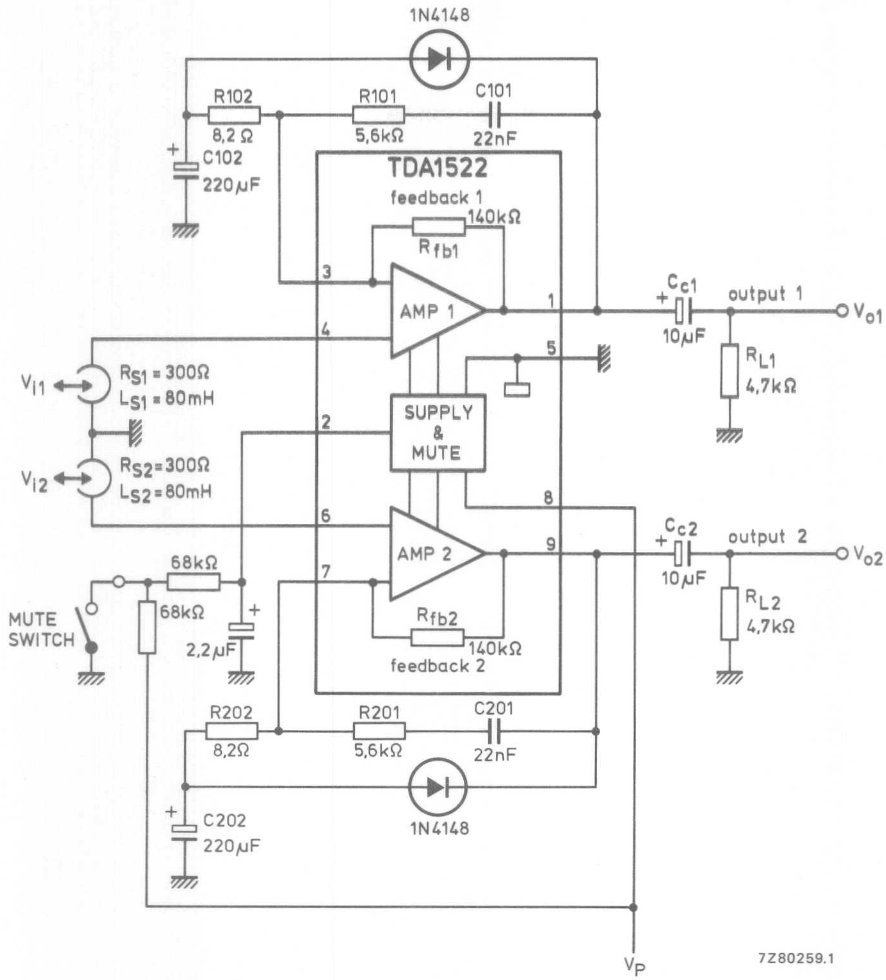



Fig. 10 Application for plop-free muting.

# STEREO-TONE/VOLUME CONTROL CIRCUIT

## GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

### Features

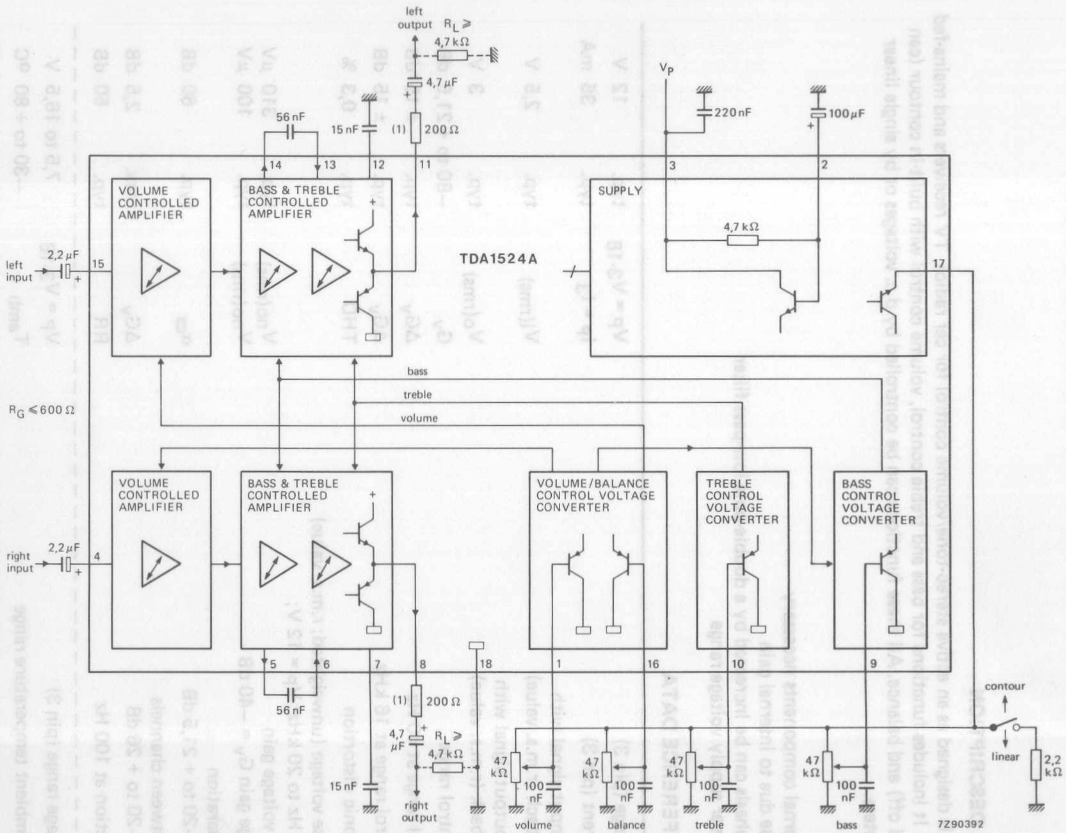
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 3) | $V_P = V_{3\text{-}18}$ | typ. | 12 | V |
| Supply current (pin 3) | $I_P = I_3$ | typ. | 35 | mA |
| Maximum input signal with d.c. feedback (r.m.s. value) | $V_{i(rms)}$ | typ. | 2,5 | V |
| Maximum output signal with d.c. feedback (r.m.s. value) | $V_{o(rms)}$ | typ. | 3 | V |
| Volume control range | $G_v$ | | −80 to + 21,5 | dB |
| Bass control range at 40 Hz | $\Delta G_v$ | typ. | ± 15 | dB |
| Treble control range at 16 kHz | $\Delta G_v$ | typ. | ± 15 | dB |
| Total harmonic distortion | THD | typ. | 0,3 | % |
| Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; $V_P$ = 12 V; | | | | |
| for max. voltage gain | $V_{no(rms)}$ | typ. | 310 | μV |
| for voltage gain $G_v$ = −40 dB | $V_{no(rms)}$ | typ. | 100 | μV |
| Channel separation at $G_v$ = −20 to + 21,5 dB | $\alpha_{cs}$ | typ. | 60 | dB |
| Tracking between channels at $G_v$ = −20 to + 26 dB | $\Delta G_v$ | max. | 2,5 | dB |
| Ripple rejection at 100 Hz | RR | typ. | 50 | dB |
| Supply voltage range (pin 3) | $V_P = V_{3\text{-}18}$ | | 7,5 to 16,5 | V |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).




(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

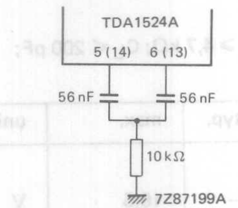



Fig. 2 Double-pole low-pass filter for improved bass-boost.

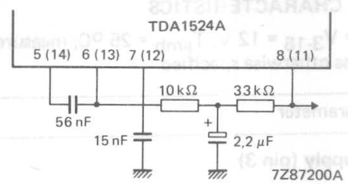



Fig. 3 D.C. feedback with filter network for improved signal handling.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 3) | $V_P = V_{3\text{-}18}$ | max. | 20 | V |
| Total power dissipation | $P_{tot}$ | max. | 1200 | mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 | °C |

## D.C. CHARACTERISTICS

$V_P = V_{3\text{-}18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 3) | | | | | |
| Supply voltage | $V_P = V_{3\text{-}18}$ | 7,5 | – | 16,5 | V |
| Supply current | | | | | |
| at $V_P$ = 8,5 V | $I_P = I_3$ | 19 | 27 | 35 | mA |
| at $V_P$ = 12 V | $I_P = I_3$ | 25 | 35 | 45 | mA |
| at $V_P$ = 15 V | $I_P = I_3$ | 30 | 43 | 56 | mA |
| D.C. input levels (pins 4 and 15) | | | | | |
| at $V_P$ = 8,5 V | $V_{4,15\text{-}18}$ | 3,8 | 4,25 | 4,7 | V |
| at $V_P$ = 12 V | $V_{4,15\text{-}18}$ | 5,3 | 5,9 | 6,6 | V |
| at $V_P$ = 15 V | $V_{4,15\text{-}18}$ | 6,5 | 7,3 | 8,2 | V |
| D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3) | | | | | |
| at $V_P$ = 8,5 V | $V_{8,11\text{-}18}$ | 3,3 | 4,25 | 5,2 | V |
| at $V_P$ = 12 V | $V_{8,11\text{-}18}$ | 4,6 | 6,0 | 7,4 | V |
| at $V_P$ = 15 V | $V_{8,11\text{-}18}$ | 5,7 | 7,5 | 9,3 | V |
| **Pin 17** | | | | | |
| Internal potentiometer supply voltage at $V_P$ = 8,5 V | $V_{17\text{-}18}$ | 3,5 | 3,75 | 4,0 | V |
| Contour on/off switch (control by $I_{17}$) | | | | | |
| contour (switch open ) | $-I_{17}$ | – | – | 0,5 | mA |
| linear (switch closed) | $-I_{17}$ | 1,5 | – | 10 | mA |
| Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off) | | | | | |
| Voltage range forced to pin 17 | $V_{17\text{-}18}$ | 4,5 | – | $V_P/2 - V_{BE}$ | V |
| D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively) | | | | | |
| at $V_{17\text{-}18}$ = 5 V | $V_{1,9,10,16}$ | 1,0 | – | 4,25 | V |
| using internal supply | $V_{1,9,10,16}$ | 0,25 | – | 3,8 | V |
| Input current of control inputs (pins 1, 9, 10 and 16) | $-I_{1,9,10,16}$ | – | – | 5 | μA |

## A.C. CHARACTERISTICS

$V_P = V_{3\text{-}18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Control range** | | | | | |
| Max. gain of volume (Fig. 5) | $G_{v\ max}$ | 20,5 | 21,5 | 23 | dB |
| Volume control range; $G_{v\ max}/G_{v\ min}$ | $\Delta G_v$ | 90 | 100 | – | dB |
| Balance control range; $G_v$ = 0 dB (Fig. 6) | $\Delta G_v$ | – | −40 | – | dB |
| Bass control range at 40 Hz (Fig. 7) | $\Delta G_v$ | ± 12 | ± 15 | – | dB |
| Treble control range at 16 kHz (Fig. 8) | $\Delta G_v$ | ± 12 | ± 15 | – | dB |
| Contour characteristics | | see Figs 9 and 10 | | | |
| **Signal inputs, outputs** | | | | | |
| Input resistance; pins 4 and 15 (note 1) at gain of volume control: $G_v$ = 20 dB | $R_{i4,15}$ | 10 | – | – | kΩ |
| $G_v$ = −40 dB | $R_{i4,15}$ | – | 160 | – | kΩ |
| Output resistance (pins 8 and 11) | $R_{o8,11}$ | – | – | 300 | Ω |
| **Signal processing** | | | | | |
| Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_v$ = 0 dB | RR | 35 | 50 | – | dB |
| Channel separation (250 Hz to 10 kHz) at $G_v$ = −20 to + 21,5 dB | $\alpha_{cs}$ | 46 | 60 | – | dB |
| Spread of volume control with constant control voltage $V_{1\text{-}18} = 0{,}5\ V_{17\text{-}18}$ | $\Delta G_v$ | – | – | ± 3 | dB |
| Gain tolerance between left and right channel $V_{16\text{-}18} = V_{1\text{-}18} = 0{,}5\ V_{17\text{-}18}$ | $\Delta G_{v,L\text{-}R}$ | – | – | 1,5 | dB |
| Tracking between channels for $G_v$ = 21,5 to −26 dB f = 250 Hz to 6,3 kHz; balance adjusted at $G_v$ = 10 dB | $\Delta G_v$ | – | – | 2,5 | dB |

A.C. CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Signal handling with d.c. feedback** (Fig. 3) | | | | | |
| Input signal handling | | | | | |
| at $V_P$ = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value) | $V_{i(rms)}$ | 1,4 | – | – | V |
| at $V_P$ = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value) | $V_{i(rms)}$ | 1,8 | 2,4 | – | V |
| at $V_P$ = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{i(rms)}$ | 1,4 | – | – | V |
| at $V_P$ = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{i(rms)}$ | 2,0 | 3,2 | – | V |
| at $V_P$ = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{i(rms)}$ | 1,4 | – | – | V |
| at $V_P$ = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{i(rms)}$ | 2,0 | 3,2 | – | V |
| Output signal handling (note 2 and note 3) | | | | | |
| at $V_P$ = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value) | $V_{o(rms)}$ | 1,8 | 2,0 | – | V |
| at $V_P$ = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value) | $V_{o(rms)}$ | – | 2,2 | – | V |
| at $V_P$ = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{o(rms)}$ | 2,5 | 3,0 | – | V |
| at $V_P$ = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value) | $V_{o(rms)}$ | – | 3,5 | – | V |
| **Noise performance** ($V_P$ = 8,5 V) | | | | | |
| Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(rms)}$ | – | 260 | – | μV |
| for $G_v$ = –3 dB (note 4) | $V_{no(rms)}$ | – | 70 | 140 | μV |
| Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(m)}$ | – | 890 | – | μV |
| for maximum emphasis of bass and treble (contour off; $G_v$ = –40 dB) | $V_{no(m)}$ | – | 360 | – | μV |
| **Noise performance** ($V_P$ = 12 V) | | | | | |
| Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(rms)}$ | – | 310 | – | μV |
| for $G_v$ = –16 dB (note 4) | $V_{no(rms)}$ | – | 100 | 200 | μV |
| Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(m)}$ | – | 940 | – | μV |
| for maximum emphasis of bass and treble (contour off; $G_v$ = –40 dB) | $V_{no(m)}$ | – | 400 | – | μV |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Noise performance** ($V_P$ = 15 V) | | | | | |
| Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(rms)}$ | – | 350 | – | μV |
| for $G_v$ = 16 dB (note 4) | $V_{no(rms)}$ | – | 110 | 220 | μV |
| Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) | | | | | |
| for maximum voltage gain (note 4) | $V_{no(m)}$ | – | 980 | – | μV |
| for maximum emphasis of bass and treble (contour off; $G_v$ = –40 dB) | $V_{no(m)}$ | – | 420 | – | μV |

**Notes to characteristics**

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ \text{k}\Omega}{1 + G_v};\ G_{v\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

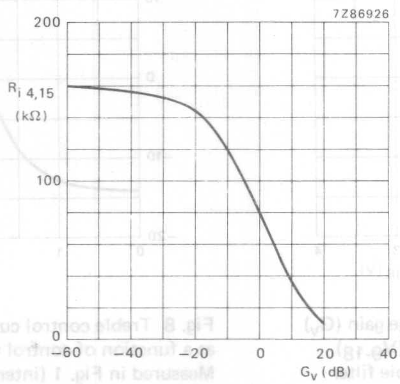



Fig. 4 Input resistance ($R_i$) as a function of gain of volume control ($G_v$). Measured in Fig. 1.

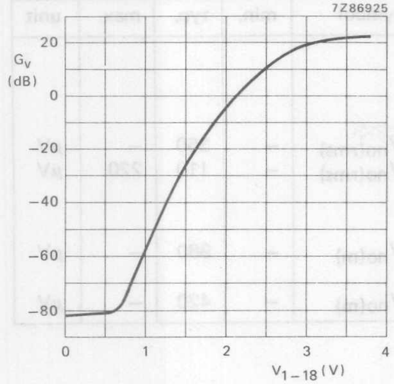



Fig. 5 Volume control curve; voltage gain ($G_V$) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); $V_P$ = 8,5 V; f = 1 kHz.

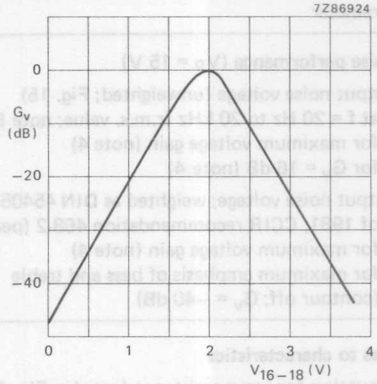



Fig. 6 Balance control curve; voltage gain ($G_V$) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); $V_P$ = 8,5 V.

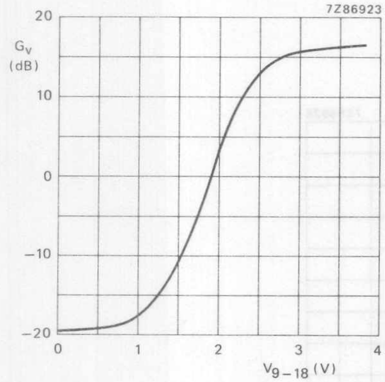



Fig. 7 Bass control curve; voltage gain ($G_V$) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); $V_P$ = 8,5 V; f = 40 Hz.

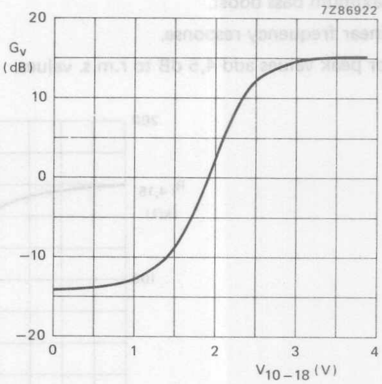



Fig. 8 Treble control curve; voltage gain ($G_V$) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); $V_P$ = 8,5 V; f = 16 kHz.

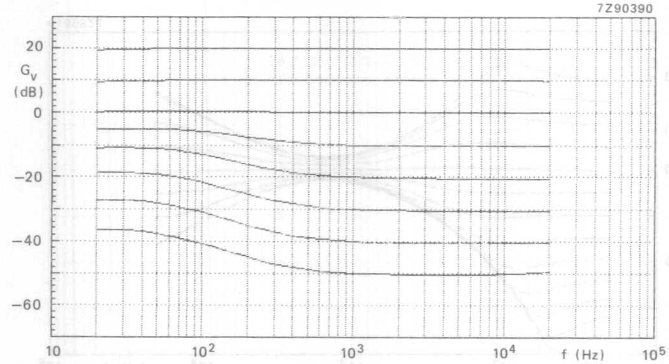



Fig. 9 Contour frequency response curves; voltage gain ($G_V$) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; $V_P$ = 8,5 V.

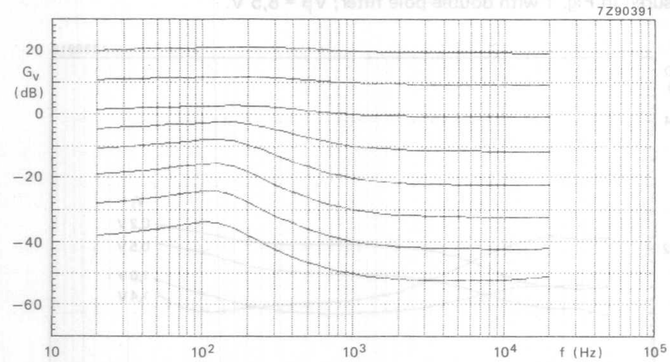



Fig. 10 Contour frequency response curves; voltage gain ($G_V$) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; $V_P$ = 8,5 V.

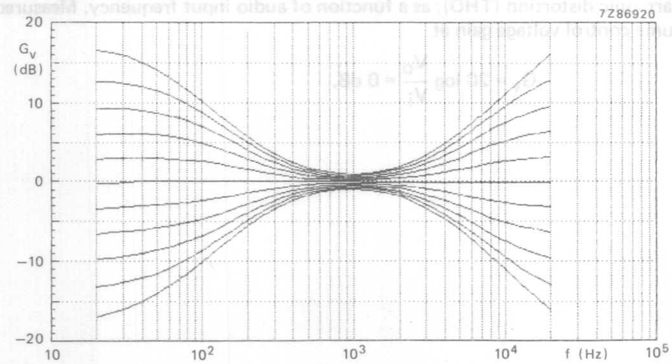



Fig. 11 Tone control frequency response curves; voltage gain ($G_V$) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; $V_P$ = 8,5 V.

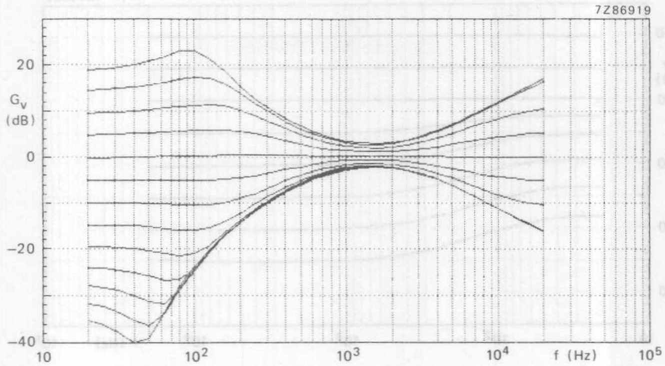



Fig. 12 Tone control frequency response curves; voltage gain ($G_v$) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; $V_P$ = 8,5 V.

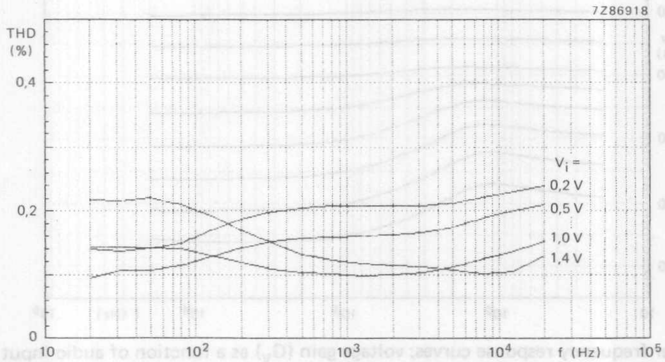



Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; $V_P$ = 8,5 V; volume control voltage gain at

$$G_v = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

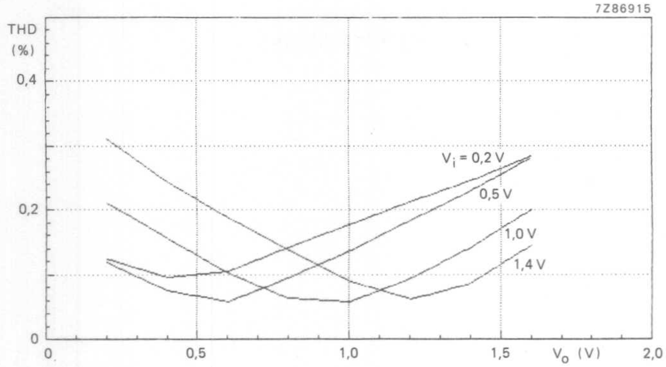
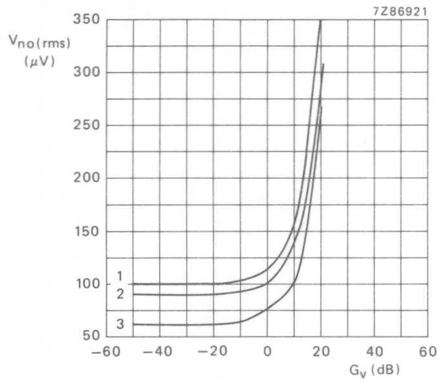



Fig. 14 Total harmonic distortion (THD); as a function of output voltage ($V_o$). Measured in Fig. 1; $V_P$ = 8,5 V; $f_i$ = 1 kHz.




(1) $V_P$ = 15 V.
(2) $V_P$ = 12 V.
(3) $V_P$ = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain ($G_v$). Measured in Fig. 1; f = 20 Hz to 20 kHz.

# PLL MOTOR SPEED CONTROL CIRCUIT FOR HI-FI APPLICATIONS

The TDA1533 is a monolithic integrated circuit intended for PLL motor speed control in several hi-fi applications; e.g. record players, cassette recorders, reel-to-reel, and operates in accordance with the phase-locked-loop (PLL) system.
The circuit incorporates the following functions:

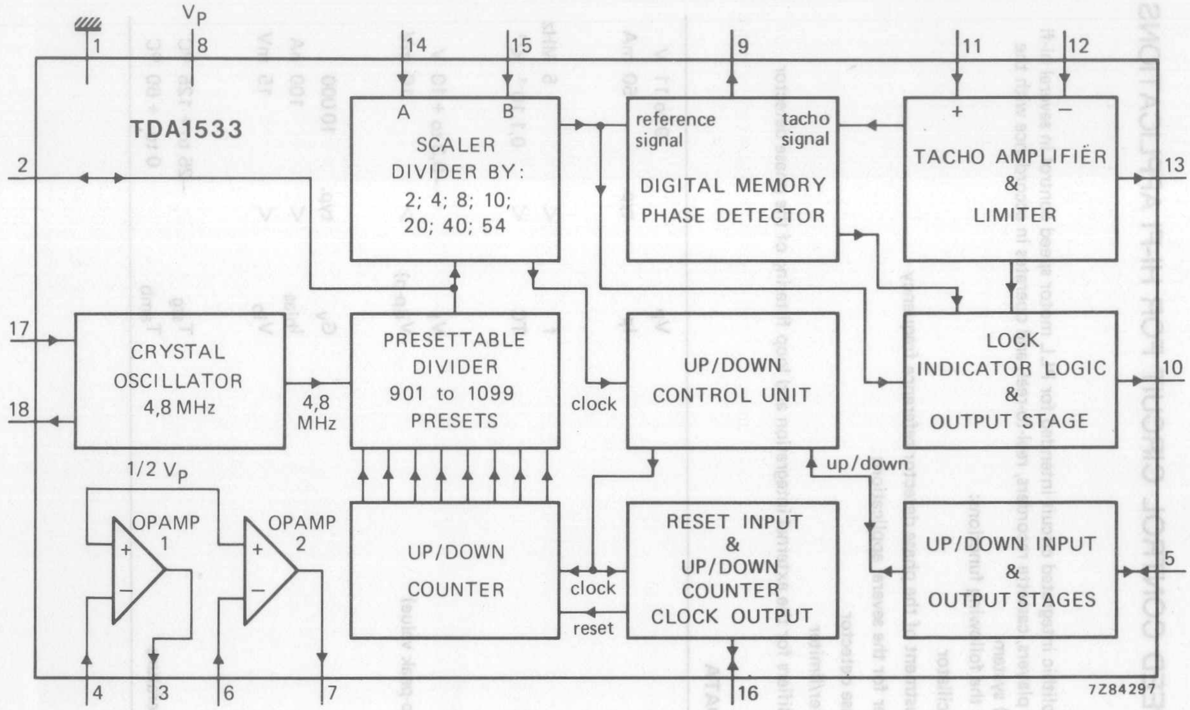
- A quartz reference oscillator
- A synthesizer for adjustment of the phase detector reference frequency
- A programmable scaler for the several applications
- A digital memory phase detector
- A tacho-signal amplifier/limiter
- Two operational amplifiers for the external integration and loop filtering of the phase detector output.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 9 to 11 | V |
| Supply current | $I_P$ | typ. | 50 | mA |
| **Crystal oscillator** | | | | |
| Frequency | f | < | 5 | MHz |
| Temperature coefficient | TC | < | $0{,}1.10^{-6}$ | $K^{-1}$ |
| **Tacho input** | | | | |
| Input voltage | $V_I$ | | −0,3 to + 10 | V |
| Input sensitivity (peak-to-peak value) | $V_{i(p-p)}$ | > | 10 | mV |
| **Operational amplifiers** | | | | |
| Voltage gain | $G_v$ | typ. | 10 000 | |
| Input bias current | $I_{bias}$ | < | 100 | nA |
| Input offset voltage | $V_{io}$ | < | 15 | mV |
| **Temperatures** | | | | |
| Storage temperature | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 60 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).




PINNING

1. Ground
2. Test input/output
3. Output of opamp 1
4. Input of opamp 1
5. Up/down input/output
6. Input of opamp 2
7. Output of opamp 2
8. Positive supply (+ 10 V)
9. Phase detector output
10. Lock indicator output
11. + input tacho limiter
12. − input tacho limiter
13. Output tacho limiter
14. A-input scaler control
15. B-input scaler control
16. Reset input/output
17. Crystal oscillator input
18. Crystal oscillator output

Fig. 1 Block diagram.

## GENERAL DESCRIPTION (see also Fig. 1)

The crystal frequency (e.g. 4,8 MHz) is divided by the presettable 901 to 1099 divider. The scaler is used to obtain the reference signal for the digital memory phase detector. The tacho signal is derived from the tacho amplifier/limiter.
The output of the phase detector becomes HIGH on the positive-going edge of the reference signal, and it is floating on the first-coming positive edge of the tacho signal, if the angle between the edges is not more than 360°. The output becomes LOW if the first positive-going edge is the edge of the tacho signal, and it is floating on the first-coming positive edge of the reference signal. This means that the holding range is 720°.
The lock indication output is HIGH, except for the period between the two positive and the two negative-going edges of the tacho and reference signals.
The dividing number of the presettable divider depends on the state of its presets, thus on the position of the up/down counter.
A pull-up to the IC supply voltage of the reset input results into a reset of the up/down counter and dividing by 1000.
The up/down counter can be changed in position by means of the up/down input and the up/down control unit, and therefore the divisors of the presettable divider in a range from 901 to 1099.
The clock of the up/down counter is available at the reset input as a 0,1 $V_P$ to 0,8 $V_P$ pulse.
The timing diagram of the up/down counter is given in Fig. 2.
The up/down input and the scaler control inputs are 3-state inputs. The scaler truth table is given below.
A HIGH level at the up/down input gives an increase, a LOW level a decrease, of the phase detector reference signal frequency.
The information at the up/down input will be internally forced on the state present, over a period of 250 ms. Together with the up/down clock at the reset pin, this offers the possibility of displaying the number of clock pulses used.

## SCALER TRUTH TABLE

| control inputs A | control inputs B | division ratio |
|---|---|---|
| H | H | note 1 |
| H | L | note 2 |
| F | F | 4 |
| F | H | 8 |
| F | L | 2 |
| H | F | 54 |
| L | H | 10 |
| L | L | 20 |
| L | F | 40 |

H = HIGH state (the more positive voltage)
L = LOW state ( the less positive voltage)
F = floating (pin open)

### Notes

1. Test 1; general preset.
2. Test 2; fast clock via test pin (pin 2).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P = V_{8\text{-}1}$ | max. | 12 V |
| Total power dissipation | $P_{tot}$ | max. | 1 W |
| Storage temperature | $T_{stg}$ | | −25 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +80 °C |

## CHARACTERISTICS

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | typ. | 10 V |
| | | | 9 to 11 V |
| Supply current | $I_P$ | typ. | 50 mA |
| Operating ambient temperature | $T_{amb}$ | | 0 to 60 °C |

The following characteristics are measured at $V_P$ = 10 V; $T_{amb}$ = 25 °C; unless otherwise specified

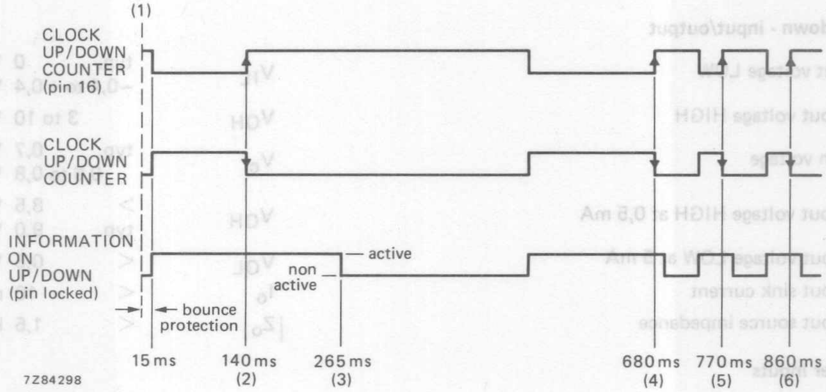
| | | | |
|---|---|---|---|
| **Crystal oscillator** | | | |
| Frequency | f | typ. | 4,8 MHz |
| | | < | 5,0 MHz |
| Input voltage HIGH | $V_{IH}$ | | 2,6 to 10 V |
| Input voltage LOW | $V_{IL}$ | | −2,0 to +2,0 V |
| Input resistance | $R_i$ | > | 50 kΩ |
| Input capacitance | $C_i$ | < | 5 pF |
| Open voltage 1 | $V_{o1}$ | typ. | 2 V |
| Open voltage 2 | $V_{o2}$ | typ. | 1,3 V |
| Temperature coefficient | TC | < | $0{,}1.10^{-6}$ $K^{-1}$ |
| **Lock indicator output** (open collector) | | | |
| Output voltage HIGH | $V_{OH}$ | < | 12 V |
| Output voltage LOW at 10 mA | $V_{OL}$ | typ. | 0,25 V |
| | | < | 0,5 V |
| Output sink current | $I_o$ | typ. | 10 mA |
| | | < | 20 mA |
| **Phase detector output** | | | |
| Output voltage HIGH at 20 µA | $V_{OH}$ | > | 9,5 V |
| | | typ. | 9,7 V |
| Output voltage LOW at 20 µA | $V_{OL}$ | typ. | 0,3 V |
| | | < | 0,5 V |
| Output current | | | |
| source | $I_o$ | > | 30 µA |
| | | typ. | 44 µA |
| sink | $I_o$ | > | 30 µA |
| | | typ. | 44 µA |

| | | | |
|---|---|---|---|
| **Tacho input** | | | |
| Input voltage | $V_I$ | | −0,3 to + 10 V |
| Input biasing current | $I_{bias}$ | typ. | 0,5 μA |
| | | < | 5,0 μA |
| Input sensitivity (peak-to-peak value) | $V_{i(p-p)}$ | > | 10 mV |
| Offset voltage over temperature range | $V_{io}$ | typ. | 0,1 mV |
| | | < | 2,0 mV |
| Offset current over temperature range | $I_{io}$ | typ. | 50 nA |
| | | < | 250 nA |
| **Tacho output** (open collector) | | | |
| Output voltage HIGH | $V_{OH}$ | < | 12 V |
| Output voltage LOW at 5 mA | $V_{OL}$ | < | 0,5 V |
| Output sink current | $I_o$ | < | 10 mA |
| **Up/down - input/output** | | | |
| Input voltage LOW | $V_{IL}$ | typ. | 0 V |
| | | | −0,4 to + 0,4 V |
| Output voltage HIGH | $V_{OH}$ | | 3 to 10 V |
| Open voltage | $V_o$ | typ. | 0,7 V |
| | | | 0,6 to 0,8 V |
| Output voltage HIGH at 0,5 mA | $V_{OH}$ | > | 8,5 V |
| | | typ. | 9,0 V |
| Output voltage LOW at 5 mA | $V_{OL}$ | < | 0,5 V |
| Output sink current | $I_o$ | < | 10 mA |
| Output source impedance | $\|Z_o\|$ | < | 1,5 kΩ |
| **Scaler inputs** | | | |
| Input voltage LOW | $V_{IL}$ | typ. | 0 V |
| | | | −0,4 to + 0,4 V |
| Input voltage HIGH | $V_{IH}$ | | 4 to 10 V |
| Open voltage | $V_o$ | typ. | 0,7 V |
| | | | 0,6 to 0,8 V |
| **Reset input/output** | | | |
| Input voltage HIGH | $V_{IH}$ | > | 9,5 V |
| | | typ. | 10,0 V |
| Output voltage LOW | $V_{OL}$ | typ. | 0,3 V |
| | | < | 0,5 V |
| Output voltage HIGH | $V_{OH}$ | typ. | 8 V |

**CHARACTERISTICS** (continued)

**Operational amplifiers**

| | | | | |
|---|---|---|---|---|
| Voltage gain | $G_v$ | typ. | 10 000 | |
| Input bias current | $I_{bias}$ | typ. | 30 | nA |
| | | < | 100 | nA |
| Output sink current at $V_o$ = 1 V | $I_o$ | typ. | 0,1 | mA |
| Output source current at $V_o$ = 9 V | $I_o$ | > | 15 | mA |
| | | typ. | 20 | mA |
| Input offset voltage | $V_{io}$ | < | 15 | mV |
| Input offset voltage drift | $\Delta V_{io}/\Delta T$ | < | 0,25 | mV/K |
| Bandwidth (3 dB) | B | | 60 | Hz |




(1) Start operation of up/down pin.
(2) 1st clock pulse.
(3) From this point on, restart of cycle by second excitation is possible.
(4) 2nd clock pulse.
(5) 3rd clock pulse.
(6) 4th clock pulse.

Fig. 2 Timing diagram of up/down counter.

# 14-BIT DAC WITH 85 dB S/N RATIO

## GENERAL DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltages | | | | |
| pin 4 | $V_{P1}$ | typ. | 5 | V |
| pin 7 | $V_{N1}$ | typ. | −5 | V |
| pin 11 | $V_{N2}$ | typ. | −17 | V |
| Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22) | S/N | typ. | 85 | dB |
| Non-linearity at $T_{amb}$ = −20 to + 70 °C | | typ. | ½ | LSB |
| Current settling time | $t_{cs}$ | typ. | 0,5 | μs |
| Maximum input bit rate at data input (pin 1) | $BR_{max}$ | min. | 12 | Mbit/s |
| Maximum clock frequency at clock input (pin 28) | $f_{cl\,max}$ | min. | 12 | MHz |
| Full scale temperature coefficient at analogue output (pin 22) | $TC_{FS}$ | typ. | $\pm 30 \cdot 10^{-6}$ | $K^{-1}$ |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |
| Total power dissipation | $P_{tot}$ | typ. | 350 | mW |

## PACKAGE OUTLINES

TDA1540D: 28-lead DIL; ceramic (cerdip) (SOT-135A).
TDA1540P: 28-lead DIL; plastic (SOT-117BE).

## FUNCTIONAL DESCRIPTION

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($I_1$), I ($I_2$) and 2I ($I_3$) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0 V ± 10 mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

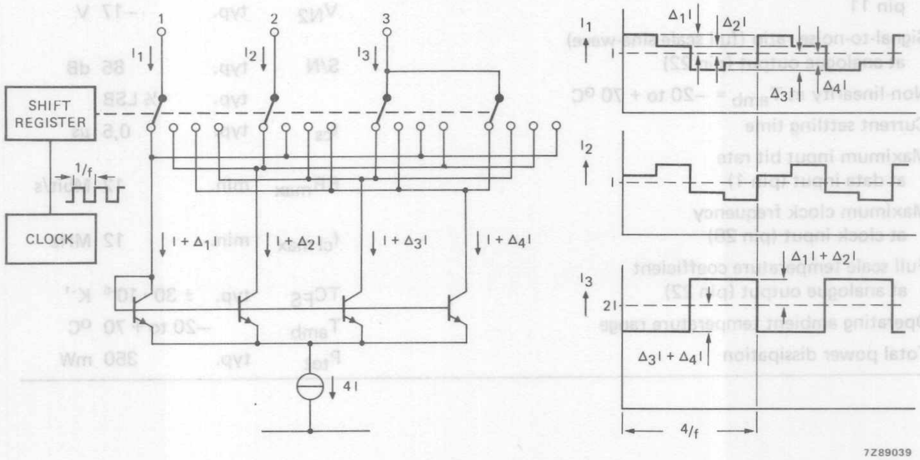



Fig. 1a Circuit diagram of one divider stage.

Fig. 1b Waveforms showing output currents $I_1$, $I_2$ and $I_3$ of Fig. 1a.

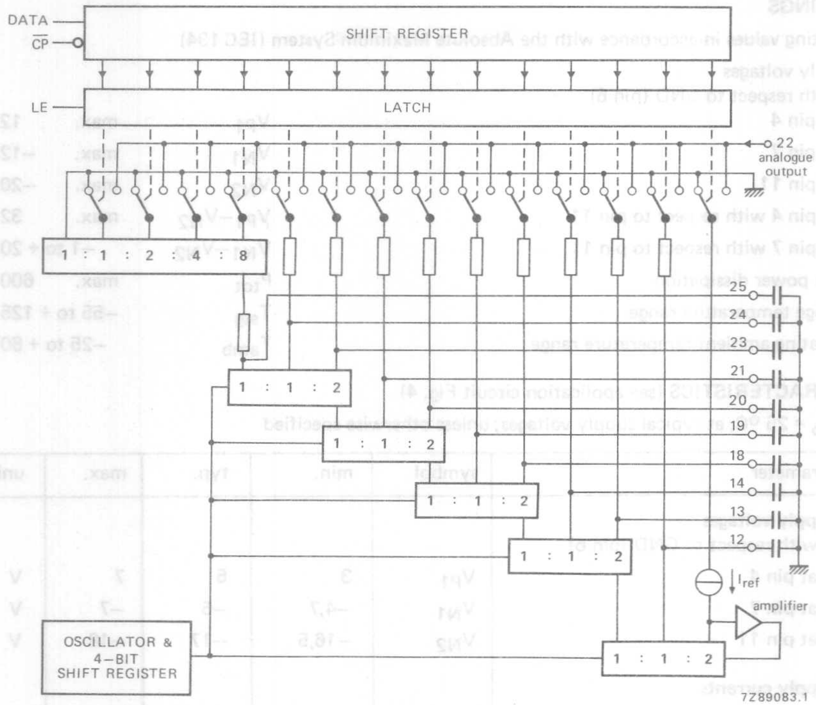



Fig. 2 Functional diagram showing cascading of current division stages.

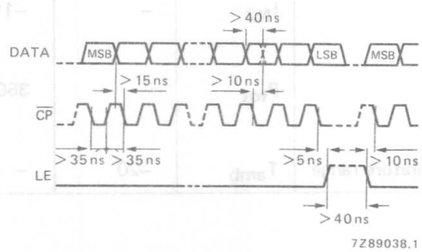



Fig. 3 Format of input signals.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltages | | | | |
| with respect to GND (pin 6) | | | | |
| at pin 4 | $V_{P1}$ | max. | 12 | V |
| at pin 7 | $V_{N1}$ | max. | −12 | V |
| at pin 11 | $V_{N2}$ | max. | −20 | V |
| at pin 4 with respect to pin 11 | $V_{P1}-V_{N2}$ | max. | 32 | V |
| at pin 7 with respect to pin 11 | $V_{N1}-V_{N2}$ | | −1 to + 20 | V |
| Total power dissipation | $P_{tot}$ | max. | 600 | mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 80 | °C |

**CHARACTERISTICS** (see application circuit Fig. 4)

$T_{amb}$ = 25 °C; at typical supply voltages; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply voltages** | | | | | |
| with respect to GND (pin 6) | | | | | |
| at pin 4 | $V_{P1}$ | 3 | 5 | 7 | V |
| at pin 7 | $V_{N1}$ | −4,7 | −5 | −7 | V |
| at pin 11 | $V_{N2}$ | −16,5 | −17 | −18 | V |
| **Supply currents** | | | | | |
| at pin 4* | $I_{P1}$ | – | 12 | 14 | mA |
| at pin 7 | $I_{N1}$ | – | −20 | −24 | mA |
| at pin 11 | $I_{N2}$ | – | −11 | −13 | mA |
| **Power dissipation** | | | | | |
| Total power dissipation | $P_{tot}$ | – | 350 | 410 | mW |
| **Temperature** | | | | | |
| Operating ambient temperature range | $T_{amb}$ | −20 | – | + 70 | °C |

* When the output current is ½$I_{FS}$ (½ full scale output current).

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Data input DATA** (pin 1) | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | 7,0 | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V |
| Input current HIGH at $V_{IH}$ | $I_{IH}$ | – | – | 50 | μA |
| Input current LOW at $V_{IL}$ | $-I_{IL}$ | – | – | 0,2 | mA |
| Maximum input bit rate | $BR_{max}$ | 12 | – | – | Mbits/s |
| **Latch enable input LE** (pin 2) | | | | | |
| **Clock input $\overline{CP}$** (pin 28) | | | | | |
| Input voltage HIGH | $V_{IH}$ | 2,0 | – | 7,0 | V |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V |
| Input current HIGH at $V_{IH}$ | $I_{IH}$ | – | – | 50 | μA |
| Input current LOW at $V_{IL}$ | $-I_{IL}$ | – | – | 0,2 | mA |
| Maximum clock frequency | $f_{CPmax}$ | 12 | – | – | MHz |
| **Oscillator** (pins 8 and 9) | | | | | |
| Oscillator frequency at $C_{8-9}$ = 820 pF | $f_{osc}$ | 100 | 160 | 200 | kHz |
| **Analogue output $I_{out}$** (pin 22) | | | | | |
| Output voltage compliance | $V_{OC}$ | –10 | – | +10 | mV |
| Full scale current | $I_{FS}$ | 3,8 | 4,0 | 4,2 | mA |
| Zero scale current | $\pm I_{ZS}$ | – | – | 100 | nA |
| Full scale temperature coefficient $T_{amb}$ = –20 to + 70 °C | $TC_{FS}$ | – | $\pm 30 \times 10^{-6}$ | – | $K^{-1}$ |
| Settling time to ± ½LSB all bits on or off | $t_{cs}$ | – | 0,5 | – | μs |
| Signal-to-noise ratio* | S/N | 80 | 85 | – | dB |

* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

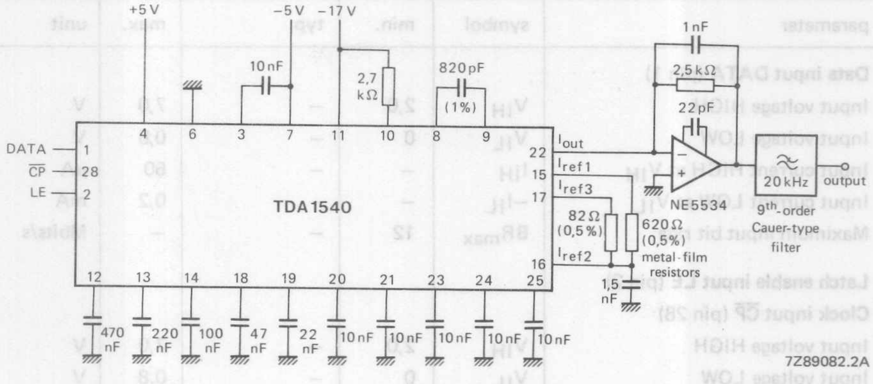



Fig. 4 Application circuit.

## PINNING

| | | |
|---|---|---|
| 1 | DATA | data input |
| 2 | LE | latch enable input |
| 3 | $V_{ref1}$ | voltage reference |
| 4 | $V_{P1}$ | positive supply |
| 5 | i.c.* | frequency compensation on-chip operational amplifier |
| 6 | GND | ground |
| 7 | $V_{N1}$ | negative supply |
| 8 | OSC1 | oscillator capacitor |
| 9 | OSC2 | oscillator capacitor |
| 10 | $V_{ref2}$ | voltage reference |
| 11 | $V_{N2}$ | negative supply |
| 12 | C1 | decoupling binary weighted current sources |
| 13 | C2 | decoupling binary weighted current sources |
| 14 | C3 | decoupling binary weighted current sources |
| 15 | $I_{ref1}$ | current reference sources |
| 16 | $I_{ref2}$ | current reference sources |
| 17 | $I_{ref3}$ | current reference sources |
| 18 | C4 | decoupling binary weighted current sources |
| 19 | C5 | decoupling binary weighted current sources |
| 20 | C6 | decoupling binary weighted current sources |
| 21 | C7 | decoupling binary weighted current sources |
| 22 | $I_{out}$ | analogue output |
| 23 | C8 | decoupling binary weighted current sources |
| 24 | C9 | decoupling binary weighted current sources |
| 25 | C10 | decoupling binary weighted current sources |
| 26 | i.c.* | voltage reference |
| 27 | i.c.* | voltage reference |
| 28 | $\overline{CP}$ | clock pulse input |

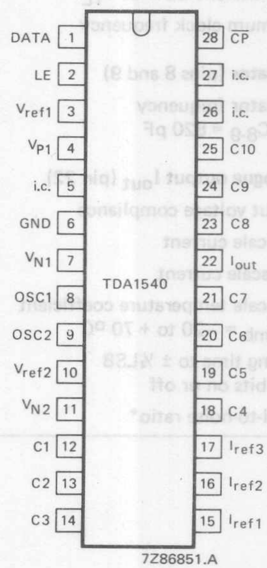



Fig. 5 Pinning diagram.

* i.c.: internally connected.

# MOTOR SPEED REGULATOR

The TDA1559 is a 3 pins speed regulator circuit for d.c. motors. It is especially intended for low-voltage motors in battery operated cassette recorder systems and record players. The IC features a high multiplication coefficient (k = 21,5) and a low drop-out voltage (0,5 V). It also contains a current limiter and thermal shut-down.

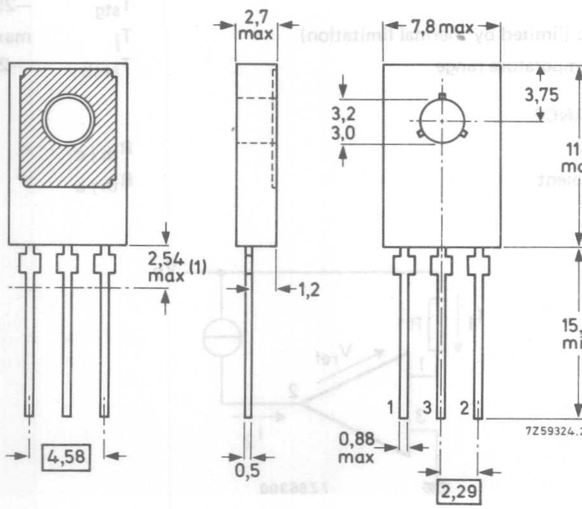
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | 16 | V |
| Internal reference voltage | $V_{ref}$ | typ. | 1,26 | V |
| Drop-out voltage | $V_{2\text{-}3}$ | typ. | 0,5 | V |
| Limited output current | $I_{2\,lim}$ | typ. | 0,7 | A |
| Multiplication coefficient | k | typ. | 21,5 | |
| Thermal limitation | $T_{j\,lim}$ | typ. | 145 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to +70 | °C |

## PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.




(1) Within this region the cross-section of the leads is uncontrolled.

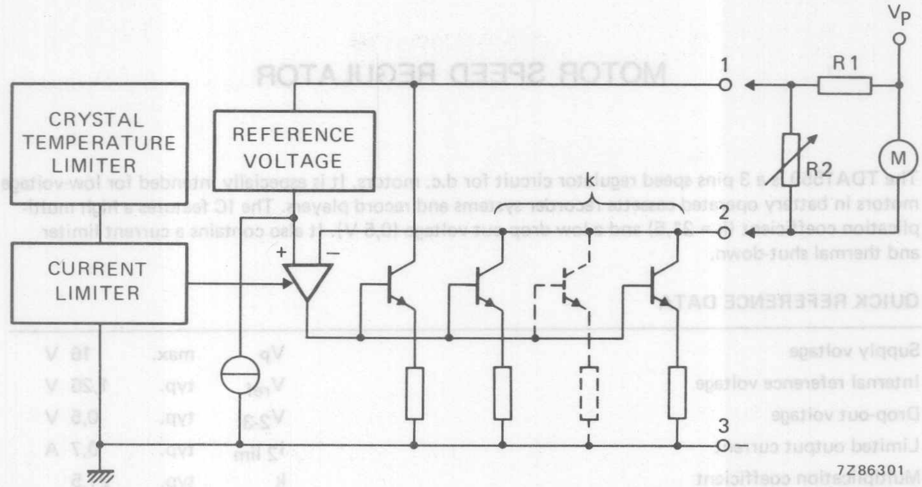



Fig. 2 Functional diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{1\text{-}3}$ | max. | 16 | V |
| Output current | $I_2$ | max. | 1,2 | A |
| Storage temperature | $T_{stg}$ | | −25 to +125 | °C |
| Junction temperature (limited by thermal limitation) | $T_j$ | max. | 130 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 70 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to case | $R_{th\ j\text{-}c}$ | = | 10 | K/W |
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 100 | K/W |

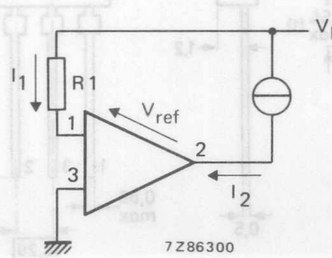



Fig. 3 Test circuit.

## CHARACTERISTICS

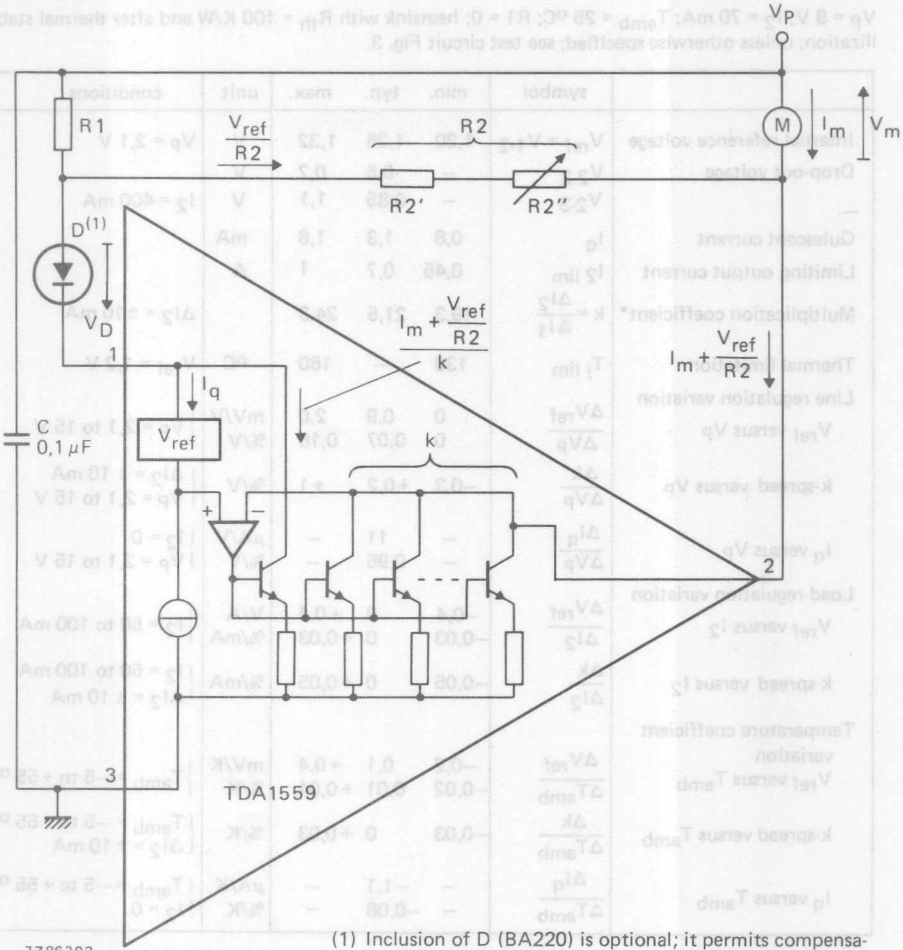
$V_P$ = 9 V; $I_2$ = 70 mA; $T_{amb}$ = 25 °C; R1 = 0; heatsink with $R_{th}$ = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 3.

| | symbol | min. | typ. | max. | unit | conditions |
|---|---|---|---|---|---|---|
| Internal reference voltage | $V_{ref} = V_{1\text{-}2}$ | 1,20 | 1,26 | 1,32 | V | $V_P$ = 2,1 V |
| Drop-out voltage | $V_{2\text{-}3}$ | – | 0,5 | 0,7 | V | |
| | $V_{2\text{-}3}$ | – | 0,85 | 1,1 | V | $I_2$ = 400 mA |
| Quiescent current | $I_q$ | 0,8 | 1,3 | 1,8 | mA | |
| Limiting output current | $I_{2\ lim}$ | 0,45 | 0,7 | 1 | A | |
| Multiplication coefficient* | $k = \frac{\Delta I_2}{\Delta I_1}$ | 19,3 | 21,5 | 24,3 | | $\Delta I_2 = \pm 10$ mA |
| Thermal limitation | $T_{j\ lim}$ | 130 | – | 160 | °C | $V_{ref}$ = 1,2 V |
| Line regulation variation | | | | | | |
| $V_{ref}$ versus $V_P$ | $\frac{\Delta V_{ref}}{\Delta V_P}$ | 0<br>0 | 0,9<br>0,07 | 2,0<br>0,16 | mV/V<br>%/V | $V_P$ = 2,1 to 15 V |
| k-spread versus $V_P$ | $\frac{\Delta k}{\Delta V_P}$ | –0,3 | +0,2 | +1 | %/V | $\Delta I_2 = \pm 10$ mA<br>$V_P$ = 2,1 to 15 V |
| $I_q$ versus $V_P$ | $\frac{\Delta I_q}{\Delta V_P}$ | –<br>– | 11<br>0,95 | –<br>– | μA/V<br>%/V | $I_2$ = 0<br>$V_P$ = 2,1 to 15 V |
| Load regulation variation | | | | | | |
| $V_{ref}$ versus $I_2$ | $\frac{\Delta V_{ref}}{\Delta I_2}$ | –0,4<br>–0,03 | 0<br>0 | +0,4<br>+0,03 | V/A<br>%/mA | $I_2$ = 50 to 100 mA |
| k-spread versus $I_2$ | $\frac{\Delta k}{\Delta I_2}$ | –0,05 | 0 | +0,05 | %/mA | $I_2$ = 50 to 100 mA<br>$\Delta I_2 = \pm 10$ mA |
| Temperature coefficient variation | | | | | | |
| $V_{ref}$ versus $T_{amb}$ | $\frac{\Delta V_{ref}}{\Delta T_{amb}}$ | –0,2<br>–0,02 | 0,1<br>0,01 | +0,4<br>+0,04 | mV/K<br>%/K | $T_{amb}$ = –5 to +55 °C |
| k-spread versus $T_{amb}$ | $\frac{\Delta k}{\Delta T_{amb}}$ | –0,03 | 0 | +0,03 | %/K | $T_{amb}$ = –5 to +55 °C<br>$\Delta I_2 = \pm 10$ mA |
| $I_q$ versus $T_{amb}$ | $\frac{\Delta I_q}{\Delta T_{amb}}$ | –<br>– | –1,1<br>–0,08 | –<br>– | μA/K<br>%/K | $T_{amb}$ = –5 to +55 °C<br>$I_2$ = 0 |

* There are 4 ranges of k-factors, indicated by either '1', '2', '3', or '4' on the package. Ordering a specific range is not possible.

1 = 19,3 to 20,5
2 = 20,3 to 21,5
3 = 21,3 to 22,7
4 = 22,5 to 24,3

## APPLICATION INFORMATION




(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 4 Example of using the TDA1559 in a d.c. motor speed regulation circuit.

Notes to Fig. 4

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$ where: $n$ = speed in revolutions per minute

$I_m = T \times \frac{2\pi}{60} = \frac{1}{C.\phi}$

$C$ = motor constant
$\phi$ = magnetic flux
$E_n$ = electromotive force (e.m.f.)
$T$ = motor torque
$R_m$ = motor resistance

$E_n$ can be expressed as:

$$E_n = I_m \left(\frac{R1}{k} - R_m\right) + V_{ref} \left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m \left(\frac{R1}{k} - R_m\right)}$$

Example:

$E_n = E_{2000} = 3{,}58$ V ± 11,6%
$R_m = 13\ \Omega \pm 10\%$
n = 2000 rev/min
T = 1 mNm
R1 = 220 Ω
R2′ = 82 Ω
R2″ = 220 Ω

When a diode (D = BA220) is connected is series with pin 1, then the expressions for R2 and $E_n$ are:

$$R2 = \frac{(V_{ref} + V_D) \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - (V_{ref} + V_D) - I_m \left(\frac{R1}{k} - R_m\right)}$$

$$E_n = I_m \left(\frac{R1}{k} - R_m\right) + \left(V_{ref} + V_D\right) \left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 + I_q$$

Example:

$E_n = E_{2000} = 3{,}58$ V ± 11,6%
$R_m = 13\ \Omega \pm 10\%$
n = 2000 rev/min
T = 1 mNm
R1 = 220 Ω
R2′ = 160 Ω
R2″ = 470 Ω
D = BA220

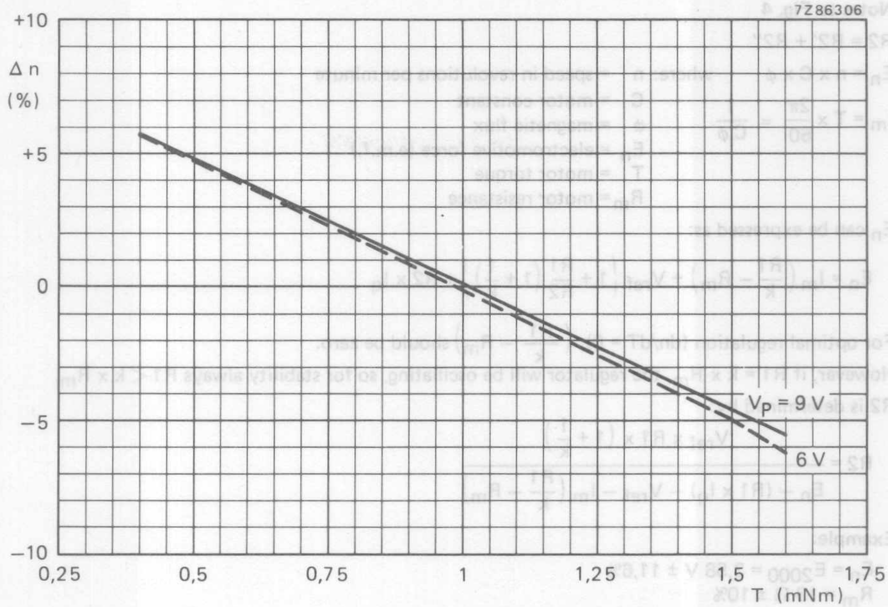



Fig. 5 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at $T_{amb}$ = 25 °C.

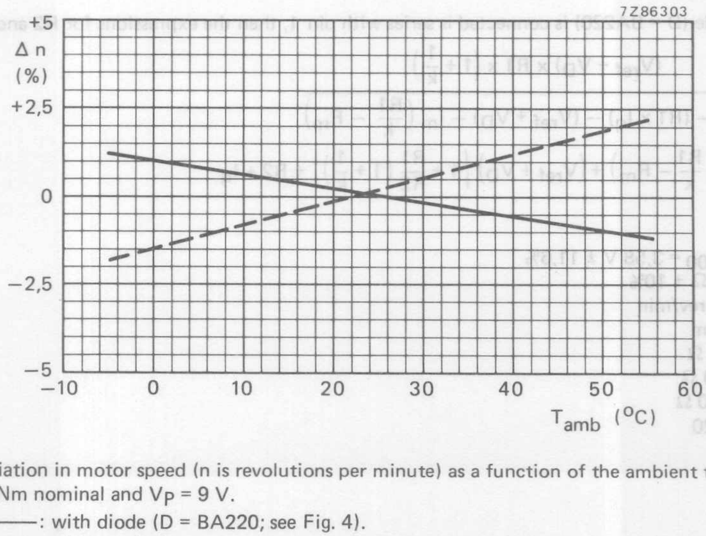



Fig. 6 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1 mNm nominal and $V_P$ = 9 V.

————————: with diode (D = BA220; see Fig. 4).

— — — — — —: without diode.

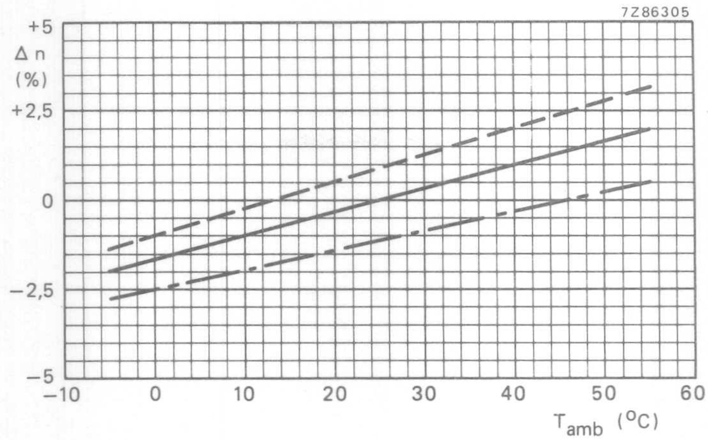



Fig. 7a $V_P$ = 6 V.

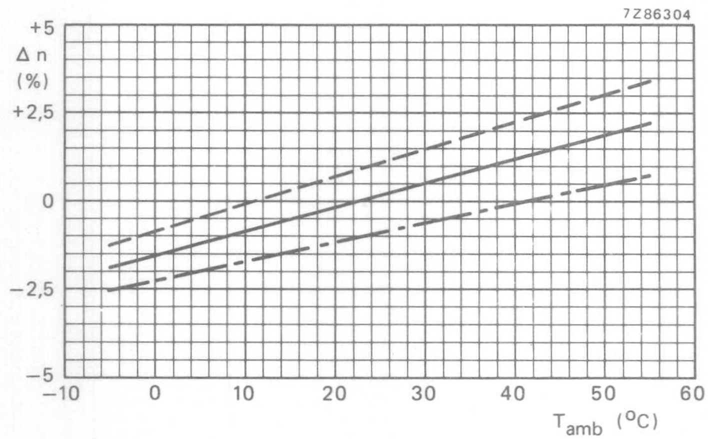



Fig. 7b $V_P$ = 9 V.

Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (D = BA220; see Fig. 4).

– – – – – – – : T = 0,9 mNm
——————— : T = 1,0 mNm
- —— - —— - —— : T = 1,1 mNm

# INTEGRATED FM TUNER FOR RADIO RECEIVERS

## GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

### Features

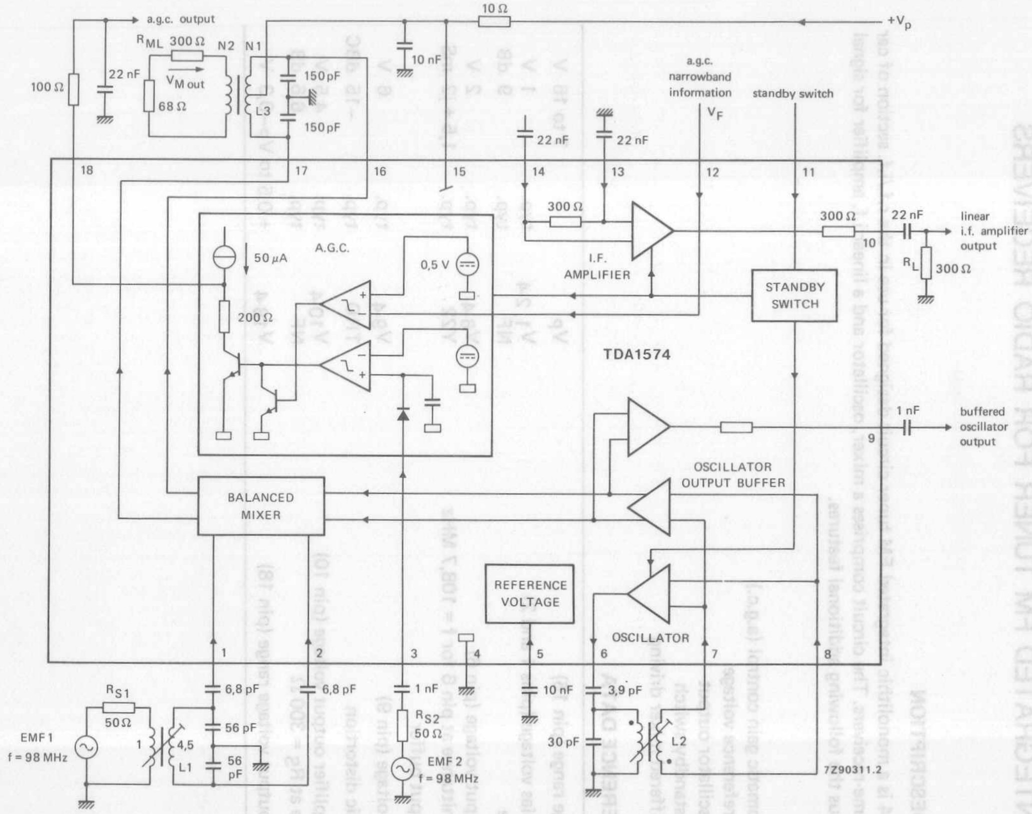
- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 15) | $V_P$ | | 7 to 16 | V |
| Mixer input bias voltage (pins 1 and 2) | $V_{1,2\text{-}4}$ | typ. | 1 | V |
| noise figure | NF | typ. | 9 | dB |
| Oscillator output voltage (pin 6) | $V_{6\text{-}4}$ | typ. | 2 | V |
| output admittance at pin 6 for f = 108,7 MHz | Y22 | typ. | 1,5 + j2 | mS |
| Oscillator output buffer | | | | |
| D.C. output voltage (pin 9) | $V_{9\text{-}4}$ | typ. | 6 | V |
| Total harmonic distortion | THD | typ. | −15 | dBC |
| Linear i.f. amplifier output voltage (pin 10) | $V_{10\text{-}4}$ | typ. | 4,5 | V |
| noise figure at $R_S$ = 300 Ω | NF | typ. | 6,5 | dB |
| Keyed a.g.c. output voltage range (pin 18) | $V_{18\text{-}4}$ | | + 0,5 to $V_P$−0,3 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).




**Coil data**

L1: TOKO MC-108, 514HNE-150014S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

Fig. 1 Block diagram and test circuit.

## FUNCTIONAL DESCRIPTION

### Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

### Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

### Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

### Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrow-band AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 15) | $V_P = V_{15\text{-}4}$ | max. | 18 V |
| Mixer output voltage (pins 16 and 17) | $V_{16,\ 17\text{-}4}$ | max. | 35 V |
| Standby switch input voltage (pin 11) | $V_{11\text{-}4}$ | max. | 23 V |
| Reference voltage (pin 5) | $V_{5\text{-}4}$ | max. | 7 V |
| Field strength input voltage (pin 12) | $V_{12\text{-}4}$ | max. | 7 V |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature range | $T_{stg}$ | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | −40 to + 85 | °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to ambient (in free air) | $R_{th\ j\text{-}amb}$ | = | 80 K/W |

### Note

All pins are short-circuit protected to ground.

## CHARACTERISTICS

$V_P = V_{15\text{-}4} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 15) | | | | | |
| Supply voltage | $V_P = V_{15\text{-}4}$ | 7 | – | 16 | V |
| Supply current (except mixer) | $I_P = I_{15}$ | 16 | 23 | 30 | mA |
| Reference voltage (pin 5) | $V_{5\text{-}4}$ | 3,9 | 4,1 | 4,4 | V |
| **Mixer** | | | | | |
| *D.C. characteristics* | | | | | |
| Input bias voltage (pins 1 and 2) | $V_{1,2\text{-}4}$ | – | 1 | – | V |
| Output voltage (pins 16 and 17) | $V_{16,17\text{-}4}$ | 4 | – | 35 | V |
| Output current (pin 16 + pin 17) | $I_{16} + I_{17}$ | – | 4,0 | – | mA |
| *A.C. characteristics* ($f_i$ = 98 MHz) | | | | | |
| Noise figure | NF | – | 9 | – | dB |
| Noise figure including transforming network | NF | – | 11 | – | dB |
| 3rd order intercept point | $EMF1_{IP3}$ | – | 115 | – | dBμV |
| Conversion power gain | | | | | |
| $10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$ | $G_P$ | – | 14 | – | dB |
| Input resistance (pins 1 and 2) | $R_{1,2\text{-}4}$ | – | 14 | – | Ω |
| Output capacitance (pins 16 and 17) | $C_{16,17}$ | – | 13 | – | pF |
| **Oscillator** | | | | | |
| *D.C. characteristics* | | | | | |
| Input voltage (pins 7 and 8) | $V_{7,8\text{-}4}$ | – | 1,3 | – | V |
| Output voltage (pin 6) | $V_{6\text{-}4}$ | – | 2 | – | V |
| *A.C. characteristics* ($f_{osc}$ = 108,7 MHz) | | | | | |
| Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs | Δf | – | 2,2 | – | Hz |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Linear i.f. amplifier** | | | | | |
| *D.C. characteristics* | | | | | |
| Input bias voltage (pin 13) | $V_{13\text{-}4}$ | – | 1,2 | – | V |
| Output voltage (pin 10) | $V_{10\text{-}4}$ | – | 4,5 | – | V |
| *A.C. characteristics* ($f_i$ = 10,7 MHz) | | | | | |
| Input impedance | | | | | |
| | $R_{14\text{-}13}$ | 240 | 300 | 360 | Ω |
| | $C_{14\text{-}13}$ | – | 13 | – | pF |
| Output impedance | | | | | |
| | $R_{10\text{-}4}$ | 240 | 300 | 360 | Ω |
| | $C_{10\text{-}4}$ | – | 3 | – | pF |
| Voltage gain | | | | | |
| $20 \log \frac{V_{10\text{-}4}}{V_{14\text{-}13}}$ | $G_{VIF}$ | 27 | 30 | – | dB |
| $T_{amb}$ = –40 to + 85 °C | $\Delta G_{VIF}$ | – | 0 | – | dB |
| 1 dB compression point (r.m.s. value) | | | | | |
| at $V_P$ = 8,5 V | $V_{10\text{-}4rms}$ | – | 750 | – | mV |
| at $V_P$ = 7,5 V | $V_{10\text{-}4rms}$ | – | 550 | – | mV |
| Noise figure | | | | | |
| at $R_S$ = 300 Ω | NF | – | 6,5 | – | dB |
| **Keyed a.g.c.** | | | | | |
| *D.C. characteristics* | | | | | |
| Output voltage range (pin 18) | $V_{18\text{-}4}$ | 0,5 | – | $V_P$–0,3 | V |
| A.G.C. output current | | | | | |
| at $I_3 = \phi$ or | | | | | |
| $V_{12\text{-}4}$ = 450 mV; $V_{18\text{-}4} = V_P/2$ | $-I_{18}$ | 25 | 50 | 100 | μA |
| at $V_{3\text{-}4}$ = 2 V and | | | | | |
| $V_{12\text{-}4}$ = 1 V; $V_{18\text{-}4} = V_{15\text{-}4}$ | $I_{18}$ | 2 | – | 5 | mA |

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Narrowband threshold | | | | | |
| at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 550 mV | $V_{18\text{-}4}$ | – | | 1 | V |
| at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 450 mV | $V_{18\text{-}4}$ | $V_P$–0,3 | – | – | V |
| *A.C. characteristics* ($f_i$ = 98 MHz) | | | | | |
| Input impedance | $R_{3\text{-}4}$ | – | 4 | – | kΩ |
| | $C_{3\text{-}4}$ | – | 3 | | pF |
| Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5) | | | | | |
| at $V_{12\text{-}4}$ = 0,7 V; $V_{18\text{-}4} = V_P/2$; $I_{18}$ = 0 | $EMF2_{rms}$ | – | 17 | – | mV |
| **Oscillator output buffer** (pin 9) | | | | | |
| D.C. output voltage | $V_{9\text{-}4}$ | – | 6,0 | – | V |
| Oscillator output voltage (r.m.s. value) | | | | | |
| at $R_L = \infty$; $C_L$ = 2 pF | $V_{9\text{-}4(rms)}$ | – | 110 | – | mV |
| at $R_L$ = 75 Ω | $V_{9\text{-}4(rms)}$ | 30 | 50 | – | mV |
| D.C. output impedance | $R_{9\text{-}15}$ | – | 2,5 | – | kΩ |
| Signal purity | | | | | |
| Total harmonic distortion | THD | – | –15 | – | dBC |
| Spurious frequencies | | | | | |
| at EMF1 = 0,2 V; $R_{S1}$ = 50 Ω | $f_S$ | – | –35 | – | dBC |
| **Electronic standby switch** (pin 11) | | | | | |
| Oscillator; linear i.f. amplifier; a.g.c. | | | | | |
| at $T_{amb}$ = –40 to + 85 °C | | | | | |
| Input switching voltage | | | | | |
| for threshold ON; $V_{18\text{-}4} = \geqslant V_P$–3 V | $V_{11\text{-}4}$ | 0 | – | 2,3 | V |
| for threshold OFF; $V_{18\text{-}4} = \leqslant 0{,}5$ V | $V_{11\text{-}4}$ | 3,3 | – | 23 | V |
| Input current | | | | | |
| at ON condition; $V_{11\text{-}4}$ = 0 V | $-I_{11}$ | – | – | 150 | μA |
| at OFF condition; $V_{11\text{-}4}$ = 23 V | $I_{11}$ | – | – | 10 | μA |
| Input voltage | | | | | |
| at $I_{11} = \phi$ | $V_{11\text{-}4}$ | – | – | 4,4 | V |

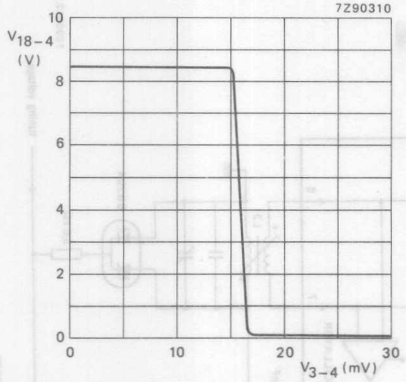



Fig. 2 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $I_{18} = \phi$.

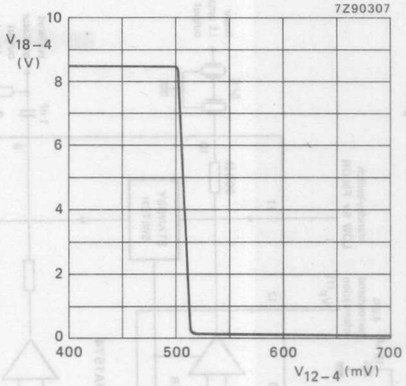



Fig. 3 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $I_{18} = \phi$.

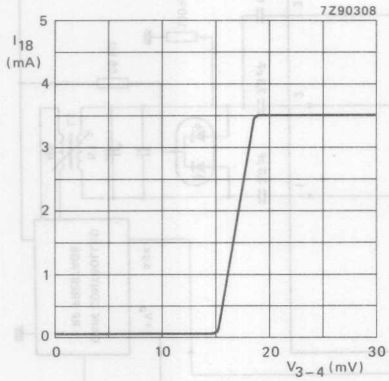



Fig. 4 Keyed a.g.c. output current $I_{18}$ as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $V_{18\text{-}4} = 8{,}5$ V.

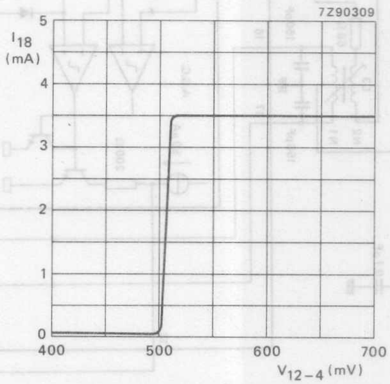



Fig. 5 Keyed a.g.c. output current $I_{18}$ as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $V_{18\text{-}4} = 8{,}5$ V.

## APPLICATION INFORMATION

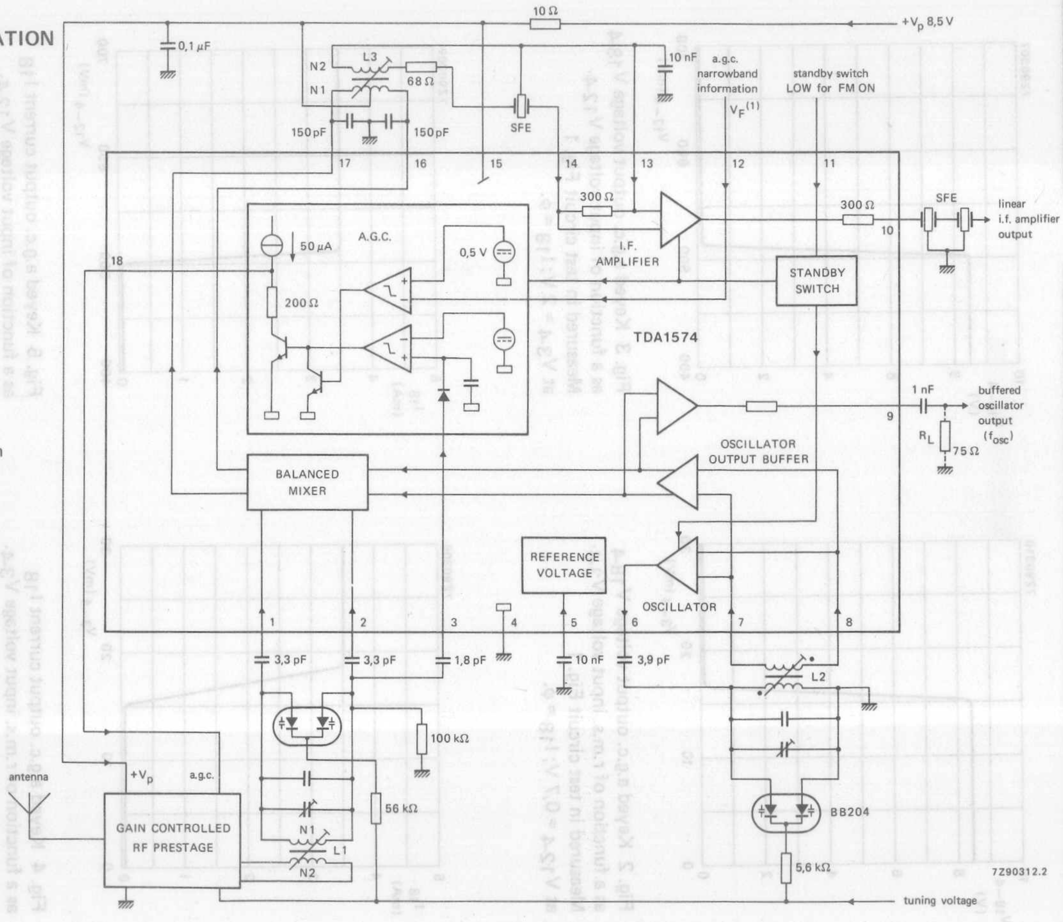



Fig. 6 TDA1574 application diagram.

**Coil data**

L1: TOKO MC-108, 514HNE-15023S15, N1 = 5,5 turns, N2 = 1 turn

L2: L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

# FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

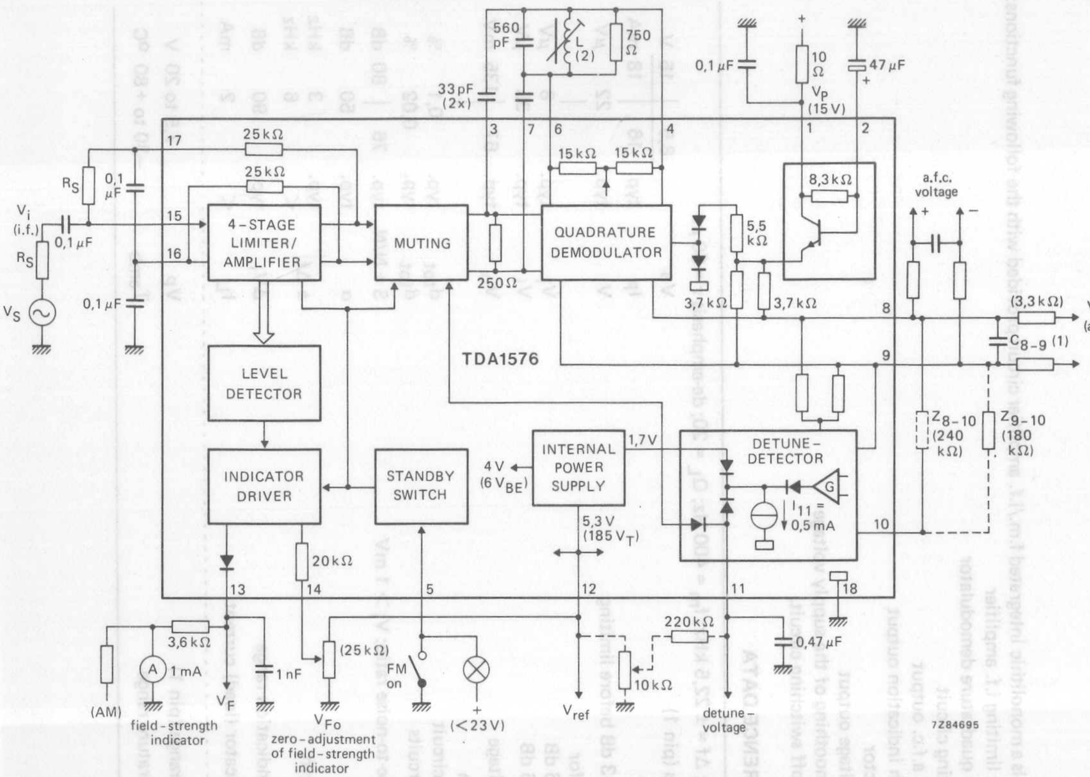
## QUICK REFERENCE DATA

$f_o$ = 10,7 MHz; $\Delta f$ = ± 22,5 kHz; $f_m$ = 400 Hz; $Q_L$ = 20; de-emphasis $\tau$ = 50 $\mu$s

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply voltages (pin 1) | $V_P$ | | 8,5 | | 15 | V |
| Supply current | $I_P$ | typ. | 16 | | 18 | mA |
| Sensitivity at −3 dB before limiting | $V_i$ | typ. | | 22 | | $\mu$V |
| I.F. sensitivity for | | | | | | |
| S + N/N = 26 dB | $V_i$ | typ. | | 8 | | $\mu$V |
| S + N/N = 46 dB | $V_i$ | typ. | | 35 | | $\mu$V |
| A.F. output voltage | $V_o$ | typ. | 67 | | 135 | mV |
| Total distortion | | | | | | |
| single tuned circuit | $d_{tot}$ | typ. | | 0,1 | | % |
| two tuned circuits | $d_{tot}$ | typ. | | 0,02 | | % |
| Signal plus noise-to-noise ratio; $V_i > 1$ mV | S + N/N | typ. | 76 | | 80 | dB |
| A.M. rejection | $\alpha$ | typ. | | 50 | | dB |
| A.F.C. offset drift | $\pm \Delta f$ | typ. | | 3 | | kHz |
| | | < | | 6 | | kHz |
| Field-strength indication range | $\Delta V_i$ | typ. | | 90 | | dB |
| Permissible indicator (load) current | $I_L$ | < | | 2 | | mA |
| Supply voltage range (pin 1) | $V_P$ | | | 7,5 to 20 | | V |
| Ambient temperature range | $T_{amb}$ | | | −30 to +80 | | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).




(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) $L = 0{,}38\ \mu H$; $Q_o = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion ($d_2$); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}18}$ | max. | 23 V |
| Voltages | | | |
| at pin 2 | $V_{2\text{-}18}$ | max. | $V_P$ V |
| | $-V_{2\text{-}18}$ | max. | 0 V |
| at pin 5 | $V_{5\text{-}18}$ | max. | 23 V |
| | $-V_{5\text{-}18}$ | max. | 0 V |
| at pin 12 | $V_{12\text{-}18}$ | max. | 7 V |
| | $-V_{12\text{-}18}$ | max. | 0 V |
| at pin 13 | $V_{13\text{-}18}$ | max. | 6 V |
| at pin 14 | $V_{14\text{-}18}$ | max. | 23 V |
| | $-V_{14\text{-}18}$ | max. | 0 V |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From crystal to ambient | $R_{th\ cr\text{-}a}$ | = | 80 K/W |

## CHARACTERISTICS

$f_o$ = 10,7 MHz; $\Delta f = \pm$ 22,5 kHz; $f_m$ = 400 Hz; $R_S = 60\ \Omega$; de-emphasis $\tau = 50\ \mu s$ ($C_{8\text{-}9}$ = 6,8 nF); $T_{amb}$ = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic ($d_2$) distortion: $V_i$ = 1 mV; $\Delta f = \pm$ 75 kHz.

| Parameter | Symbol | | $V_P$ = 8,5 V | $V_P$ = 15 V | Unit |
|---|---|---|---|---|---|
| Supply voltage range (pin 1) | $V_P$ | | 7,5 to 20 | | V |
| Supply current; without load ($I_{12} = I_{13} = 0$) | $I_P$ | typ. | 16 | 18 | mA |
| | | | 10 to 23 | 12 to 25 | mA |
| **I.F. amplifier/detector** | | | | | |
| Sensitivity at −3 dB before limiting | $V_i$ | typ. | 22 | | $\mu$V |
| | | < | 30 | | $\mu$V |
| I.F. sensitivity for | | | | | |
| S + N/N = 26 dB | $V_i$ | typ. | 8 | | $\mu$V |
| S + N/N = 46 dB | $V_i$ | typ. | 35 | | $\mu$V |
| I.F. output voltage (peak-to-peak value) $V_i$ = 1 mV; $Z_{3\text{-}18} = Z_{7\text{-}18}$ = 1 M$\Omega$ in parallel with 10 pF | $V_{3\text{-}7(p\text{-}p)}$ | typ. | 680 | | mV |
| I.F. output resistance | $R_{3\text{-}7}$ | typ. | 250 | | $\Omega$ |
| Detector input impedance | $R_{4\text{-}6}$ | typ. | 30 | | k$\Omega$ |
| | $C_{4\text{-}6}$ | typ. | 1 | | pF |
| Output resistance | $R_8$; $R_9$ | typ. | 3,7 | | k$\Omega$ |
| D.C. output voltage | $V_{8\text{-}18} = V_{9\text{-}18}$ | typ. | 5,5 | 9,8 | V |
| A.F. output voltage; $Q_L$ = 20 | $V_o$ | typ. | 67 | 135 | mV |
| | | | 60 to 75 | 120 to 150 | mV |
| Total distortion | | | | | |
| single tuned circuit; $Q_L$ = 20 | $d_{tot}$ | typ. | 0,1 | | % |
| two tuned circuits | $d_{tot}$ | typ. | 0,02 | | % |
| Signal plus noise-to-noise ratio B = 250 Hz to 15 kHz; $V_i$ > 1 mV | S + N/N | typ. | 76 | 80 | dB |
| A.M. rejection; $V_i$ = 10 mV f.m.: $f_m$ = 70 Hz; $\Delta f = \pm$ 22,5 kHz a.m.: $f_m$ = 1 kHz; m = 0,3 | $\alpha$ | typ. | 54 | | dB* |
| I.F. input voltage range; $\alpha$ > 40 dB | $V_i$ | | 0,5 to 500 | | mV |
| Hum suppression at f = 100 Hz $V_P = V_{1\text{-}18}$ = 100 mV r.m.s.; $C_{2\text{-}18}$ = 47 $\mu$F | $\alpha_{100}$ | > | 43 | | dB |
| | | typ. | 48 | | dB |
| A.F.C. tuning slope at $Q_L$ = 20 | $\frac{\Delta V_{8\text{-}9}}{\Delta f_o}$ | typ. | 8,5 | 17 | mV/kHz |
| A.F.C. offset voltages; $Q_L$ = 20 at $V_i$ = 1 mV | $\pm \Delta V_{8\text{-}9}$ | < | 100 | 200 | mV |
| at $V_i$ = 30 $\mu$V to 500 mV (reference at 1 mV and muting) | $\pm \Delta V_{8\text{-}9}$ | typ. | 25 | 50 | mV |
| | | < | 50 | 100 | mV |

* Simultaneously measured.

| Parameter | Symbol | | $V_P = 8,5$ V | $V_P = 15$ V | Unit |
|---|---|---|---|---|---|
| **Field-strength indication** | | | | | |
| Indicator sensitivity; $I_{14} = 0$ | $V_i$ | | 20 $\mu$V to 600 mV | | |
| Field-strength indicator voltage $R_{13\text{-}18} = 3,6\ k\Omega$; $I_{14} = 0$ | | | | | |
| $V_i = 0$ | $V_F = V_{13\text{-}18}$ | typ. | 0 | | mV |
| | | < | 200 | | mV |
| $V_i = 250$ mV | $V_F = V_{13\text{-}18}$ | typ. | 3,6 | | V |
| | | | 3,2 to 4,1 | | V |
| Available output current | $-I_{13}$ | > | 2 | | mA |
| Reverse voltage at the output for FM 'off'; $V_{5\text{-}18} > 3,5$ V | $V_{13\text{-}18}$ | > | 5 | | V |
| **Detune-detector** | | | | | |
| Quiescent input current; $V_{10\text{-}9} = 0$ | $I_{10}$ | typ. | 20 | | nA |
| | | < | 100 | | nA |
| Output voltage range | $V_{11\text{-}18}$ | | 1,8 to 5,0 | | V |
| Available output current | $I_{11}$ | typ. | 0,5 | | mA |
| | | | 0,35 to 0,65 | | mA |
| Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10\text{-}9})$ at $I_{11} = 0,25$ mA | $G_v$ | typ. | – | 3,3 | |
| Input offset voltage (pin 10) at $V_{11\text{-}18} = 2,5$ V | $V_{10\text{-}9}$ | typ. | 20 | | mV |
| **Reference voltage** | | | | | |
| Output voltage; $-I_{12} = 1$ mA | $V_{ref} = V_{12\text{-}18}$ | typ. | 5,1 | 5,3 | V |
| Available output current | $-I_{12}$ | typ. | 2,5 | | mA |
| **Standby switch** | | | | | |
| Required control voltage within the rated ambient temperature and supply voltage ranges for FM 'on' | $V_{5\ on}$ | < | 2 | | V |
| for FM 'off' | $V_{5\ off}$ | > | 3,5 | | V |
| Input switching current for FM 'on' | $-I_5$ | < | 100 | | $\mu$A |

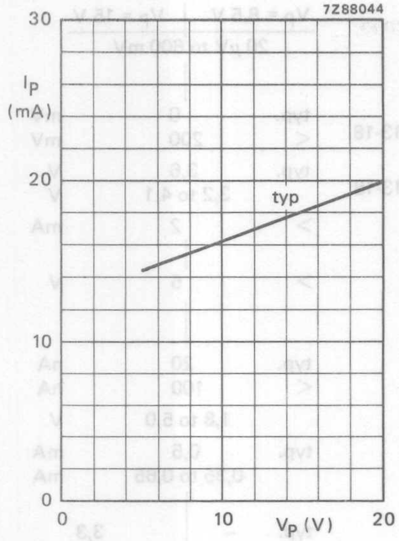



Fig. 2 Supply current consumption; without load.

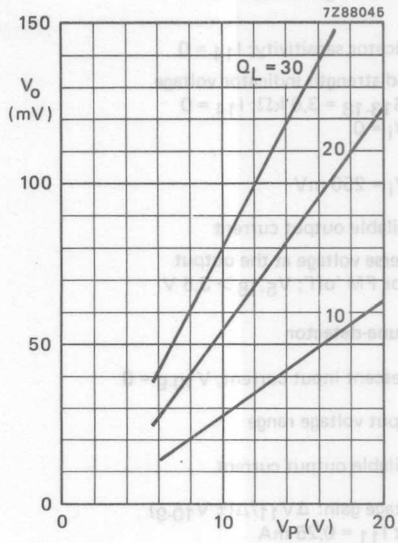



Fig. 3 A.F. output voltage; $V_i$ = 1 mV (i.f.); $\Delta f = \pm$ 15 kHz; $f_m$ = 400 Hz; typical values.

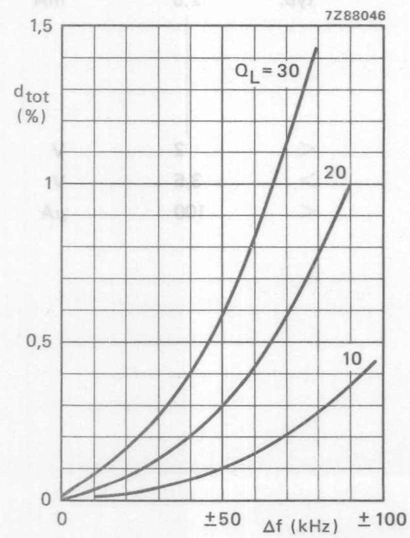



Fig. 4 Total distortion for single tuned circuit; $V_i$ = 1 mV (i.f.); $f_m$ = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

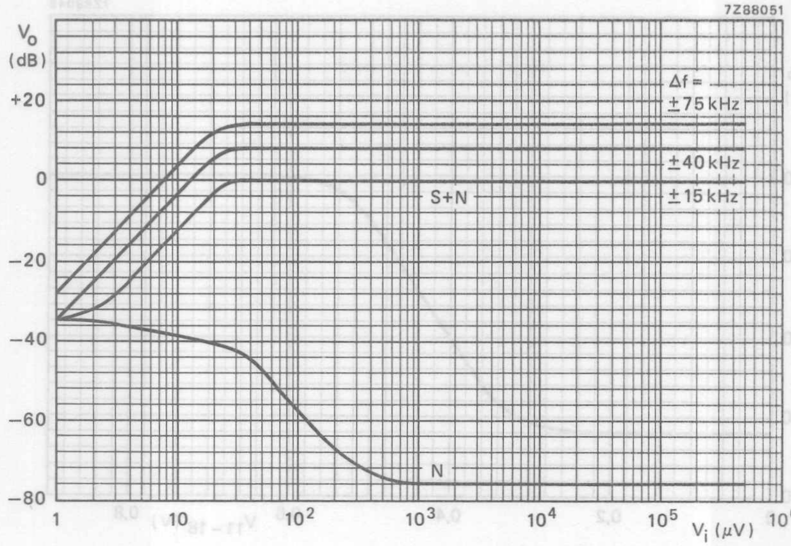



Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; $V_P$ = 15 V; $f_m$ = 400 Hz; B = 250 Hz to 16 kHz; $Q_L$ = 20; $C_{8\text{-}9}$ = 6,8 nF; typical values.

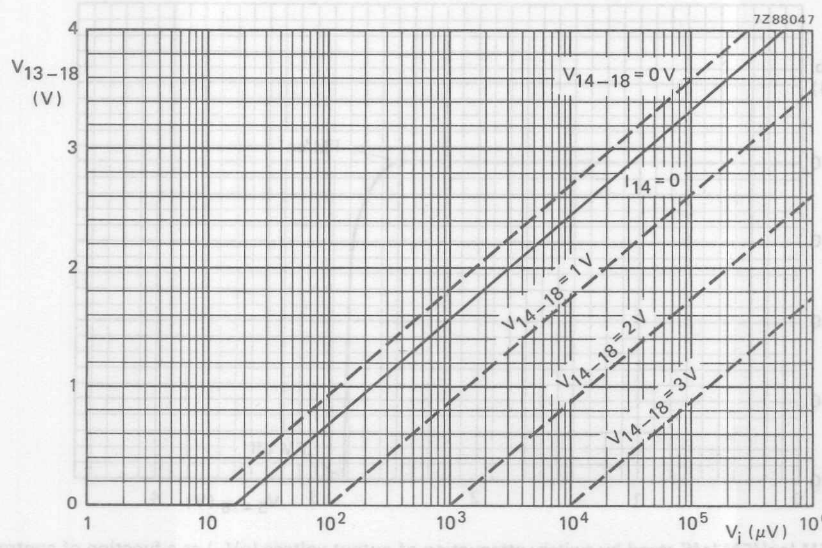



Fig. 6 Voltage at field-strength indicator output (proportional to $V_{12\text{-}18}$); $R_{13\text{-}18}$ = 3,6 kΩ.

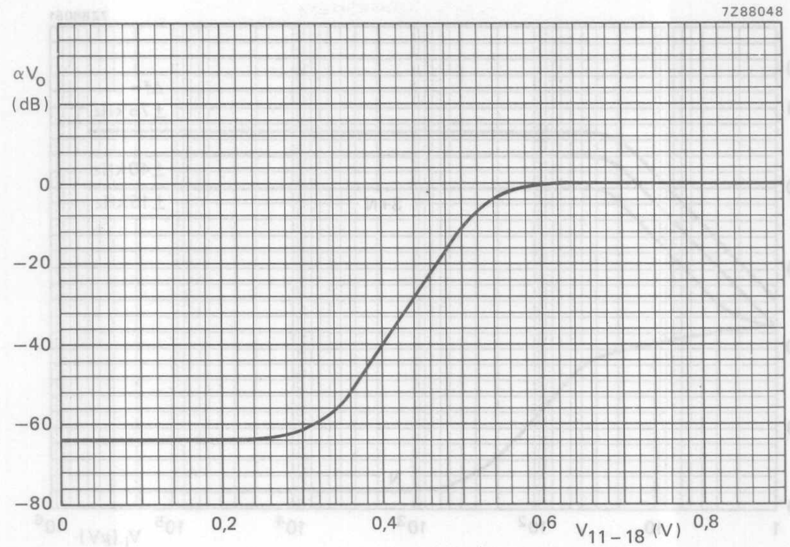



Fig. 7 Attenuation of output voltage ($\alpha V_o$) as a function of the muting control voltage $V_{11\text{-}18}$.

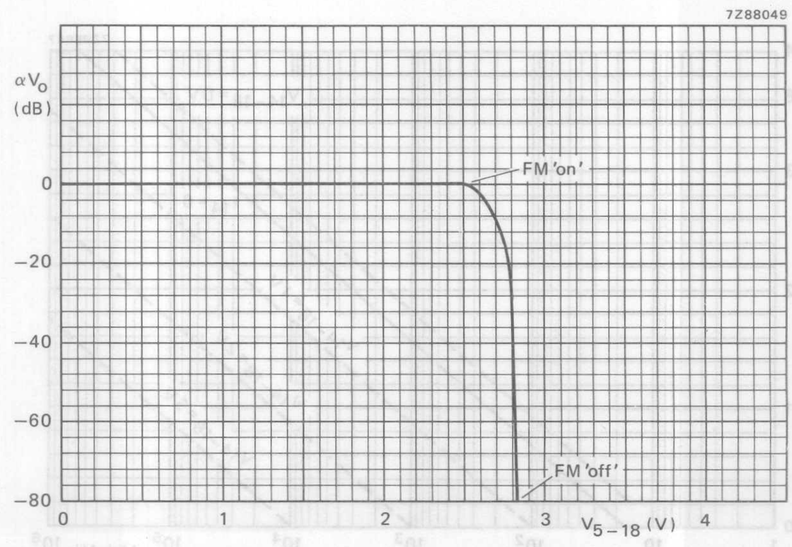
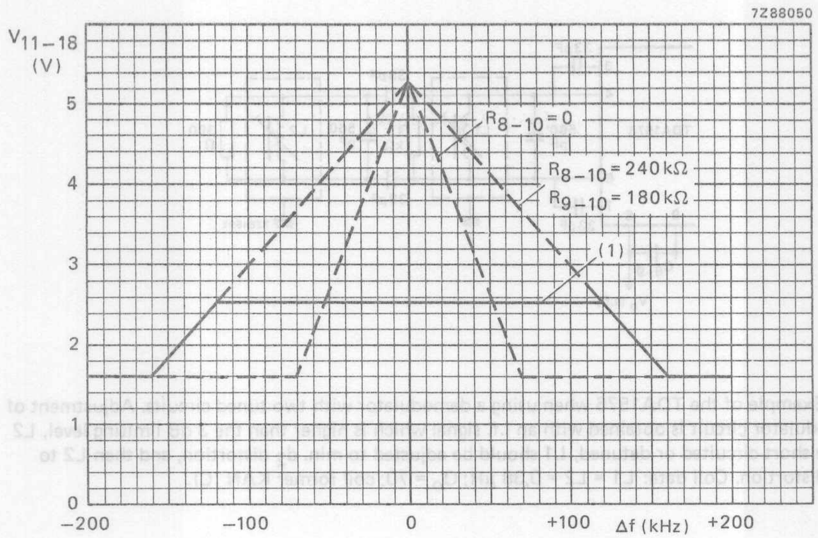



Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage ($\alpha V_o$) as a function of control voltage $V_{5\text{-}18}$.




(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; $V_P$ = 7,5 to 20 V; $Q_L$ = 20.

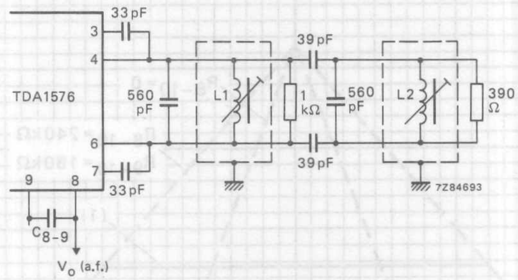



Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. $d_2$ distortion, and then L2 to min. $d_2$ distortion. Coil data: L1 = L2 = 0,38 $\mu$H; $Q_o$ = 70; coil former KAN (C).

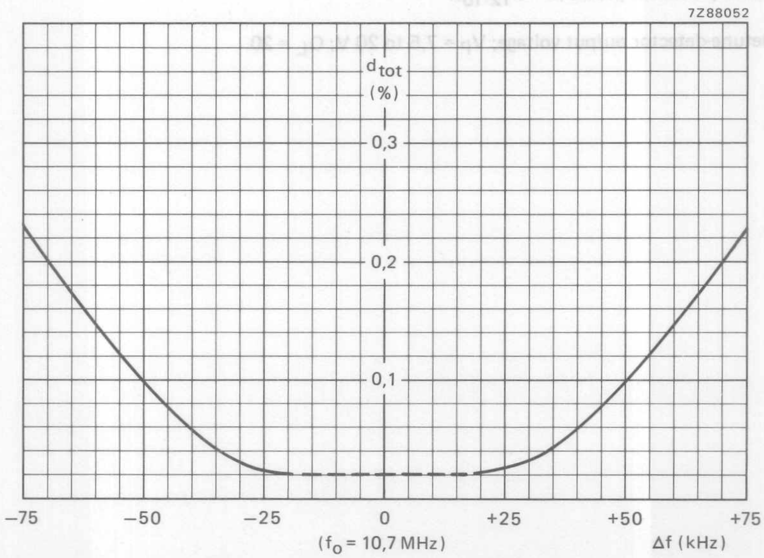
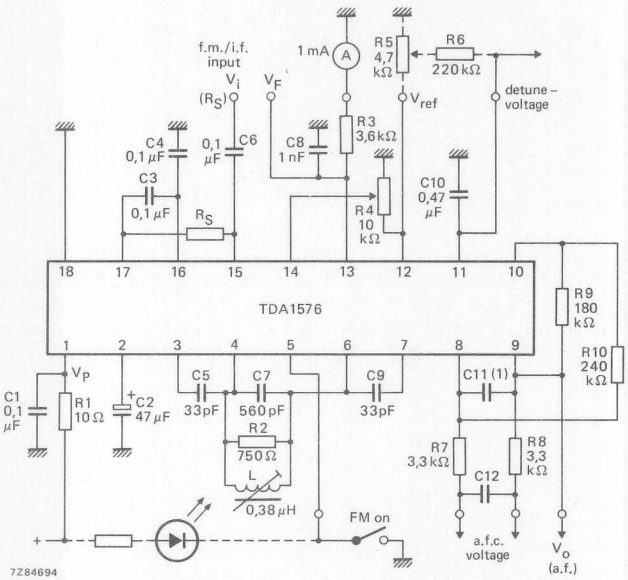



Fig. 11 Total distortion as a function of detuning; $f_m$ = 400 Hz; $C_{8\text{-}9}$ = 6,8 nF; Δf = ± 75 kHz; $V_o$ = 330 mV for a frequency deviation Δf = ± 75 kHz.




(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

# TIME MULTIPLEX PLL STEREO DECODER

## GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

**Features**

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

## QUICK REFERENCE DATA

Measured with a frequency deviation $\Delta f = \pm$ 75 kHz without pilot; $f_m$ = 1 kHz

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply voltage (pin 8) | | $V_P = V_{8\text{-}7}$ | typ. | 8,5 | 15 | V |
| Supply current (pin 8) | | $I_P = I_8$ | typ. | 21 | 30 | mA |
| Multiplex input signal (adjustable) | | $V_{MUX(p\text{-}p)}$ | typ. | 0,5 | 1 | V |
| Input resistance (adjustable) | | $R_i$ | typ. | 47 | | kΩ |
| A.F. output voltage (R = 15 kΩ) | | $V_o$ | typ. | 0,75 | 1,5 | V |
| Output resistance | | $R_o$ | | low-ohmic | | |
| Spread in gain | | $\Delta G_v$ | ⩽ | 1 | | dB |
| Channel separation | | $\alpha$ | typ. | 50 | | dB |
| Total harmonic distortion | | THD | ⩽ | 0,3 | 0,1 | % |
| Signal-to-noise ratio | | S/N | typ. | 90 | | dB |
| Carrier and harmonic suppression | | | | | | |
| pilot signal; | f = 19 kHz | $\alpha_{19}$ | typ. | 32 | | dB |
| subcarrier; | f = 38 kHz | $\alpha_{38}$ | typ. | 50 | | dB |
| | f = 57 kHz | $\alpha_{57}$ | typ. | 46 | | dB |
| | f = 76 kHz | $\alpha_{76}$ | typ. | 60 | | dB |
| traffic radio (V.W.F.); | f = 57 kHz | $\alpha_{57(VWF)}$ | typ. | 70 | | dB |
| SCA (Subsidiary Communications Authorization); | f = 67 kHz | $\alpha_{67}$ | typ. | 70 | | dB |
| ACI (Adjacent Channel Interference); | f = 114 kHz | $\alpha_{114}$ | typ. | 80 | | dB |
| intermodulation; | f = 10/13 kHz | $\alpha_2, \alpha_3$ | typ. | 70 | | dB |
| Supply voltage range (pin 8) | | $V_P = V_{8\text{-}7}$ | | 7,5 to 18 | | V |
| Operating ambient temperature range | | $T_{amb}$ | | −30 to +80 | | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

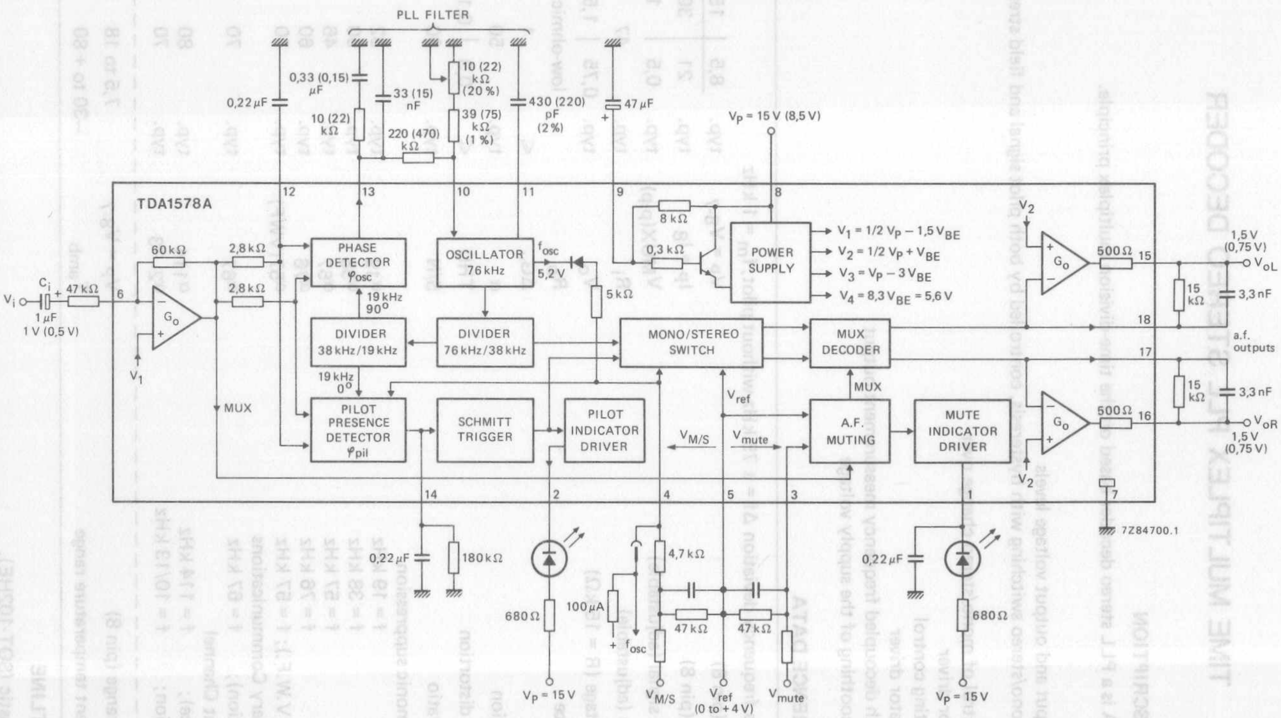



Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for Vp = 8,5 V.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 8) | $V_P = V_{8\text{-}7}$ | max. | 20 | V |
| Input voltages (pins 3, 4 and 5) | $V_{3;4;5\text{-}7}$ | | 0 to 12 | V |
| Indicator driver output voltage | $V_{1;2\text{-}7}$ | max. | 24 | V |
| Indicator driver output current | $I_1; I_2$ | max. | 30 | mA |
| Total power dissipation at $T_{amb}$ = 25 °C | $P_{tot}$ | max. | 1,2 | W |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 80 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From crystal to ambient | $R_{th\ c\text{-}a}$ | = | 80 | K/W |

**CHARACTERISTICS** (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz);
modulation frequency: 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V;
de-emphasizing time: T = 50 $\mu$s; oscillator adjusted to $f_{osc}$ at a pilot voltage $V_i = 0$ V;
$T_{amb} = 25$ °C; unless otherwise specified

| parameter | $V_P$ (V) | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply voltage range (pin 8) | – | $V_P$ | 7,5 | – | 18 | V |
| Supply current (except output and indicator) pin 8 | 8,5 | $I_P$ | – | 21 | | mA |
| | 15 | $I_P$ | – | 30 | 40 | mA |
| Nominal multiplex input voltage (peak-to-peak value) | 8,5 | $V_{MUX(p\text{-}p)}$ | – | 0,5 | | V |
| $R_i = 47$ kΩ | 15 | $V_{MUX(p\text{-}p)}$ | – | 1,0 | – | V |
| Overdrive reserve of input at THD = 1 % | 8,5 | | 3 | 6 | – | dB |
| at THD = 0,3 % | 15 | | 3 | 6 | – | dB |
| A.F. output voltage (r.m.s. value; mono without pilot) $R_{15\text{-}18} = R_{16\text{-}17} = 15$ kΩ | 8,5 | $V_{o(rms)}$ | – | 0,75 | – | V |
| | 15 | $V_{o(rms)}$ | – | 1,5 | – | V |
| $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ | 8,5 | $V_{o(rms)}$ | – | 1,2 | – | V |
| | 15 | $V_{o(rms)}$ | – | 2,4 | – | V |
| Overdrive reserve of output $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ | * | | 3 | – | – | dB |
| Spread in output voltage levels | * | $\pm \Delta V_o/V_o$ | – | – | 1 | dB |
| Difference of output voltage levels | * | $\pm \Delta V_{15\text{-}16}/V_o$ | – | – | 1 | dB |
| Output resistance | * | $R_o$ | low-ohmic | | | |
| Available output current pins 15 and 16 | * | $\pm I_o$ | – | – | – | mA |
| Modulation range at output (unloaded) | * | $V_{15;16\text{-}7}$ | – | 1 to $V_{9\text{-}7}-1$ | – | V |
| Internal current limiting | * | $I_o$ | – | 15 | – | mA |
| D.C. output voltage | 8,5 | $V_{15;16\text{-}7}$ | 3,6 | 4,1 | 4,6 | V |
| $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ | 15 | $V_{15;16\text{-}7}$ | 7,0 | 7,7 | 8,4 | V |
| D.C. current | 8,5 | $-I_{17;18}$ | – | 33 | – | $\mu$A |
| (pins 17 and 18) | 15 | $-I_{17;18}$ | – | 23 | – | $\mu$A |

* $V_P$ = 8,5 or 15 V.

| parameter | $V_P$ (V) | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Channel separation at $V_{4\text{-}5} = 0$ V | 8,5 | $\alpha$ | 32 | 50 | – | dB |
| | 15 | $\alpha$ | 39 | 50 | – | dB |
| Total harmonic distortion | 8,5 | THD | – | 0,1 | 0,3 | % |
| | 15 | THD | – | 0,04 | 0,1 | % |
| Signal-to-noise ratio f = 20 Hz to 16 kHz | 8,5 | S/N | – | 87 | – | dB |
| | 15 | S/N | – | 90 | – | dB |
| Carrier and harmonic suppression at the output | | | | | | |
| pilot signal; f = 19 kHz | * | $\alpha_{19}$ | – | 32 | – | dB |
| subcarrier; f = 38 kHz | * | $\alpha_{38}$ | 40 | 50 | – | dB |
| f = 57 kHz | * | $\alpha_{57}$ | – | 46 | – | dB |
| f = 76 kHz | * | $\alpha_{76}$ | – | 60 | – | dB |
| intermodulation (note 1) $f_m = 10$ kHz; spurious signal $f_s = 1$ kHz | | | | | | |
| PLL-filter Fig. 1 | * | $\alpha_2$ | – | 50 | | dB |
| PLL-filter Fig. 2 | * | $\alpha_2$ | – | 70 | | dB |
| $f_m = 13$ kHz; spurious signal $f_s = 1$ kHz | * | $\alpha_3$ | – | 75 | | dB |
| traffic radio (V.W.F.); f = 57 kHz (note 2) | * | $\alpha_{57(VWF)}$ | – | 70 | – | dB |
| SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4) | * | $\alpha_{67}$ | – | 70 | – | dB |
| ACI (Adjacent Channel Interference) (note 3); f = 114 kHz | * | $\alpha_{114}$ | – | 80 | – | dB |
| f = 190 kHz | * | $\alpha_{190}$ | – | 52 | | dB |
| Ripple rejection at the output; f = 100 Hz; $V_{P(rms)} = 100$ mV (pin 8) | * | $RR_{100}$ | 40 | 43 | – | dB |
| Voltage on filter capacitor without external load | * | $V_{9\text{-}7}$ | – | $V_P$–0,25 | | V |
| Source resistance | * | $R_{9\text{-}8}$ | 6 | 8 | 10 | kΩ |

* $V_P = 8{,}5$ or 15 V.

**CHARACTERISTICS** (continued)

| parameter | $V_P$ (V) | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Mono/stereo control** | | | | | | |
| Pilot threshold voltages (peak-to-peak values) | | | | | | |
| for stereo 'ON' | 8,5 | $V_{i(p-p)}$ | – | 21 | 30 | mV |
| | 15 | $V_{i(p-p)}$ | – | 43 | 61 | mV |
| for mono 'ON' | 8,5 | $V_{i(p-p)}$ | 6 | 15 | – | mV |
| | 15 | $V_{i(p-p)}$ | 12 | 30 | – | mV |
| Switch hysteresis $V_{i\,ON}/V_{i\,OFF}$ | * | $\Delta V_i$ | – | 3 | – | dB |
| Switching time at $C_{14\text{-}7}$ = 0,22 $\mu$F | | | | | | |
| for stereo 'ON' | * | $t_{st\,ON}$ | – | 15 | – | ms |
| for mono 'ON' | * | $t_{m\,ON}$ | – | 27 | – | ms |
| **External mono/stereo control** (see Fig. 12 and note 5) | | | | | | |
| Switching voltage for external mono control | 8,5 | $V_{14\text{-}7}$ | – | – | 0,7 | V |
| | 15 | $V_{14\text{-}7}$ | – | – | 1,4 | V |
| | * | or: $-V_{4\text{-}5}$ | 315 | – | – | mV |
| Control voltage for channel separation: $\alpha$ = 6 dB | 8,5 | $-V_{4\text{-}5}$ | – | 120 | – | mV |
| | 15 | $-V_{4\text{-}5}$ | – | 130 | – | mV |
| | * | $\Delta V_{4\text{-}5}$ | – | – | ± 20 | mV |
| $\alpha$ = 26 dB | 8,5 | $-V_{4\text{-}5}$ | – | 70 | – | mV |
| | 15 | $-V_{4\text{-}5}$ | – | 80 | – | mV |
| Control voltage for mono 'ON' | 8,5 | $-V_{4\text{-}5}$ | – | 240 | – | mV |
| | 15 | $-V_{4\text{-}5}$ | – | 270 | – | mV |
| for stereo 'ON' | 8,5 | $-V_{4\text{-}5}$ | – | 220 | – | mV |
| | 15 | $-V_{4\text{-}5}$ | – | 250 | – | mV |
| Control voltage difference for $\alpha$ = 6 dB; stereo 'ON' | 8,5 | $\Delta V_{4\text{-}7}$ | 80 | 100 | 120 | mV |

* $V_P$ = 8,5 or 15 V.

| parameter | $V_P$ (V) | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Muting circuit** (see Fig. 13 and note 5) | | | | | | |
| Control voltage for an attenuation: $\alpha$ = 3 dB | 8,5 | $-V_{3\text{-}5}$ | – | 140 | | mV |
| | 15 | $-V_{3\text{-}5}$ | – | 145 | | mV |
| | * | $\Delta V_{3\text{-}5}$ | – | ± 20 | – | mV |
| $\alpha$ = 26 dB | 8,5 | $-V_{3\text{-}5}$ | – | 255 | | mV |
| | 15 | $-V_{3\text{-}5}$ | – | 270 | – | mV |
| Attenuation with $V_{3\text{-}5}$ = 0 V | * | $\alpha$ | – | – | 0,2 | dB |
| with $-V_{3\text{-}5}$ = 450 mV | * | $\alpha$ | – | 80 | | dB |
| LED driver output current at an attenuation: $\alpha$ = 3 dB | * | $I_1$ | 1,2 | 1,7 | 2,2 | mA |
| Control voltage for $I_1$ = 200 $\mu$A | 8,5 | $-V_{3\text{-}5}$ | – | 150 | – | mV |
| | 15 | $-V_{3\text{-}5}$ | – | 160 | – | mV |
| **Control inputs** | | | | | | |
| Recommended voltage range | * | $V_{3;4;5\text{-}7}$ | 0 | – | 4 | V |
| Input bias current | * | $I_{3;4;5}$ | – | 10 | 100 | nA |
| **Indicator driver** | | | | | | |
| Output saturation voltages at $I_1$ = 20 mA; $V_{3\text{-}5}$ = 0 V | * | $V_{1\text{-}7sat}$ | – | 1,2 | 1,8 | V |
| at $I_2$ = 20 mA | * | $V_{2\text{-}7sat}$ | – | 0,5 | 1,0 | V |
| Output leakage current at $V_{1;2\text{-}7}$ = 24 V | * | $I_{1;2}$ | – | 20 | – | $\mu$A |

* $V_P$ = 8,5 or 15 V.

**CHARACTERISTICS** (continued)

| parameter | $V_P$ (V) | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **VCO** | | | | | | |
| Oscillator frequency adjustable with $R_{10\text{-}7}$ | * | $f_{osc}$ | – | 76 | – | kHz |
| Spread of free-running frequency at nominal external circuitry | * | $f_{osc}$ | 71 | – | 82 | kHz |
| Free-running frequency dependency (note 6) | | | | | | |
| with temperature | * | TC | – | $1 \times 10^{-4}$ | – | $K^{-1}$ |
| with supply voltage | * | $\Delta f_{osc}/\Delta V_P$ | – | – | 400 | Hz/V |
| Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\,nom}$ | * | $\Delta f/f$ | ± 2 | – | – | % |
| PLL control slope (total) | * | $S_{tot}$ | – | 4,5 | – | kHz/µs |
| D.C. voltage at pin 10 | * | $V_{10\text{-}7}$ | – | 2,1 | – | V |
| | | or: | – | $3{,}2\ V_{BE}$ | – | V |
| Frequency measuring point; internal switching threshold | * | $V_{4\text{-}7}$ | – | 6 | – | V |
| | | or: | – | $9\ V_{BE}$ | – | V |
| Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ | * | $V_{4\text{-}7(p\text{-}p)}$ | – | 350 | – | mV |
| Output resistance | * | $R_{4\text{-}7}$ | – | 5 | – | kΩ |

* $V_P$ = 8,5 or 15 V.

**Notes to the characteristics**

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with: 91% mono signal; $f_m$ = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz} \pm 23\ \text{kHz})}$$

measured with: 91% stereo signal; $f_m$ = 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 Hz, $f_m$ = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 4 kHz})};\ f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 4 kHz})};\ f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

measured with: 90% mono signal; $f_m$ = 1 kHz; 9% pilot signal;
1% spurious signal ($f_s$ = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 9 kHz})};\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with: 81% mono signal; $f_m$ = 1 kHz; 9% pilot signal;
10% SCA-subcarrier ($f_s$ = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q}$ = 28,6 mV at $T_j$ = 330 K.

6. The effects of external components are not taken into account.

## APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at pin 12 ($C_{12\text{-}7}$): phasing 19/38 kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation ($\alpha_2$); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

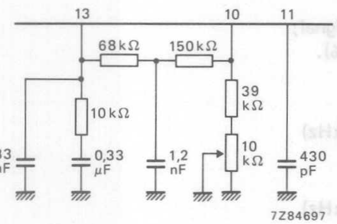



Fig. 2 PLL-filter for $\alpha_2$ = 70 dB at $V_P$ = 15 V (see also Fig. 1).

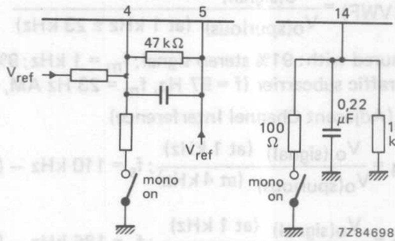



Fig. 3 (a) At pin 4; $-V_{4\text{-}5} > 300$ mV; (b) at pin 14.

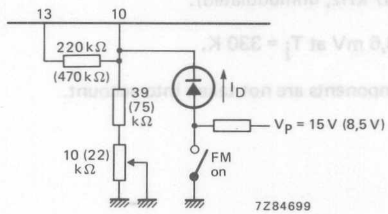



Fig. 4 The oscillator is switched-off when:
$I_D > 100\ \mu A$ ($> 50\ \mu A$ for $V_P$ = 8,5 V) and $I_D < 1$ mA.

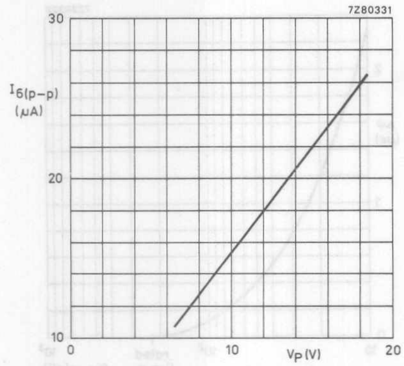



Fig. 5 Signal handling range at the input for $I_{6nom}$ (± 75 kHz); $V_{9\text{-}7} = V_P$.

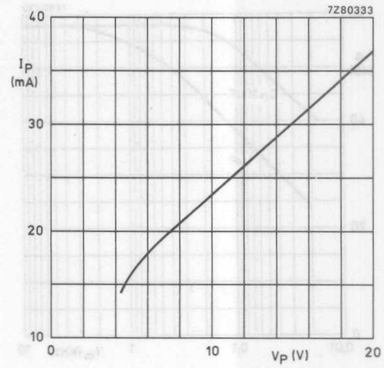



Fig. 6 Supply current comsumption at $V_{9\text{-}7} = V_P$.

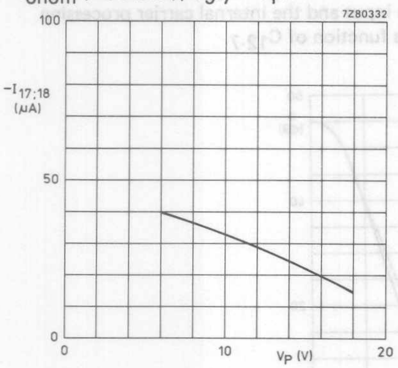



Fig. 7 D.C. current in the feedback loop of the output amplifier.

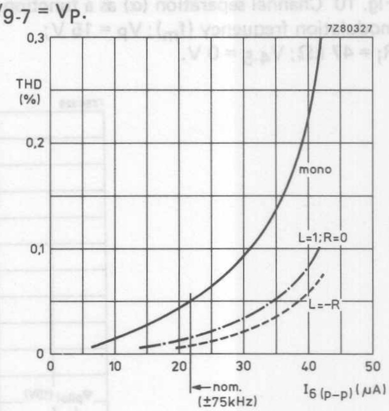



Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; $V_P = 15$ V; $f_m = 1$ kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V.

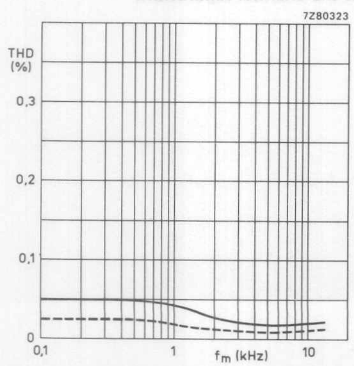



Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency ($f_m$); $V_P = 15$ V; $I_{6(p-p)} = 21{,}5$ μA.

——— mono

– – – – stereo; L = –R; 91% + 9% pilot signal.

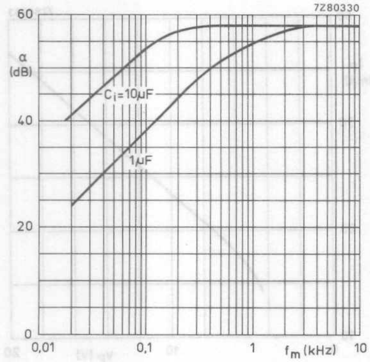



Fig. 10 Channel separation ($\alpha$) as a function of the modulation frequency ($f_m$); $V_P$ = 15 V; $R_i$ = 47 kΩ; $V_{4\text{-}5}$ = 0 V.

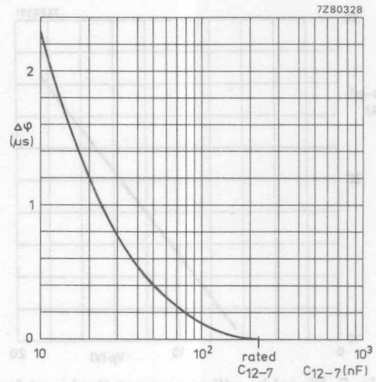



Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of $C_{12\text{-}7}$.

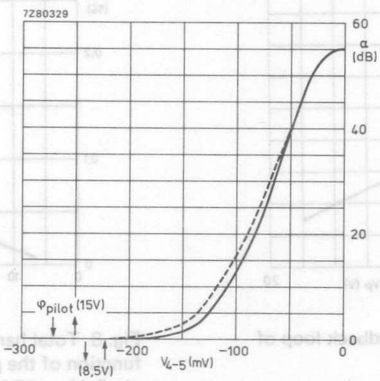



Fig. 12 Mono/stereo control at $f_m$ = 1 kHz; $\alpha$ is the channel separation.
——— $V_P$ = 8,5 V
– – – – $V_P$ = 15 V

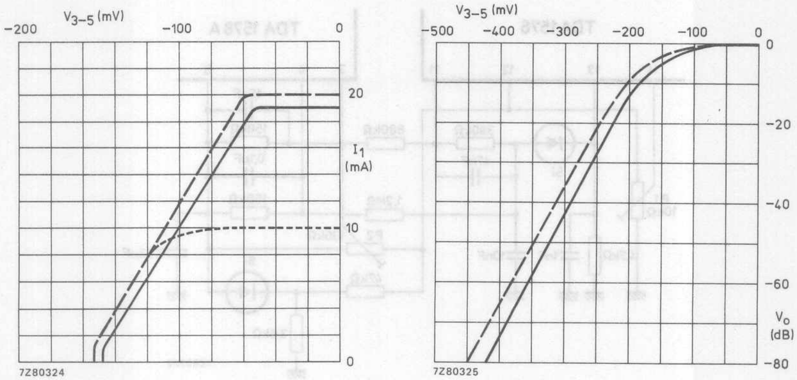



Fig. 13 Muting ($V_o$) and muting indicator current ($I_1$) as a function of $V_{3-5}$.
$V_o$ in dB curves; ——— $V_P$ = 8,5 V
– – – – $V_P$ = 15 V
$I_1$ in mA curves for $V_{PL}/R_{bias1}$ (pin 1); — — — 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - 10 V/680 Ω

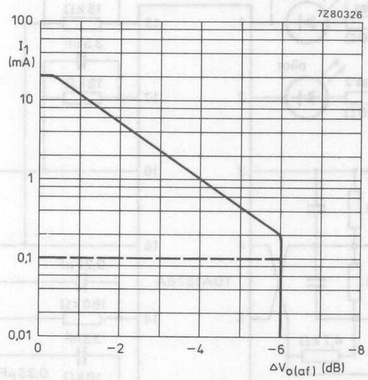



Fig. 14 Muting indicator current; $V_P$ = 8,5 to 15 V; $V_{PL}$ = 14 V.
——— $R_{bias1}$ = 680 Ω
– – – – $R_{bias1}$ = matched

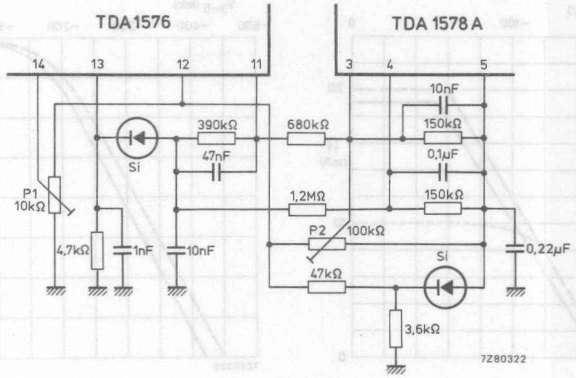



Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)} = 100\ \mu V$ with P1 to $\alpha = 6$ dB (channel separation),
at $V_{i(hf)} = 15\ \mu V$ with P2 to $V_{o(af)} = -3$ dB.

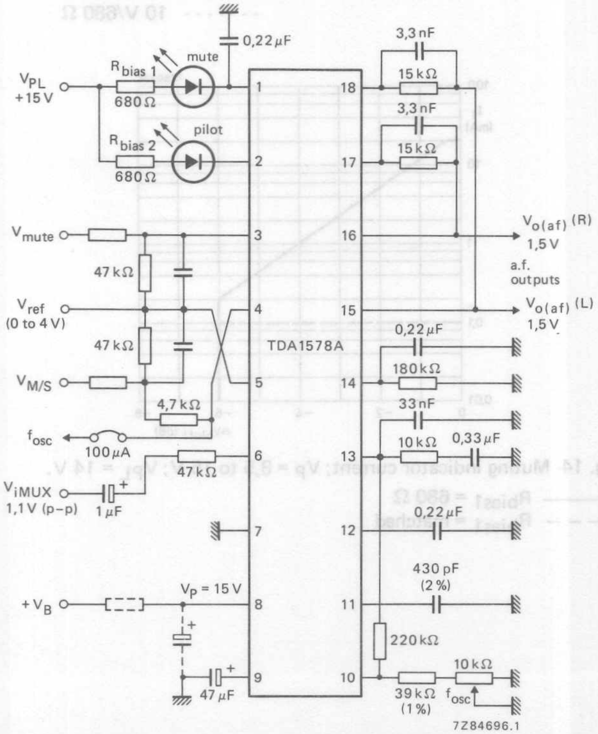



Fig. 16 Typical application circuit using TDA1578A for $V_P = 15$ V.

# TRAFFIC WARNING (VWF) DECODER CIRCUIT

The TDA1579 is intended for processing AM-modulated sub-carriers.

It incorporates the following functions:

- controllable selective sub-carrier amplifier (57 kHz)
- SK* decoder
- active BK/DK* filters
- BK/DK* decoder circuits (Schmitt trigger with switched hysteresis)
- BK/DK* threshold level switch for switch delay
- SK* indicator driver (LED)
- $\overline{SK}/\overline{DK}$* control outputs.

* SK: Senderkennung = Transmitter Identification Code
DK: Durchsagekennung = Announcement Identification Code
BK: Bereichskennung = Area Identification Code.
These terms are used in the West German traffic warning system (Verkehrs Warnfunk).

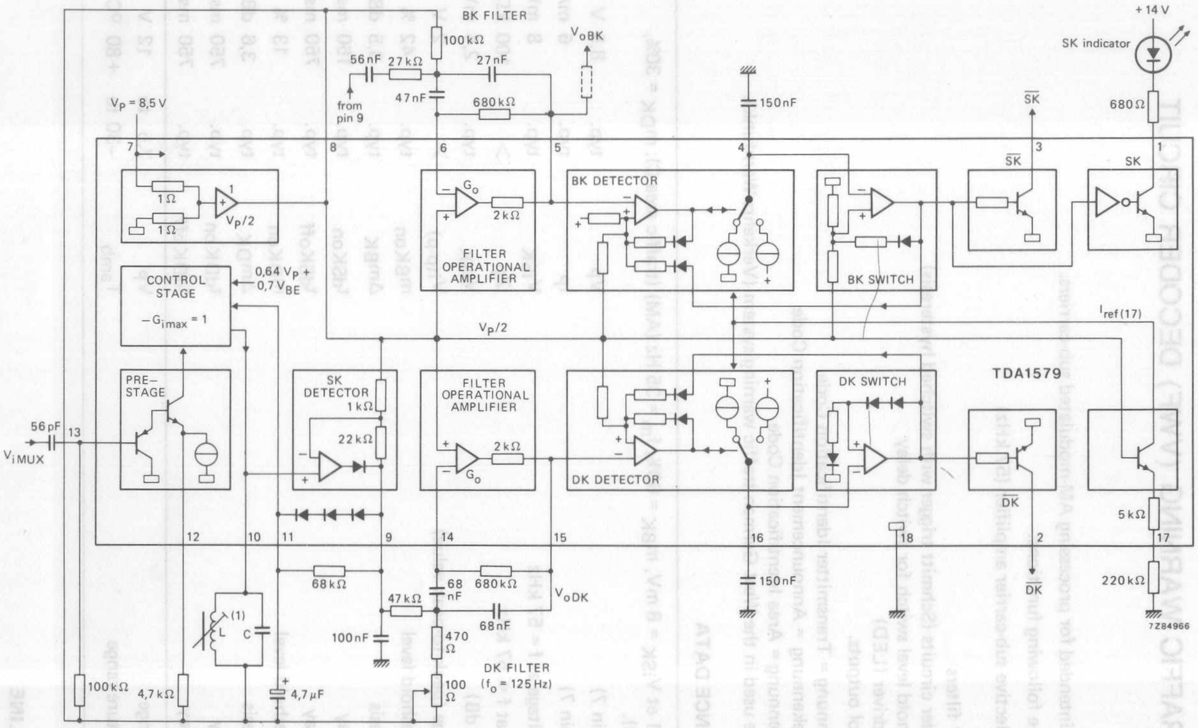
## QUICK REFERENCE DATA

Measured in Fig. 1 at $V_{iSK}$ = 8 mV, $m_{BK}$ = 60%, $f_m$ = 35 Hz (AM) (traffic area C); $m_{DK}$ = 30%, $f_m$ = 125 Hz (AM).

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 7) | $V_P$ | typ. | 8,5 | V |
| Supply current (pin 7) | $I_P$ | typ. | 6 | mA |
| Nominal input voltage at f = 57 kHz | $V_{iSK}$ | typ. | 8 | mV |
| Input impedance at f ⩽ 57 kHz | $\|Z_i\|$ | > | 100 | kΩ |
| Control level (–3 dB) | $V_{iSK}$ | typ. | 2,4 | mV |
| Input voltage range (peak-to-peak value) | $V_{i(p-p)}$ | ⩾ | 2 | V |
| SK switch-on threshold level | $m_{BKon}$ | typ. | 42 | % |
| SK switch hysteresis | $\Delta m_{BK}$ | typ. | 3,5 | dB |
| SK switch-on delay | $t_{dSKon}$ | typ. | 150 | ms |
| SK switch-off delay | $t_{dSKoff}$ | typ. | 750 | ms |
| DK switch-on threshold level | $m_{DKon}$ | typ. | 13 | % |
| DK switch hysteresis | $\Delta m_{DK}$ | typ. | 3,6 | dB |
| DK swith-on delay | $t_{dDKon}$ | typ. | 750 | ms |
| DK switch-off delay | $t_{dDKoff}$ | typ. | 750 | ms |
| Supply voltage range | $V_P$ | 7,5 to | 12 | V |
| Ambient temperature range | $T_{amb}$ | –30 to | +80 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).




(1) $L = 2,36$ mH; $Q_L = 70$; $C = 3,3$ nF; $f_o = 57$ Hz; 224 turns 0,1 enamelled copper.

Fig. 1 Circuit diagram of a SK(BK)/DK decoder using the TDA1579. It also includes a BK high-pass filter and a DK band-pass filter.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 7) | $V_P = V_{7\text{-}18}$ | max. | 18 V |
| Switch outputs (voltage and current) | | | |
| pin 1 | $V_{1\text{-}18}$ | max. | 23 V |
| | $I_1$ | max. | 50 mA |
| pins 2 and 3 | $V_{2;3\text{-}18}$ | max. | 18 V |
| | $I_{2;3}$ | max. | 5 mA |
| negative voltage at pins 1, 2 and 3 | $-V_{1;2;3\text{-}18}$ | max. | 0,5 V |
| or: negative current at pins 1, 2 and 3 | $-I_{1;2;3}$ | max. | 10 mA |
| Signal input (voltage and current) | | | |
| pin 13 | $V_{13\text{-}18}$ | max. | $V_P$ |
| negative voltage at pin 13 | $-V_{13\text{-}18}$ | max. | 0,5 V |
| or: negative current at pin 13 | $-I_{13}$ | max. | 10 mA |
| Total power dissipation | $P_{tot}$ | max. | 800 mW |
| Storage temperature range | $T_{stg}$ | −55 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | −30 to +80 | °C |

## CHARACTERISTICS

$V_P$ = 8,5 V; $T_{amb}$ = 25 °C; measured at nominal input signal: $V_{iSK}$ = 8 mV, f = 57 kHz, amplitude modulated with $f_m$ = 34,95 Hz, m = 0,6 (for BK, traffic area C), $f_m$ = 125 Hz, m = 0,3 (for DK); unless otherwise specified.

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 7) | $V_P$ | | 7,5 to 12 | V |
| Supply current (pin 7) | $I_P$ | typ. | 6 | mA |
| | | < | 10 | mA |
| **SK amplifier/decoder** | | | | |
| Input impedance; f ≤ 57 kHz | $\lvert Z_i \rvert$ | > | 100 | kΩ |
| Input voltage range (peak-to-peak value) | $V_{i(p\text{-}p)}$ | > | 2 | V |
| Input voltage at start of control $V_{o9BK}$ = −3 dB | $V_{iSK}$ | typ. | 2,4 | mV* |
| Voltage gain; $V_{9BK}/V_{13SK}$ | $G_{v9\text{-}13}$ | typ. | 44 | dB* |
| Spread in gain | $\pm\Delta G_{v9\text{-}13}$ | < | 2 | dB |
| Gain control range | $\Delta G_v$ | > | 40 | dB |
| Output voltage; controlled | $V_{o9BK}$ | typ. | 440 | mV |
| | $V_{o9DK}$ | typ. | 220 | mV |
| **BK circuit** | | | | |
| Switch-on threshold level; pin 3 blocked | $V_{o5BKon}$ | typ. | 670 | mV |
| | | | 600 to 750 | mV |
| Switch hysteresis | $\frac{V_{o5BKon}}{V_{o5BKoff}}$ | typ. | 3,5 | dB |
| | | | 3 to 4 | dB |
| BK switch threshold level for BK (SK) off; pin 3 conducting | $V_{4\text{-}18off}$ | typ. | 0,88 | V |
| | | | 0,8 to 0,97 | V |
| | or: | typ. | $0{,}21V_{8\text{-}18}$ | |
| Switch output (pin 3) | | | | |
| allowable load current | $I_3$ | < | 1,5 | mA |
| saturation voltage at $I_3$ = 1,5 mA | $V_{3\text{-}18sat}$ | < | 0,35 | V |
| rejection voltage at $I_3$ < 5 μA | $V_{3\text{-}18}$ | > | 18 | V |
| Indicator driver (pin 1) | | | | |
| allowable load current | $I_1$ | < | 40 | mA |
| saturation voltage at $I_1$ = 20 mA | $V_{1\text{-}18sat}$ | < | 0,8 | V |
| rejection voltage at $I_1$ < 10 μA | $V_{1\text{-}18}$ | > | 23 | V |

* Selectable by $R_{12\text{-}8}$ or $Z_{10\text{-}8}$.

**DK-circuit**

| | | | |
|---|---|---|---|
| Switched-on threshold level; pin 2 blocked | $V_{15\,DK\,on}$ | typ. | 670 mV |
| | | | 600 to 750 mV |
| Switch hysteresis | $\frac{V_{15\,DK\,on}}{V_{15\,DK\,off}}$ | typ. | 3,6 dB |
| | | | 3,1 to 4,1 dB |
| DK switch threshold level (Schmitt trigger) for DK off; pin 2 conducting | $V_{16\text{-}18\,off}$ | typ. | 0,6 V |
| | or: | typ. | $1 \cdot V_{BE}$ |
| Switch output (pin 2) | | | |
| allowable load current | $I_2$ | < | 1,5 mA |
| saturation voltage at $I_2$ = 1,5 mA | $V_{2\text{-}18sat}$ | < | 0,35 V |
| rejection voltage at $I_2 < 5\ \mu A$ | $V_{2\text{-}18}$ | > | 18 V |

**BK and DK filter amplifiers**

| | | | |
|---|---|---|---|
| Gain (open circuit) at f = 100 Hz | $G_o$ | > | 84 dB |
| Current gain | $G_i$ | > | 120 dB |
| Input bias current | $\pm I_i$ | < | 50 mA |
| Output offset voltage at $R_{5\text{-}6} = R_{14\text{-}15}$ = 680 kΩ | $\pm V_{o5\text{-}8;\,15\text{-}8}$ | < | 50 mV |
| Available output current | $\pm I_o$ | > | 1 mA |
| Output resistance | $R_o$ | typ. | 2 kΩ |
| | | < | 3,5 kΩ |
| Allowable load capacitance | $C_L$ | < | 50 pF |

**Internal reference voltage**

| | | | |
|---|---|---|---|
| Output voltage | $V_{8\text{-}18}$ | typ. | 4,25 V |
| | | | 4,0 to 4,5 V |
| | or: | typ. | $0,5 \cdot V_P$ |
| Internal resistor of voltage source | $R_8$ | < | 5 Ω |
| Available output current | $-I_8$ | > | 2 mA |
| | $+I_8$ | > | 0,6 mA |
| Output short-circuit current | $-I_{8sc}$ | typ. | 8 mA |
| | or: | typ. | $V_P$/1 kΩ |

**Reference current source**

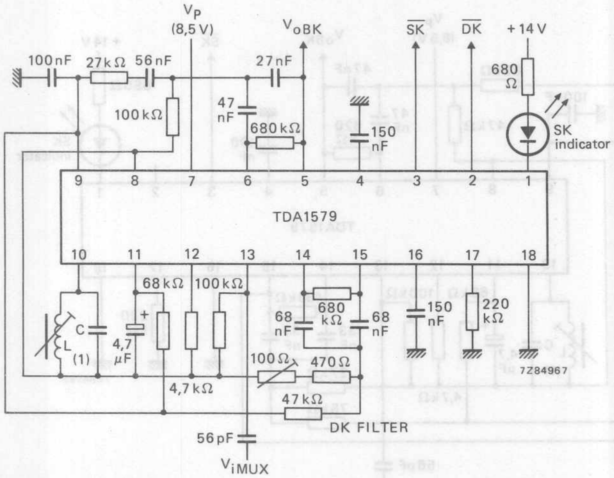
| | | | |
|---|---|---|---|
| Reference voltage | $V_{17\text{-}18}$ | typ. | 3,6 V |
| | or: | typ. | $V_{8\text{-}18} - V_{BE}$ |
| Internal biasing resistor | $R_{i17}$ | typ. | 5 kΩ |
| Allowable range of external reference resistor | $R_{17\text{-}18}$ | | 180 to 270 kΩ |

## APPLICATION INFORMATION (Figs 2, 3 and 4)

| | | | Fig. 2 | Fig. 3 | Fig. 4 | |
|---|---|---|---|---|---|---|
| SK switch-on threshold level | | | | | | |
| at $m_{BK} = 0,6$ | $V_{iSK\,on}$ | typ. | 2,5 | 1,8 | 1,8 | mV |
| at $V_{iSK} = 8$ mV | $m_{BK\,on}$ | typ. | 0,42 | 0,32 | 0,32 | |
| SK switch hysteresis | $\frac{m_{BK\,on}}{m_{BK\,off}}$ | > | 3,0 | 3,0 | 3,0 | dB |
| | | typ. | 3,5 | 3,5 | 3,5 | dB |
| | | < | 4,0 | 4,0 | 4,0 | dB |
| SK switch-on delay (note 1) | $t_{dSK\,on}$ | typ. | 150 | 95 | 95 | ms |
| | | < | – | 130 | 130 | ms |
| SK switch-off delay (note 2) | $t_{dSK\,off}$ | > | – | 380 | 380 | ms |
| | | typ. | 750 | 500 | 500 | ms |
| | | < | – | 620 | 620 | ms |
| DK switch-on threshold level | | | | | | |
| at $m_{DK} = 0,3$ | $V_{iSK\,on}$ | typ. | 1,5 | 1,5 | – | mV |
| at $V_{iSK} = 8$ mV | $m_{DK\,on}$ | typ. | 0,13 | 0,13 | – | |
| DK switch hysteresis | $\frac{m_{DK\,on}}{m_{DK\,off}}$ | > | 3,1 | 3,1 | – | dB |
| | | typ. | 3,6 | 3,6 | – | dB |
| | | < | 4,1 | 4,1 | – | dB |
| DK switch-on delay (note 1) | $t_{dDK\,on}$ | typ. | 750 | 750 | – | ms |
| | | < | 1000 | 1000 | – | ms |
| DK switch-off delay (note 2) | $t_{dDK\,off}$ | > | 600 | 600 | – | ms |
| | | typ. | 750 | 750 | – | ms |
| | | < | 1000 | 1000 | – | ms |

Notes

1. Measuring conditions for switch-on delay ($t_{d\,on}$).
   Pin 4 (16) is connected to ground via a switch. The circuit is in a transient state. The switch at pin 4 (16) is opened at the zero-crossing of the positive-going $V_{oBK}$ ($V_{oDK}$) signal. The time between opening the switches and the positive switching-edge of the output signal at pin 3 (2) is defined as the switch-on delay $t_{d\,on}$.
2. Measuring conditions for switch-off delay ($t_{d\,off}$).
   After finishing the measurement of $t_{d\,on}$, the SK-input signal is switched off at the zero-crossing of the negative-going $V_{oBK}$ ($V_{oDK}$) signal (pins 11 and 8 are not short-circuited). The time between the input switching-off and the negative switching-edge of the output signal at pin 3 (2) is defined as the switch-off delay $t_{d\,off}$.




(1) L = 2,56 mH; $Q_L$ = 70; C = 3,3 nF.

Fig. 2 Typical application circuit using TDA1579. It includes SK(BK) and DK decoder with BK high-pass filter and DK band-pass filter.

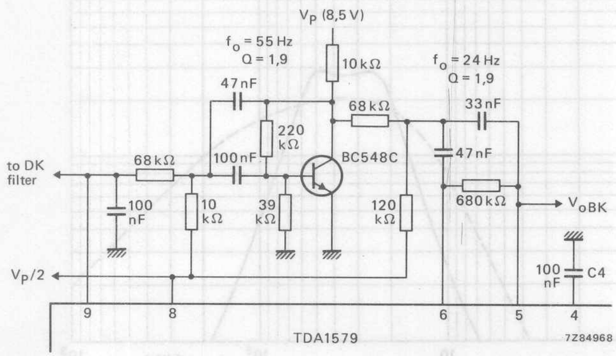



Fig. 3 Typical application circuit using TDA1579 for SK(BK) and DK decoder with BK band-pass filter and DK band-pass filter; for further circuitry see Fig. 2.

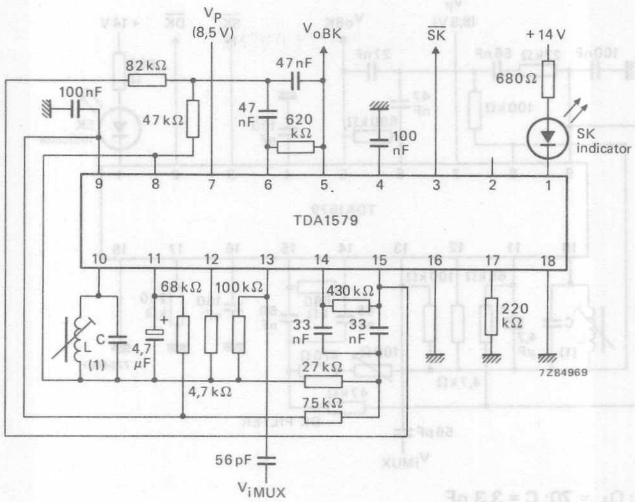



Fig. 4 Typical application circuit using TDA1579 for SK(BK) decoder with BK band-pass filter.

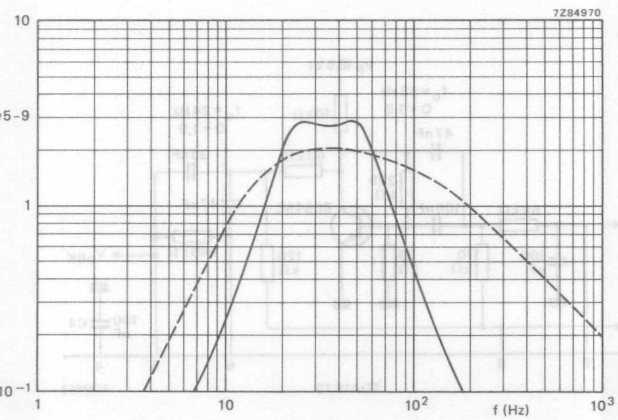



Fig. 5 Voltage gain between pins 5 and 9 as a function of frequency; BK selection.
——— band-pass circuits (Figs 3 and 4); – – – high-pass circuits (Figs 1 and 2).

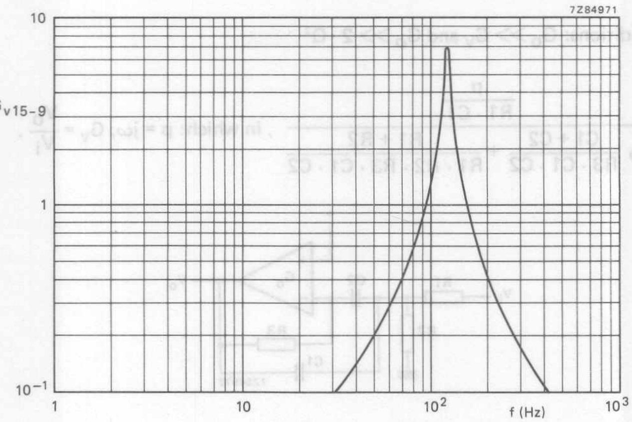



Fig. 6 Voltage gain between pins 15 and 19 as a function of frequency; DK selection; $f_o = 125$ Hz; $Q \approx 18$.

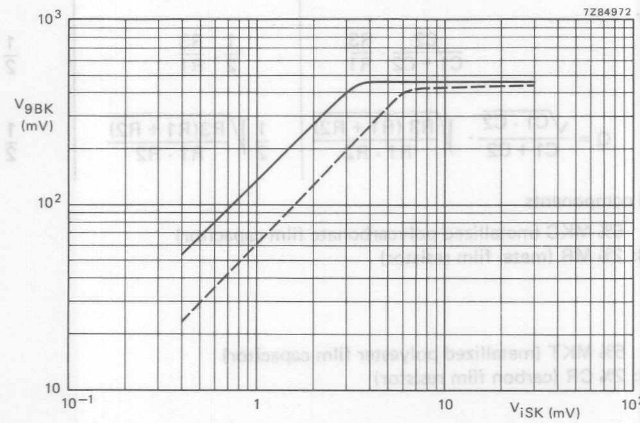
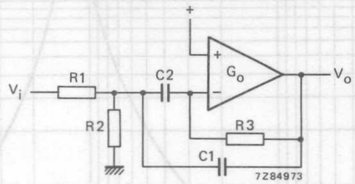



Fig. 7 Control characteristic of the SK amplifier at $V_P = 8{,}5$ V; $m_{BK} = 60\%$ and $Q_L = 70$.

## GENERAL FILTER CALCULATIONS

1. Gain
   Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = -\frac{\frac{p}{R1 \cdot C1}}{p^2 + p\frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}, \text{ in which: } p = j\omega;\ G_v = \frac{V_o}{V_i}.$$




| | general | C1 = C2 = C | C1 = C2 = C<br>R2 << R1 |
|---|---|---|---|
| 2. Resonance frequency $\omega_r =$ | $\frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$ | $\frac{1}{C\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3}}$ | $\frac{1}{C\sqrt{R2 \cdot R3}}$ |
| 3. Gain at $\omega = \omega_r$ $-G_{vr} =$ | $\frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$ | $\frac{1}{2} \cdot \frac{R3}{R1}$ | $\frac{1}{2} \cdot \frac{R3}{R1}$ |
| 4. Quality | $Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$ | $\frac{1}{2}\sqrt{\frac{R3(R1 + R2)}{R1 \cdot R2}}$ | $\frac{1}{2} \cdot \frac{R3}{R2}$ |

5. Recommended components
   C1 and C2: 5% MKC (metallized polycarbonate film capacitor)
   R1, R2 and R3: 2% MR (metal film resistor)

   or:

   C1 and C2: 5% MKT (metallized polyester film capacitor)
   R1, R2 and R3: 2% CR (carbon film resistor)

# TRAFFIC CONTROL MESSAGES AND WARNING TONE CIRCUIT

The TDA1589 is for evaluation of operating signals and logic control signals of a traffic control (TC) message decoder.

**Features**

- mute of non-traffic control stations
- restriction to traffic-control message reception
- LED display driver for MUTE indication
- control output for TC messages minimum volume
- delayed start of warning tone signal on failure of TC transmission. Also to be used to control a start of search tuning
- warning tone generator with automatic level control increasing volume in five steps
- interruption of cassette playback with motor stop during TC messages
- warning tone indicating failure of TC transmission also during cassette playback

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 10) | $V_P$ | | 7,5 to 16 | V |
| | | typ. | 8,5 | V |
| Supply current | $I_P$ | typ. | 4,5 | mA |
| Warning tone maximum voltage | $V_{o(p-p)}$ | typ. | 4,3 | V |
| Output LED driver current (pin 3) | $I_3$ | typ. | 30 | mA |
| motor stop current (pin 5) | $I_5$ | typ. | 30 | mA |
| motor stop current (pin 6) | $I_6$ | typ. | 2 | mA |
| MUTE display current (pin 8) | $I_8$ | typ. | 2 | mA |
| start warning tone current (pin 13) | $I_{13}$ | typ. | 2 | mA |
| Saturation voltage at output for minimum volume-on (pin 7) | $V_{7\,sat}$ | < | 0,1 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

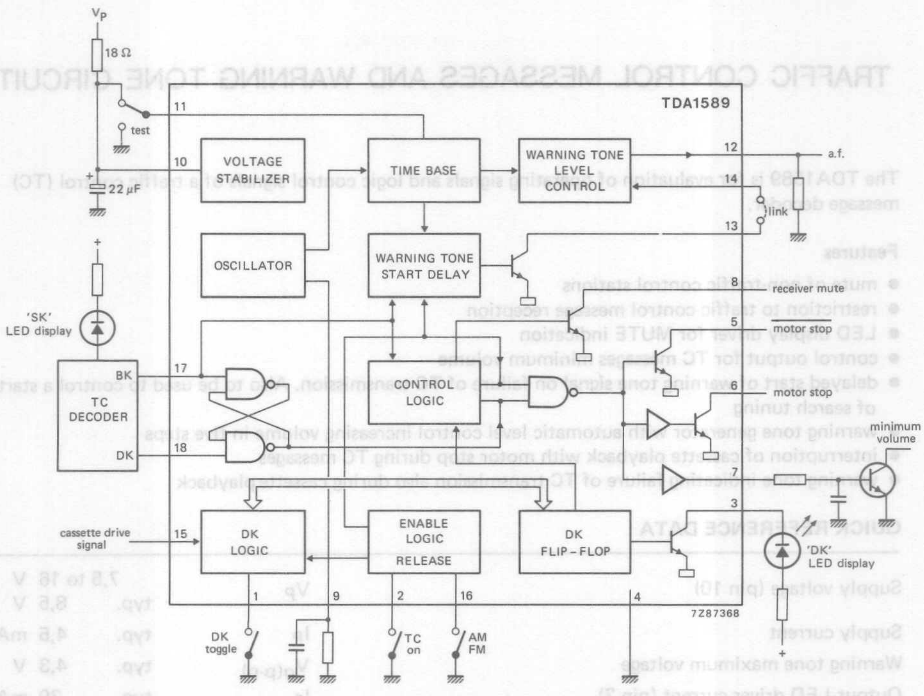
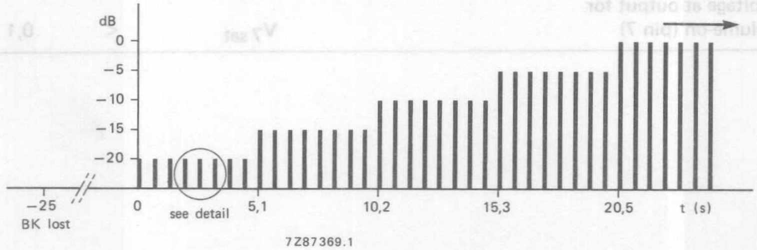



Fig. 1 Block diagram with external components; used as test circuit.

BK = TC area identification code (BereichsKennung)
DK = TC message identification code (DurchsageKennung)
SK = TC station identification code (SenderKennung)



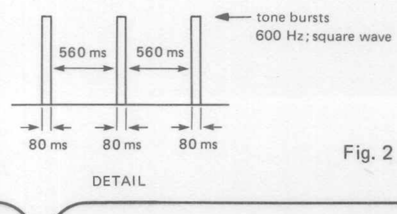




Fig. 2 Intermittent step pulse warning signal.

## FUNCTIONAL DESCRIPTION

The automatic evaluation of traffic control signals is only possible during FM reception. The enable circuit will be active when pin 16 (FM on) is LOW. If traffic control messages are desired, pin 2 (TC on) must be switched to LOW.

### FM radio mode

By operating the DK-toggle switch at pin 1 the DK flip-flop is set. This is displayed by a LED connected to pin 3. In the position "TC off" (pin 2 HIGH) it is not possible to set the DK flip-flop. Non-traffic control stations are muted. If a message is transmitted on the tuned TC station the minimum volume at pin 7 is exposed.

In case of BK-signal failure pin 13 changes to LOW after a delay of about 25 seconds. If pins 13 and 14 are then connected, an intermittent warning signal will be supplied at pin 12. The level increases automatically from −20 dB to 0 dB in 5 steps. (See Fig. 2.)

### Cassette mode

If a TC message is delivered when TC is switched on (pin 16 and pin 2 LOW) and the DK flip-flop is set, the motor of the cassette player is stopped and the receiver automatically cuts in. The minimum volume is also set at the same time.

In case of BK-signal failure, the warning tone will be mixed into the cassette playback.

### Protection

To avoid faulty switching, an internal latch will be set only if both DK (pin 18) and BK (pin 17) are HIGH. The latch will be reset if DK is changed to LOW independent of BK.

Reset of the DK-toggle flip-flop:
- by operating the DK-toggle (pin 1) twice
- by opening the TC-switch (pin 2)
- by switching to AM reception (pin 16)
- by switching off the cassette-player (pin 15)
- by switching power off or on.

### Transmission monitoring

At reception failure of a TC-station BK at pin 17 will become LOW. After about 25 seconds the output (pin 13) will be set LOW to start the warning signal via the jumper between pins 13 and 14. In the meantime the search-tuning can also be started. The warning tone stage gives a graduated signal with a level increasing in five steps from −20 dB to 0 dB in about 20 seconds. The frequency of the warning signal is about 600 Hz; tone period ≈ 80 ms; pause ≈ 560 ms.

If now another TC-message transmitter has been tuned the input BK (pin 17) becomes HIGH and the warning tone is stopped. Also when switching TC-off (pin 2 HIGH) or switching to AM reception (pin 16 HIGH) the warning tone will stop. The BK-signal has to be stable for more than 1 second to reset the just started 25-second-timer.

| mode | inputs pin numbers | | | | | | outputs pin numbers | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 16 | 2 | 15 | 1 | 17 | 18 | 7 | 5 | 6 | 8 | 13 | 3 |
| → AM RADIO | H | X | X | X | X | X | H | H | L | H | H | H |
| FM RADIO TC off | L | H | X | X | X | X | H | H | L | H | H | H |
| → FM-TC on station without TC | L | L | X | X | L | X | L | L | H | L | L* | L |
| FM-TC on station with BK | L | L | X | H | H | L | H | H | L | H | H | H |
| FM-TC on station with BK, DK | L | L | X | H | H | H | L | L | H | H | H | H |
| FM-TC on station with BK DK-toggle operated MUTE | L | L | X | H | L | H | H | L | L | H | ‾╲_ |
| FM-TC on station with BK, DK incoming message | L | L | X | H | H | _╱‾ | ‾╲_ | ‾╲_ | _╱‾ | _╱‾ | H | L |
| FM-TC on station with BK DK-toggle operated twice | L | L | X | ‾╲_╱‾╲_╱‾ | H | L | H | H | L | ‾╲_╱‾ | H | ‾╲_╱‾ |
| FM-TC on and cassette station with BK, DK cassette switched on | L | L | _╱‾ | X | H | H | L | L | H | H | H | H |
| FM-TC on and cassette station with BK cassette switched on | L | L | _╱‾ | X | H | L | H | H | L | H | H | H |
| FM-TC on and cassette station with BK cassette switched off | L | L | ‾╲_ | X | H | L | H | H | L | _╱‾ | H | _╱‾ |
| → function and state | AM/FM HIGH/LOW | TC on on = LOW | cassette off = H→L | DK toggle active = LOW | BK on = HIGH | DK on = HIGH | min. volume on = LOW | motor stop stop = LOW | motor stop stop = HIGH | MUTE on = LOW | warning tone on = LOW | DK display on = LOW |

* After about 25 seconds.

Positive logic:
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
_╱‾ = positive-going transition
‾╲_ = negative-going transition

**Functions of the control inputs**

| | | | |
|---|---|---|---|
| DK toggle operated<br>chatter-proof by internal delay<br>of 10 to 20 ms | pin 1 | active | = LOW |
| TC (traffic control) released | pin 2 | on | = LOW |
| Test condition<br>clock rate 24 times faster | pin 11 | on<br>off | = to ground<br>= to $V_P$ or open |
| Start warning signal | pin 14 | on | = LOW |
| Reset of DK flip-flop<br>by cassette player | pin 15 | reset | = HIGH to LOW transition |
| Reset of DK flip-flop<br>by tuning AM band | pin 16 | reset | = HIGH |
| BK input* | pin 17 | on | = HIGH |
| DK input* | pin 18 | on | = HIGH |
| Minimum volume | pin 7 | on | = LOW |
| Motor stop (30 mA) | pin 5 | stop | = LOW |
| Motor stop (2 mA) | pin 6 | stop | = HIGH |
| MUTE (volume off) | pin 8 | on | = LOW |
| Warning tone | pin 13 | on | = LOW |
| DK display | pin 3 | on | = LOW |

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 10) | $V_P$ | max. | 16 V |
| Input voltages<br>pins 1, 2, 11, 14, 15, 16, 17 and 18 | $V_i$ | | 0 to $V_P$ V |
| Output voltages<br>pins 3, 5, 6, 8, 13 | $V_o$ | max. | 23 V |
| Currents<br>inputs 1, 2, 11, 14, 15, 16, 17 and 18 | $I_i$ | max. | 10 mA |
| outputs 6, 8, 13 | $I_o$ | max. | 10 mA |
| outputs 3 and 5 | $I_o$ | max. | 50 mA |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 °C |

* Open collector output of TC-decoder.

## CHARACTERISTICS

$V_P$ typ. 8,5 V; $T_{amb}$ = 25 °C; unless otherwise specified (see Fig. 1)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_P$ | | 7,5 to 16 V |
| Supply current | $I_P$ | typ. | 4,5 mA |
| | | < | 6 mA |
| **Control inputs** | | | |
| Pins 1, 2, 11, 14, 15, 16, 17 and 18 | | | |
| Input voltage HIGH | $V_{IH}$ | | 3,5 V to $V_P$ |
| Input voltage LOW | $V_{IL}$ | < | 2 V |
| Input current HIGH $V_i$ = 16 V | $I_{IH}$ | < | 1 μA |
| Input current LOW $V_i$ = 0 V | $-I_{IL}$ | | 25 to 200 μA |
| Input resistance $V_i$ = 0 V | $R_i$ | < | 10 kΩ |
| **Control outputs** | | | |
| DK-LED display and $\overline{\text{motor stop}}$ open collector outputs 3 and 5 | | | |
| Output voltage LOW $I_{OL}$ = 20 mA | $V_{OL}$ | typ. | 1 V |
| | | < | 1,5 V |
| Output current LOW | $I_{OL}$ | typ. | 30 mA |
| Output voltage HIGH (open collector) $I_{OH}$ < 10 μA | $V_{OH}$ | < | 23 V |
| LF-MUTE, motor stop and warning signal start pins 8, 6 and 13 | | | |
| Output voltage LOW $I_{OL}$ = 1 mA | $V_{OL}$ | < | 0,35 V |
| Output current LOW | $I_{OL}$ | = | 2 mA |
| Output voltage HIGH (open collector) $I_{OH}$ < 1 μA | $V_{OH}$ | = | 16 V |
| Minimum voltage (pin 7) ($R_S$ = 800 Ω, $R_L$ = ∞) | | | |
| Output voltage LOW (for volume HIGH) | $V_{7-4}$ | < | 0,1 V |
| Output voltage HIGH (for volume LOW) | $V_{7-4}$ | typ. | 5 V |
| **Warning signal** (pin 12) | | | |
| f = 600 Hz; square-wave pulsed; $R_S$ = 300 Ω | | | |
| Switching time on | $t_{on}$ | typ. | 80 ms |
| Switching time off | $t_{ogf}$ | typ. | 560 ms |
| Output voltage during $t_{on}$ at maximum peak ($R_L$ = 1 kΩ) | $V_{12-4}$ | typ. | 4,3 V |
| during $T_{off}$ | $V_{12-4}$ | typ. | 0 V |

| | | | | |
|---|---|---|---|---|
| **Automatic level control** | | | | |
| Duration per level | $t_p$ | typ. | 5 | s |
| Output level swing (in 5 steps) | $\Delta V_{12\text{-}4}$ | | −20 to 0 | dB |
| Output current peak value | $-I_{12M}$ | typ. | 6 | mA |
| **Oscillator** (pin 9) | | | | |
| Frequency | f | typ. | 2400 | Hz |
| Filter resistance | $R_o$ | typ. | 100 | kΩ |
| Filter capacitance | $C_o$ | typ. | 4,7 | nF |
| Oscillator frequency tolerance | $\Delta f/f$ | | −10 to + 10 | % |

# 5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 35 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 1,5 | A |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 18 V; $R_L$ = 8 Ω | $P_o$ | typ. | 4,5 | W |
| $V_P$ = 25 V; $R_L$ = 15 Ω | $P_o$ | typ. | 5 | W |
| Total harmonic distortion at $P_o$ < 2 W; $R_L$ = 8 Ω | $d_{tot}$ | typ. | 0,3 | % |
| Input impedance | $\|Z_i\|$ | typ. | 45 | kΩ |
| Total quiescent current at $V_P$ = 18 V | $I_{tot}$ | typ. | 25 | mA |
| Sensitivity for $P_o$ = 2,5 W; $R_L$ = 8 Ω | $V_i$ | typ. | 55 | mV |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

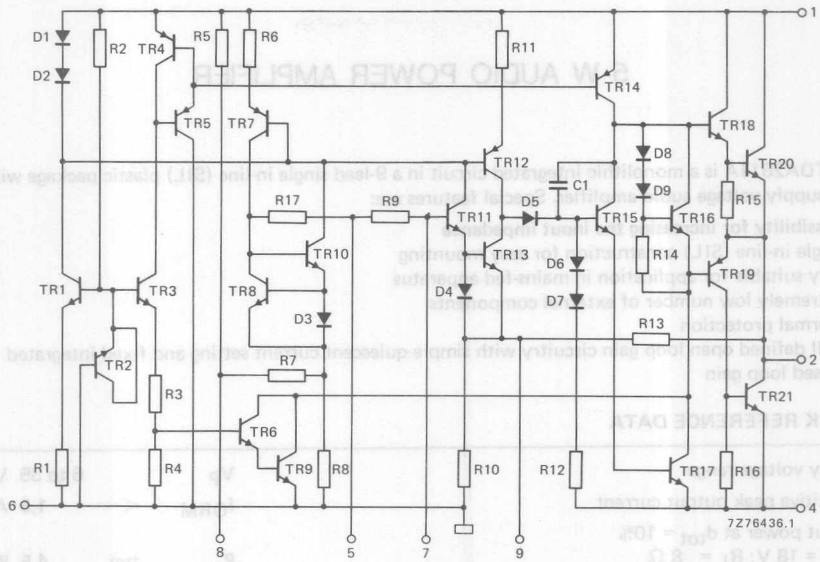



Fig. 1 Circuit diagram; pin 3 not connected.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 35 V |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 3 A |
| Repetitive peak output current | $I_{ORM}$ | max. | 1,5 A |
| Total power dissipation | see derating curves Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |

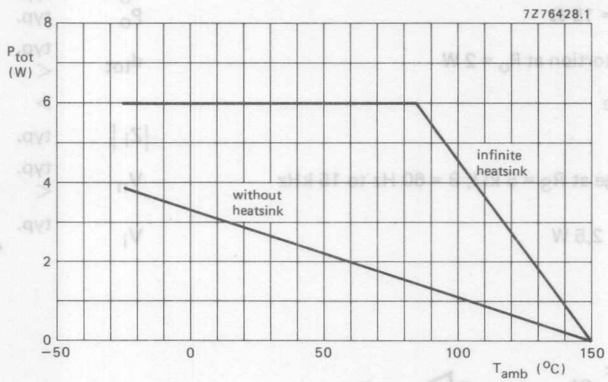



Fig. 2 Power derating curves.

## HEATSINK EXAMPLE

Assume $V_P$ = 18 V; $R_L$ = 8 Ω; $T_{amb}$ = 60 °C maximum; $T_j$ = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{2{,}2} = 41\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab}$ = 11 K/W and $R_{th\,tab\text{-}h}$ = 1 K/W, $R_{th\,h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

**D.C. CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 35 V |
| Repetitive peak output current | $I_{ORM}$ | < | 1,5 A |
| Total quiescent current at $V_P$ = 18 V | $I_{tot}$ | typ. | 25 mA |

**A.C. CHARACTERISTICS**

$T_{amb}$ = 25 °C; $V_P$ = 18 V; $R_L$ = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

| | | | |
|---|---|---|---|
| A.F. output power at $d_{tot}$ = 10% | | | |
| $V_P$ = 18 V; $R_L$ = 8 Ω | $P_o$ | > | 4 W |
| | | typ. | 4,5 W |
| $V_P$ = 12 V; $R_L$ = 8 Ω | $P_o$ | typ. | 1,7 W |
| $V_P$ = 8,3 V; $R_L$ = 8 Ω | $P_o$ | typ. | 0,65 W |
| $V_P$ = 20 V; $R_L$ = 8 Ω | $P_o$ | typ. | 6 W |
| $V_P$ = 25 V; $R_L$ = 15 Ω | $P_o$ | typ. | 5 W |
| Total harmonic distortion at $P_o$ = 2 W | $d_{tot}$ | typ. | 0,3 % |
| | | < | 1 % |
| Frequency response | | > | 15 kHz |
| Input impedance | $\|Z_i\|$ | typ. | 45 kΩ * |
| Noise output voltage at $R_S$ = 5 kΩ; B = 60 Hz to 15 kHz | $V_n$ | typ. | 0,2 mV |
| | | < | 0,5 mV |
| Sensitivity for $P_o$ = 2,5 W | $V_i$ | typ. | 55 mV |
| | | | 44 to 66 mV |

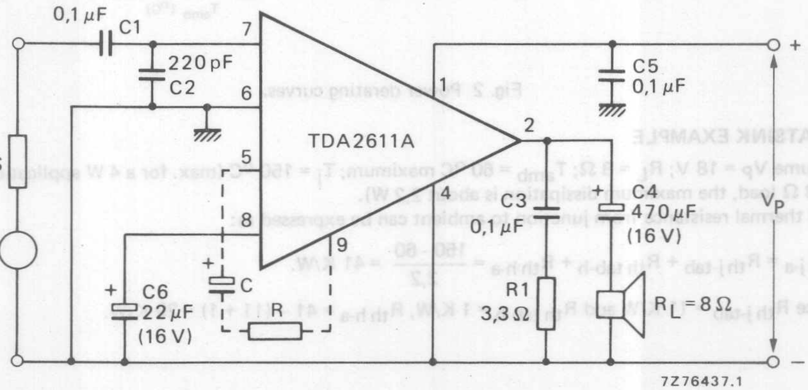



Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

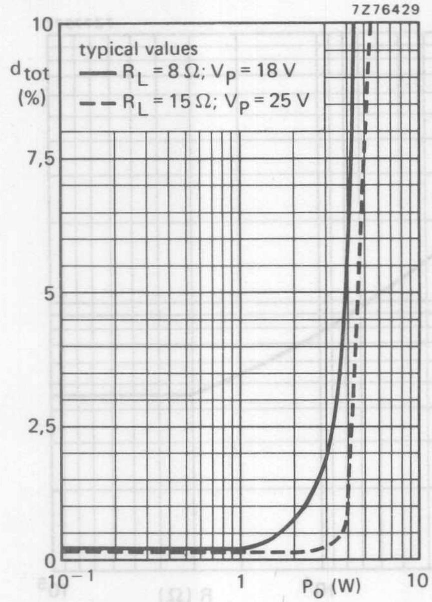



Fig. 4 Total harmonic distortion as a function of output power.

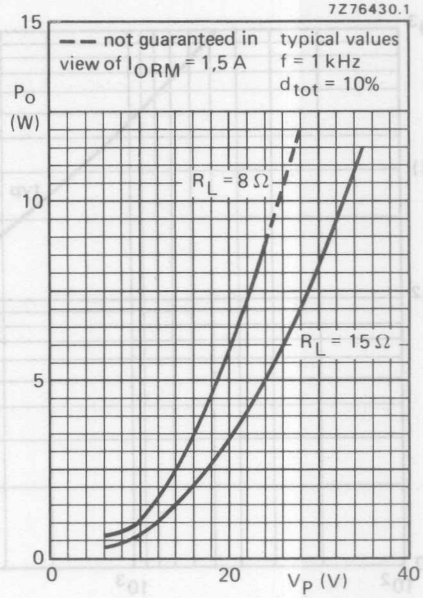



Fig. 5 Output power as a function of supply voltage.

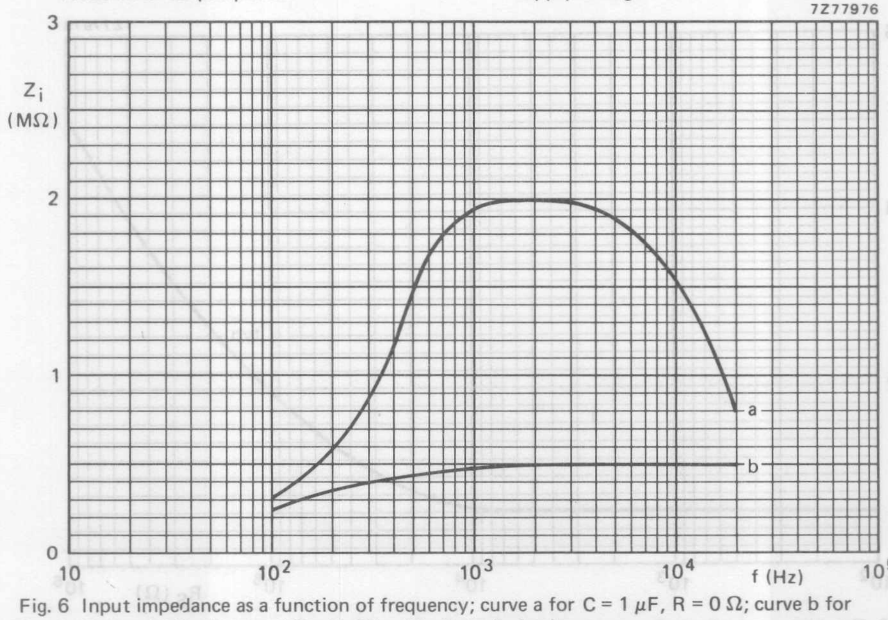



Fig. 6 Input impedance as a function of frequency; curve a for C = 1 $\mu$F, R = 0 Ω; curve b for C = 1 $\mu$F, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

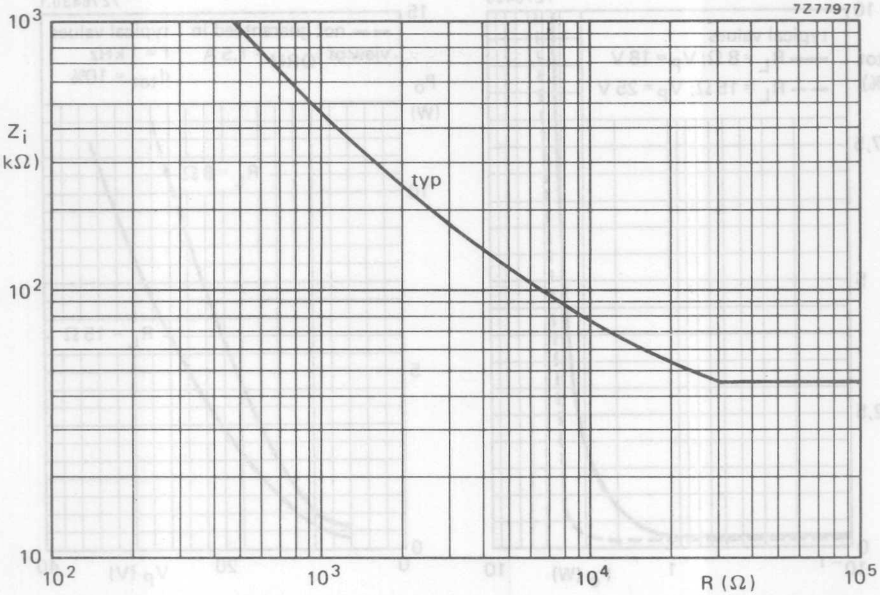



Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

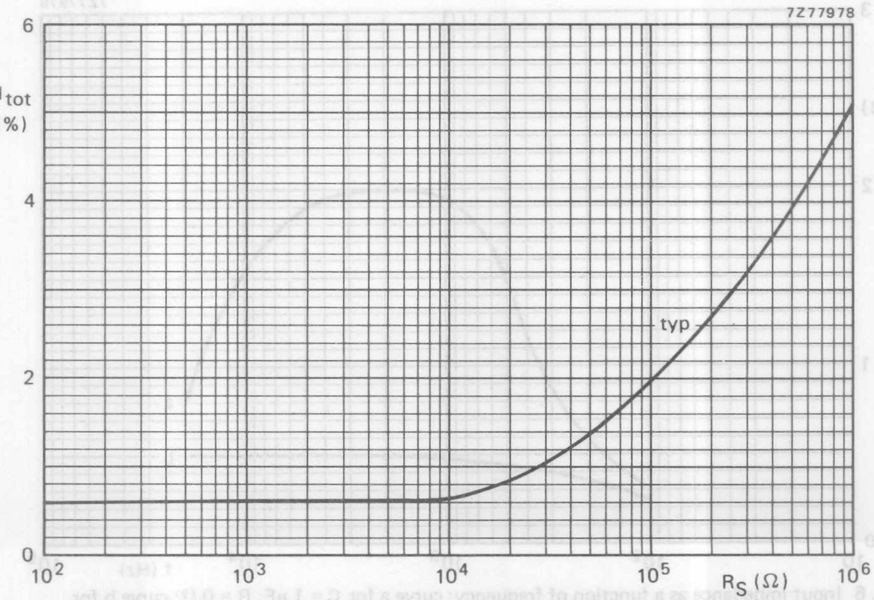



Fig. 8 Total harmonic distortion as a function of $R_S$ in the circuit of Fig. 3; $P_o$ = 3,5 W; f = 1 kHz.

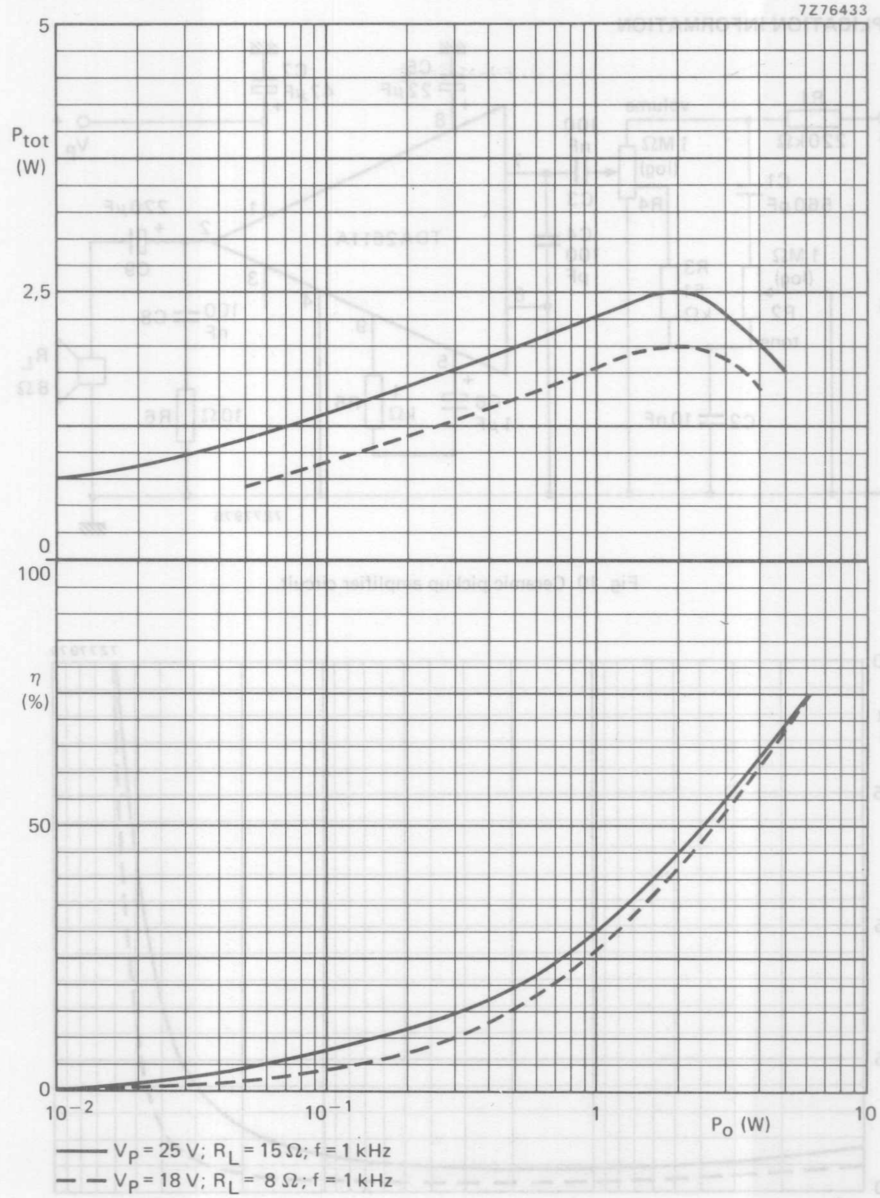



Fig. 9 Total power dissipation and efficiency as a function of output power.

## APPLICATION INFORMATION

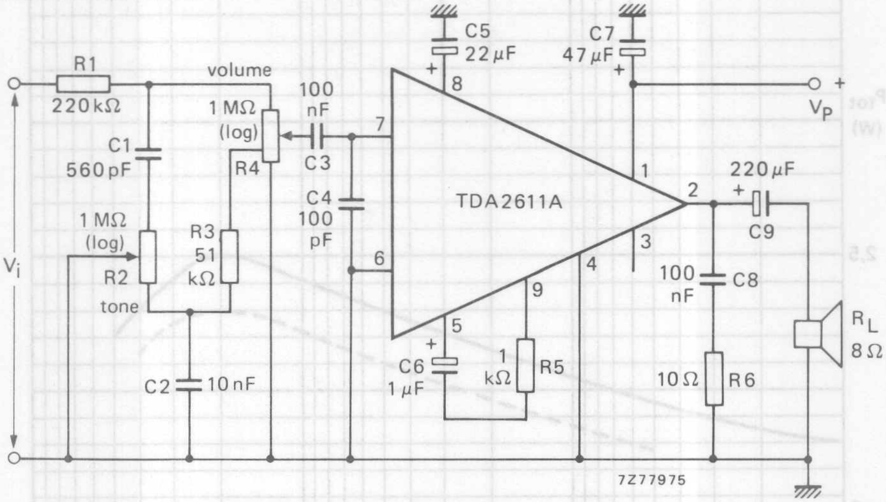



Fig. 10 Ceramic pickup amplifier circuit.

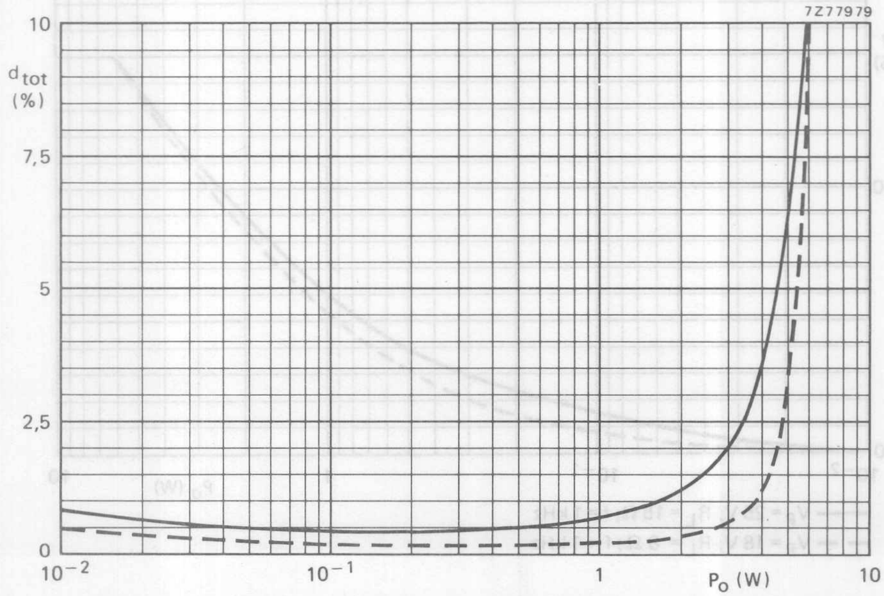



Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

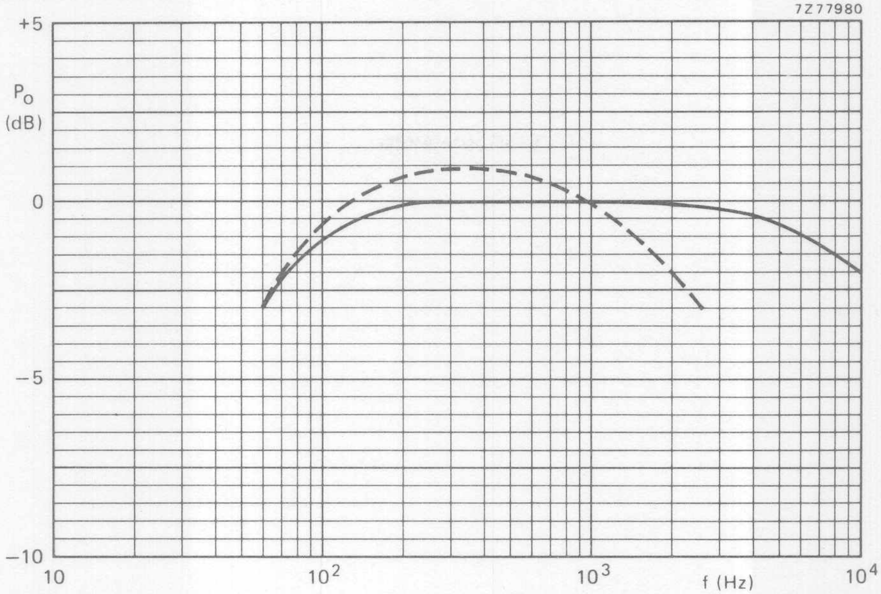



Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; $P_o$ relative to 0 dB = 3 W; typical values.

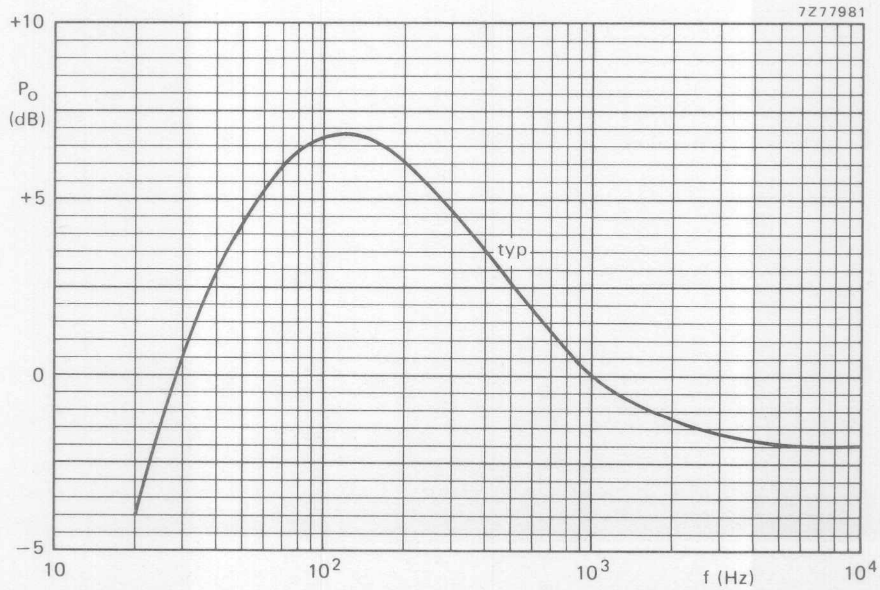



Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

# INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

### Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 8) | $V_P = V_{8\text{-}16}$ | typ. | 5 V |
| Supply current (pin 8) | $I_P = I_8$ | typ. | 2,1 mA |
| Input signal (peak-to-peak value) (100% AM; f = 36 kHz) | $V_{2\text{-}15(p\text{-}p)}$ | | 0,02 to 200 mV |
| Output signal (peak-to-peak value) | $V_{9\text{-}16(p\text{-}p)}$ | typ. | 4,5 V |

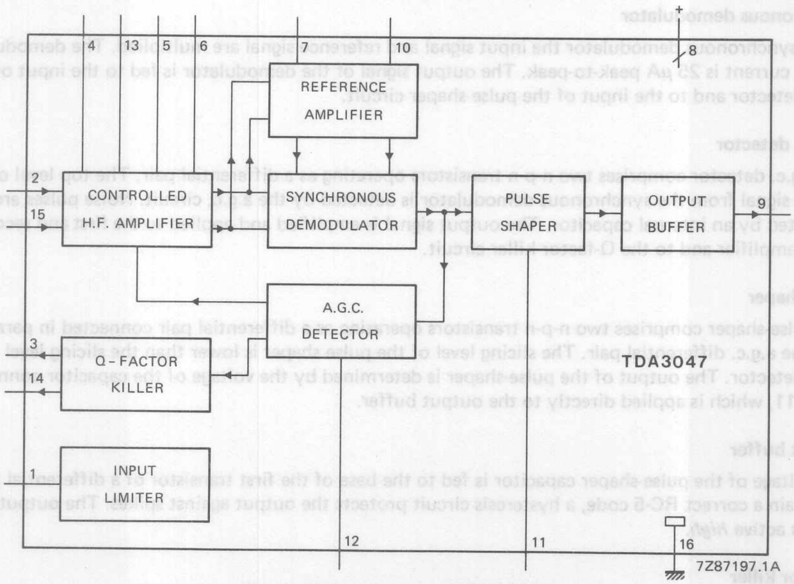



Fig. 1 Block diagram of TDA3047.

## PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT-38).
TDA3047T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

## FUNCTIONAL DESCRIPTION

### General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 $\mu$A with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

### Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

### Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

### Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 $\mu$A peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

### A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

### Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

### Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

### Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

**FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET**

# INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

**Features**

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 8) | $V_P = V_{8\text{-}16}$ | typ. | 5 | V |
| Supply current (pin 8) | $I_P = I_8$ | typ. | 2,1 | mA |
| Input signal (peak-to-peak value) (100% AM; f = 36 kHz) | $V_{2\text{-}15(p\text{-}p)}$ | | 0,02 to 200 | mV |
| Output signal (peak-to-peak value) | $V_{9\text{-}16(p\text{-}p)}$ | typ. | 4,5 | V |

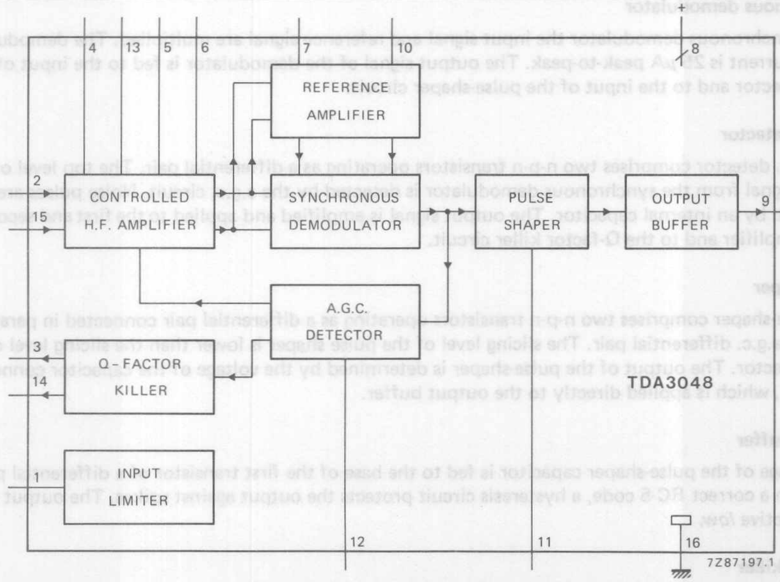



Fig. Block diagram of TDA3048.

## PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT-38).
TDA3048T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

## FUNCTIONAL DESCRIPTION

### General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 $\mu$A with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

### Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

### Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

### Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 $\mu$A peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

### A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

### Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

### Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low*.

### Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

# SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

**Features**

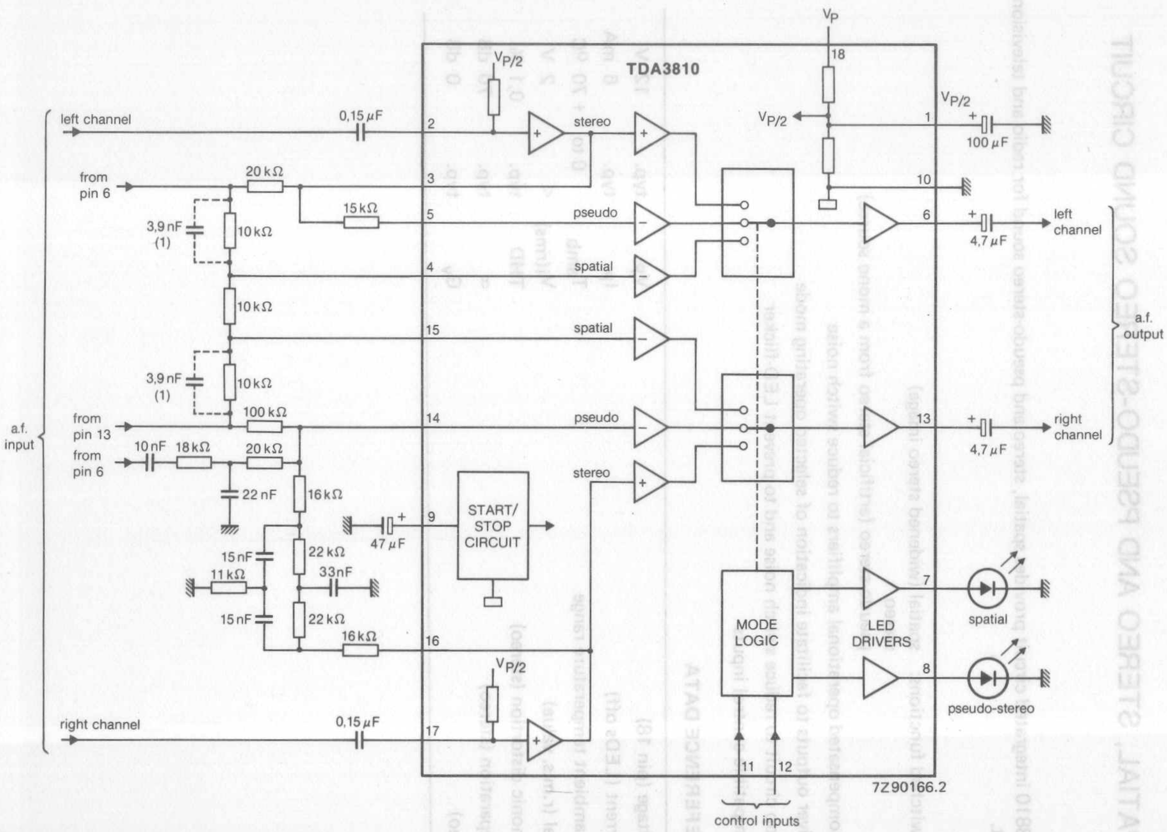
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 18) | $V_P$ | typ. | 12 | V |
| Supply current (LEDs off) | $I_P$ | typ. | 6 | mA |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 | $^oC$ |
| Input signal (r.m.s. value) | $V_{i(rms)}$ | < | 2 | V |
| Total harmonic distortion (stereo) | THD | typ. | 0,1 | % |
| Channel separation (stereo) | $\alpha$ | typ. | 70 | dB |
| Gain (stereo) | $G_v$ | typ. | 0 | dB |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).




(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 18) | $V_P$ | max. | 18 V |
| Storage temperature range | $T_{stg}$ | | −25 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 °C |

**THERMAL RESISTANCE**

| | | | |
|---|---|---|---|
| From crystal to ambient | $R_{th\ cr\text{-}a}$ | = | 80 K/W |

**CHARACTERISTICS**

$V_P$ = 12 V; $T_{amb}$ = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10, 13\text{-}10} \geqslant 4{,}7\ k\Omega$; $C_{6\text{-}10, 13\text{-}10} \leqslant 150\ pF$.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage range (pin 18) | $V_P$ | 4,5 | – | 16,5 | V |
| Supply current | $I_P$ | – | 6 | 12 | mA |
| Reference voltage | $V_S$ | 5,3 | 6 | 6,7 | V |
| Input voltage (pin 2 or 17) THD = 0,2% (stereo mode) | $V_{i(rms)}$ | – | – | 2 | V |
| Input resistance (pin 2 or 17) | $R_i$ | 50 | 75 | – | kΩ |
| Voltage gain $V_o/V_i$ | $G_v$ | – | 0 | – | dB |
| Channel separation (R/L) | $\alpha$ | 60 | 70 | – | dB |
| Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V | THD | – | 0,1 | – | % |
| Power supply ripple rejection | RR | – | 50 | – | dB |
| Noise output voltage (unweighted) left and right output | $V_{n(rms)}$ | – | 10 | – | μV |
| *SPATIAL MODE* (pins 11 and 12 HIGH) | | | | | |
| Antiphase crosstalk | $\alpha$ | – | 50 | – | % |
| Voltage gain | $G_v$ | 1,4 | 2,4 | 3,4 | dB |

**PSEUDO-STEREO MODE**

The quality and strength of the pseudo-stereo effect is determined by external filter components.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| *CONTROL INPUTS* (pins 11 and 12) | | | | | |
| Input resistance | $R_i$ | 70 | 120 | – | kΩ |
| Switching current | $-I_i$ | – | 35 | 100 | μA |
| *LED DRIVERS* (pins 7 and 8) | | | | | |
| Output current for LED | $-I_o$ | 10 | 12 | 15 | mA |
| Forward voltage | $V_F$ | – | – | 6 | V |

Truth table

| mode | control input state pin 11 | control input state pin 12 | LED spatial pin 7 | LED pseudo pin 8 |
|---|---|---|---|---|
| Mono pseudo-stereo | HIGH | LOW | off | on |
| Spatial stereo | HIGH | HIGH | on | off |
| Stereo | LOW | X | off | off |

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

# FM RADIO CIRCUIT

## GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 5) | $V_P$ | | 2,7 to 10 | V |
| Supply current at $V_P$ = 4,5 V | $I_P$ | typ. | 8 | mA |
| R.F. input frequency range | $f_{rf}$ | | 1,5 to 110 | MHz |
| Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled) | EMF | typ. | 1,5 | μV |
| Signal handling (e.m.f. voltage) (source impedance: 75 Ω) | EMF | typ. | 200 | mV |
| A.F. output voltage at $R_L$ = 22 kΩ | $V_o$ | typ. | 75 | mV |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

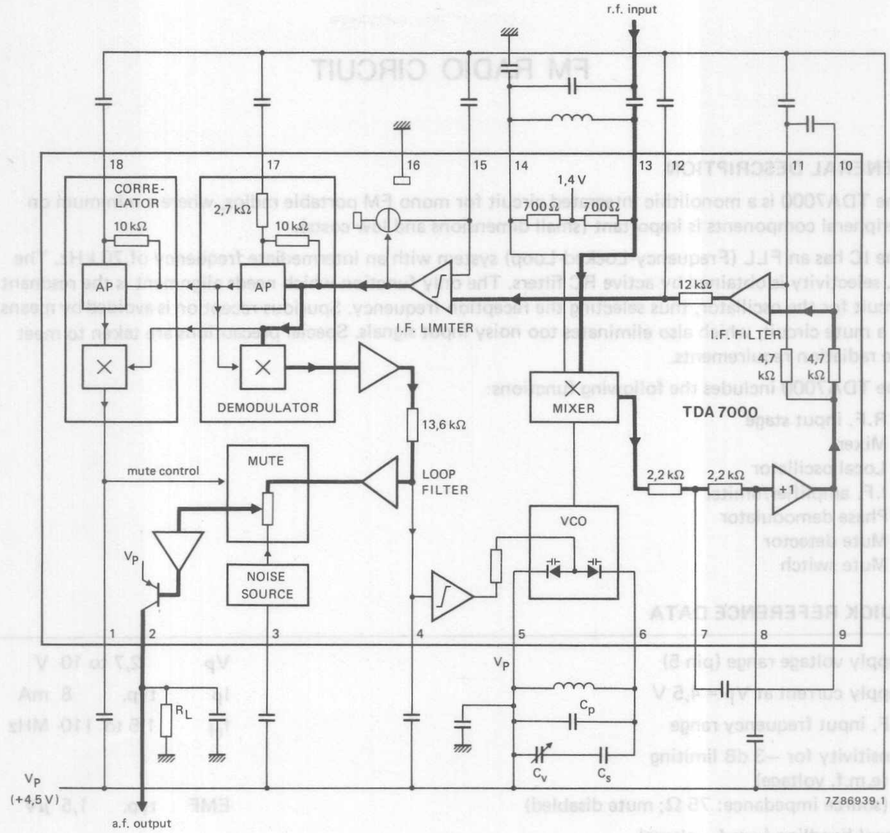



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|---|---|---|
| Supply voltage (pin 5) | $V_P$ | max. 12 V |
| Oscillator voltage (pin 6) | $V_{6\text{-}5}$ | $V_P$–0,5 to $V_P$+0,5 V |
| Total power dissipation | | see derating curve Fig. 2 |
| Storage temperature range | $T_{stg}$ | –55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | 0 to + 60 °C |

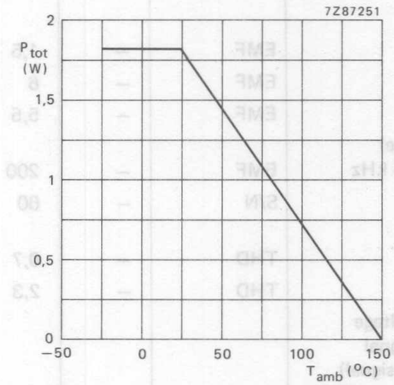



Fig. 2 Power derating curve.

## D.C. CHARACTERISTICS

$V_P$ = 4,5 V; $T_{amb}$ = 25 °C; measured in Fig. 4; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage (pin 5) | $V_P$ | 2,7 | 4,5 | 10 | V |
| Supply current at $V_P$ = 4,5 V | $I_P$ | – | 8 | – | mA |
| Oscillator current (pin 6) | $I_6$ | – | 280 | – | μA |
| Voltage at pin 14 | $V_{14\text{-}16}$ | – | 1,35 | – | V |
| Output current at pin 2 | $I_2$ | – | 60 | – | μA |
| Voltage at pin 2; $R_L$ = 22 kΩ | $V_{2\text{-}16}$ | – | 1,3 | – | V |

## A.C. CHARACTERISTICS

$V_P$ = 4,5 V; $T_{amb}$ = 25 °C; measured in Fig. 4 (mute switch open, enabled); $f_{rf}$ = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; $f_m$ = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Sensitivity (see Fig. 3) (e.m.f. voltage) | | | | | |
| for −3 dB limiting; muting disabled | EMF | – | 1,5 | – | μV |
| for −3 dB muting | EMF | – | 6 | – | μV |
| for S/N = 26 dB | EMF | – | 5,5 | – | μV |
| Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz | EMF | – | 200 | – | mV |
| Signal-to-noise ratio | S/N | – | 60 | – | dB |
| Total harmonic distortion | | | | | |
| at Δf = ± 22,5 kHz | THD | – | 0,7 | – | % |
| at Δf = ± 75 kHz | THD | – | 2,3 | – | % |
| AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: $f_m$ = 1 kHz; Δf = ± 75 kHz AM signal: $f_m$ = 1 kHz; m = 80% | AMS | – | 50 | – | dB |
| Ripple rejection ($\Delta V_P$ = 100 mV; f = 1 kHz) | RR | – | 10 | – | dB |
| Oscillator voltage (r.m.s. value) at pin 6 | $V_{6\text{-}5(rms)}$ | – | 250 | – | mV |
| Variation of oscillator frequency with supply voltage ($\Delta V_P$ = 1 V) | $\Delta f_{osc}$ | – | 60 | – | kHz/V |
| Selectivity | $S_{+300}$ | – | 45 | – | dB |
| | $S_{-300}$ | – | 35 | – | dB |
| A.F.C. range | $\Delta f_{rf}$ | – | ± 300 | – | kHz |
| Audio bandwidth at $\Delta V_o$ = 3 dB measured with pre-emphasis (t = 50 μs) | B | – | 10 | – | kHz |
| A.F. output voltage (r.m.s. value) at $R_L$ = 22 kΩ | $V_{o(rms)}$ | – | 75 | – | mV |
| Load resistance | | | | | |
| at $V_P$ = 4,5 V | $R_L$ | – | – | 22 | kΩ |
| at $V_P$ = 9,0 V | $R_L$ | – | – | 47 | kΩ |

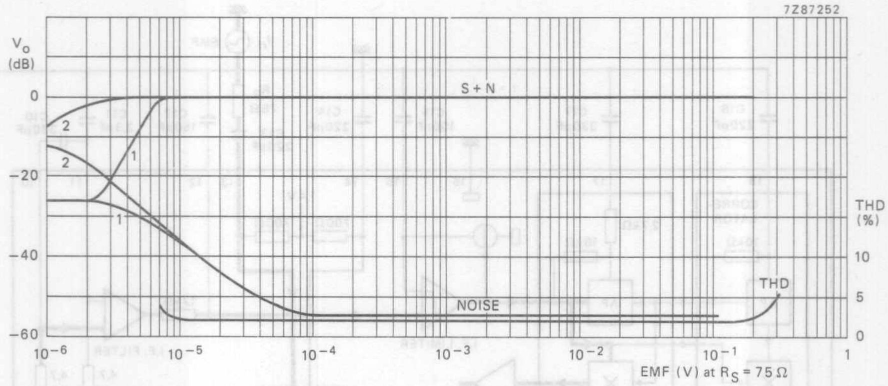



Fig. 3 A.F. output voltage ($V_o$) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance ($R_S$) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; $f_{rf}$ = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; $f_m$ = 1 kHz.
for THD curve: Δf = ± 75 kHz; $f_m$ = 1 kHz.

**Notes**

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

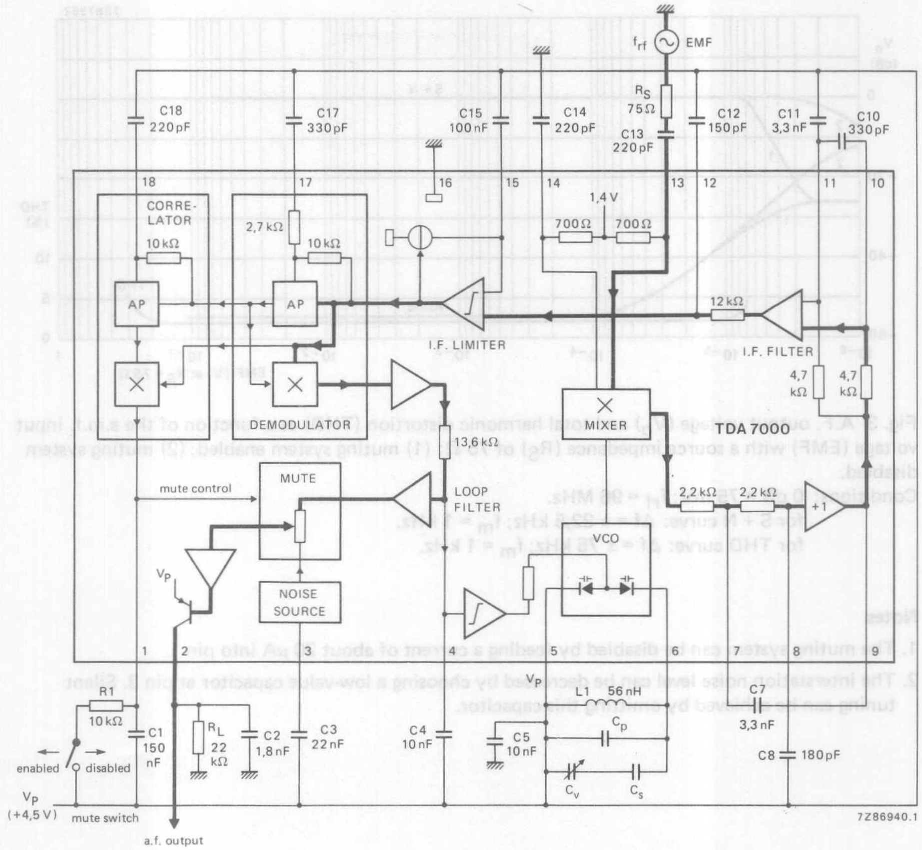



Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

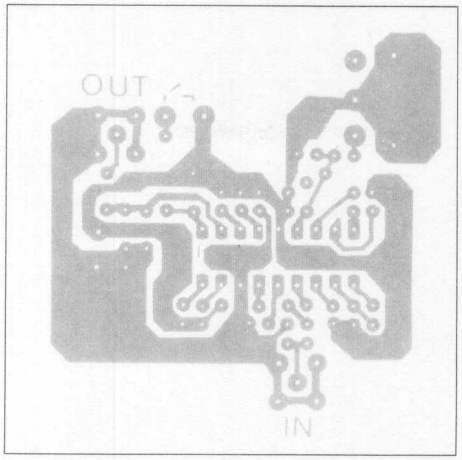



Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

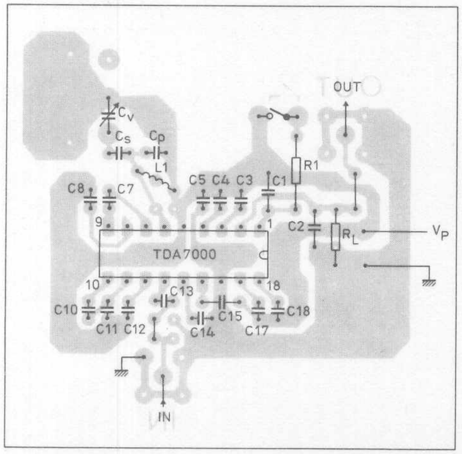



Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

# FM RADIO CIRCUIT

## GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 4) | $V_P$ | | 2,7 to 10 | V |
| Supply current at $V_P$ = 4,5 V | $I_P$ | typ. | 8 | mA |
| R.F. input frequency range | $f_{rf}$ | | 1,5 to 110 | MHz |
| Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled) | EMF | typ. | 1,5 | μV |
| Signal handling (e.m.f. voltage) (source impedance: 75 Ω) | EMF | typ. | 200 | mV |
| A.F. output voltage at $R_L$ = 22 kΩ | $V_o$ | typ. | 75 | mV |

## PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

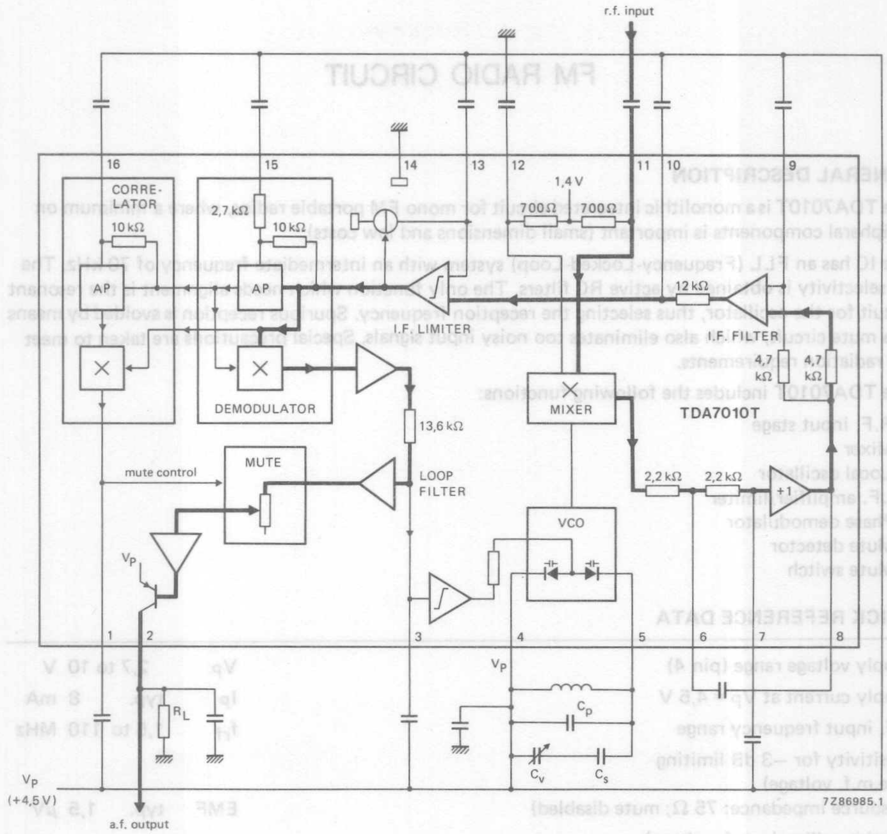



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 4) | $V_P$ | max. | 12 V |
| Oscillator voltage (pin 5) | $V_{6\text{-}5}$ | | $V_P$–0,5 to $V_P$ +0,5 V |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature range | $T_{stg}$ | | –55 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 60 °C |

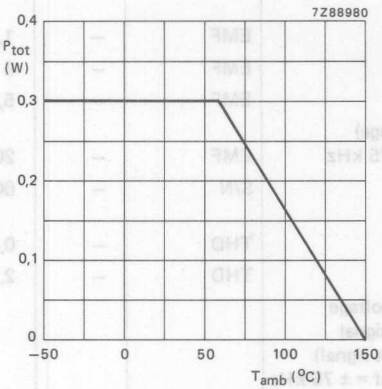



Fig. 2 Power derating curve.

## D.C. CHARACTERISTICS

$V_P$ = 4,5 V; $T_{amb}$ = 25 °C; measured in Fig. 4; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage (pin 4) | $V_P$ | 2,7 | 4,5 | 10 | V |
| Supply current at $V_P$ = 4,5 V | $I_P$ | | 8 | – | mA |
| Oscillator current (pin 5) | $I_5$ | – | 280 | – | µA |
| Voltage at pin 12 | $V_{12\text{-}14}$ | – | 1,35 | – | V |
| Output current at pin 2 | $I_2$ | – | 60 | – | µA |
| Voltage at pin 2; $R_L$ = 22 kΩ | $V_{2\text{-}14}$ | – | 1,3 | – | V |

## A.C. CHARACTERISTICS

$V_P$ = 4,5 V; $T_{amb}$ = 25 °C; measured in Fig. 4 (mute switch open, enabled); $f_{rf}$ = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; $f_m$ = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Sensitivity (see Fig. 3) (e.m.f. voltage) | | | | | |
| for −3 dB limiting; muting disabled | EMF | – | 1,5 | – | μV |
| for −3 dB muting | EMF | – | 6 | – | μV |
| for S/N = 26 dB | EMF | – | 5,5 | – | μV |
| Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz | EMF | – | 200 | – | mV |
| Signal-to-noise ratio | S/N | – | 60 | – | dB |
| Total harmonic distortion | | | | | |
| at Δf = ± 22,5 kHz | THD | – | 0,7 | – | % |
| at Δf = ± 75 kHz | THD | – | 2,3 | – | % |
| AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: $f_m$ = 1 kHz; Δf = ± 75 kHz AM signal: $f_m$ = 1 kHz; m = 80% | AMS | – | 50 | – | dB |
| Ripple rejection ($\Delta V_P$ = 100 mV; f = 1 kHz) | RR | – | 10 | – | dB |
| Oscillator voltage (r.m.s. value) at pin 5 | $V_{5\text{-}4(rms)}$ | – | 250 | – | mV |
| Variation of oscillator frequency with supply voltage ($\Delta V_P$ = 1 V) | $\Delta f_{osc}$ | – | 60 | – | kHz/V |
| Selectivity | $S_{+300}$ | – | 43 | – | dB |
| | $S_{-300}$ | – | 28 | – | dB |
| A.F.C. range | $\Delta f_{rf}$ | – | ± 300 | – | kHz |
| Audio bandwidth at $\Delta V_o$ = 3 dB measured with pre-emphasis (t = 50 μs) | B | – | 10 | – | kHz |
| A.F. output voltage (r.m.s. value) at $R_L$ = 22 kΩ | $V_{o(rms)}$ | – | 75 | – | mV |
| Load resistance | | | | | |
| at $V_P$ = 4,5 V | $R_L$ | – | – | 22 | kΩ |
| at $V_P$ = 9,0 V | $R_L$ | – | – | 47 | kΩ |

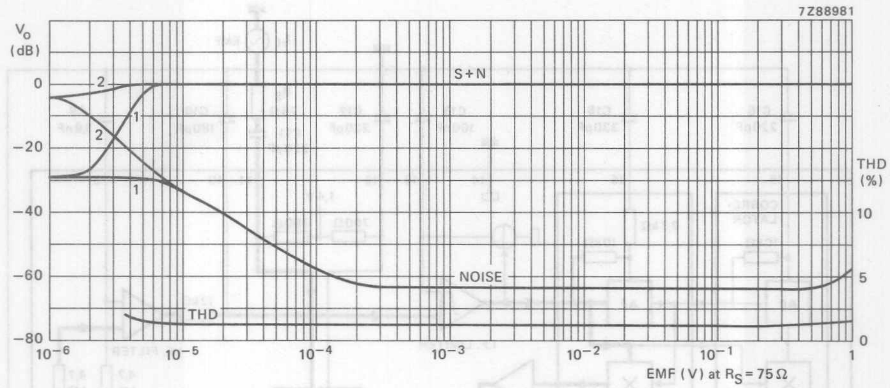



Fig. 3 A.F. output voltage ($V_o$) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance ($R_S$) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; $f_{rf}$ = 96 MHz.
for S + N curve: $\Delta f = \pm$ 22,5 kHz; $f_m$ = 1 kHz.
for THD curve: $\Delta f = \pm$ 75 kHz; $f_m$ = 1 kHz.

## Notes

1. The muting system can be disabled by feeding a current of about 20 $\mu$A into pin 1.

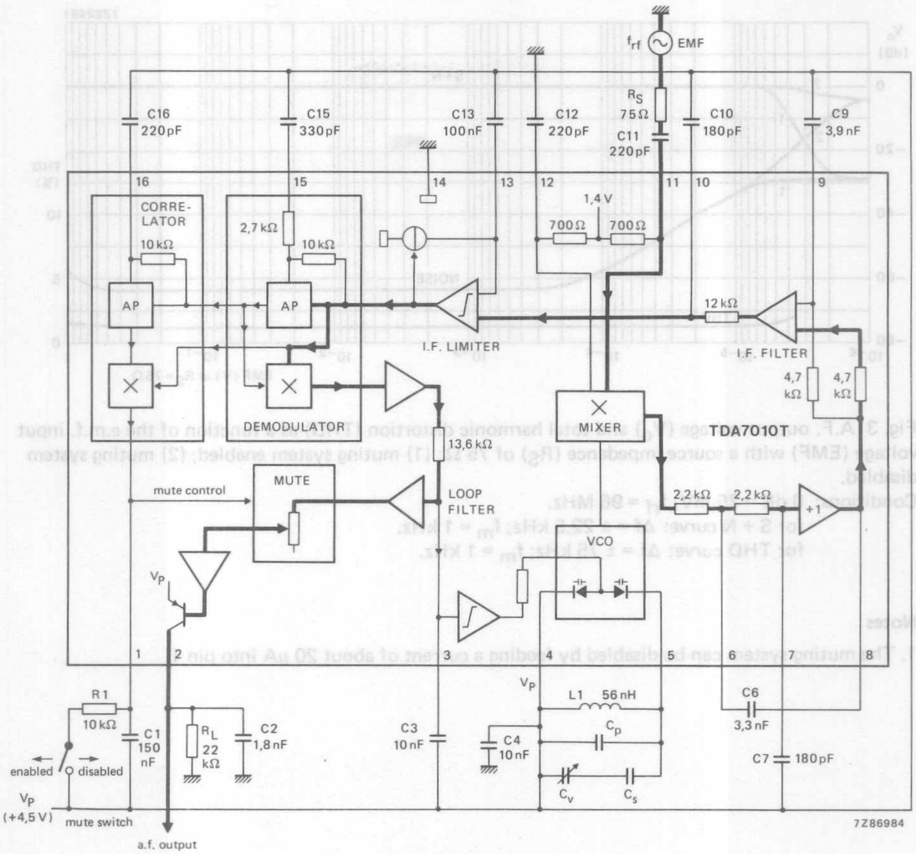



Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

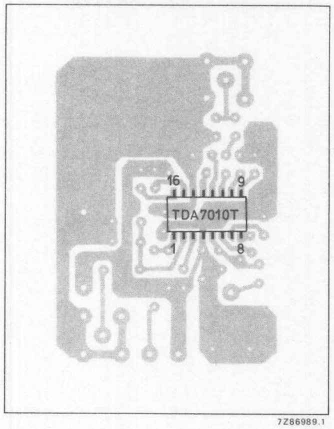



Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

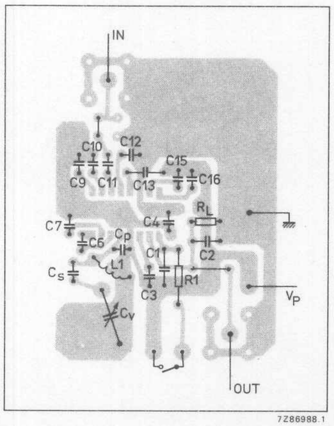



Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

# FM RADIO CIRCUIT

## GENERAL DESCRIPTION

The TDA7020T integrated circuit is for FM portable radios, stereo as well as mono, where a minimum periphery is important in terms of small dimensions and low cost. The IC has a FLL (Frequency Locked Loop) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant circuit of the oscillator. Interstation-noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

The TDA7020T includes the following functions:

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- Loop amplifier
- Internal reference circuit
- LF amplifier for:
  - mono earphone amplifier or
  - MUX filter
- field-strength dependent channel separation control facility

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 4) | $V_P$ | | 1,8 to 6 | V |
| Supply current at $V_P$ = 3 V | $I_P$ | typ. | 6,3 | mA |
| RF input frequency range | $f_{rf}$ | | 1,5 to 110 | MHz |
| Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled) | EMF | typ. | 4 | μV |
| Signal handling (e.m.f. voltage) (source impedance: 75 Ω) | EMF | typ. | 200 | mV |
| AF output voltage | $V_o$ | typ. | 90 | mV |

## PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

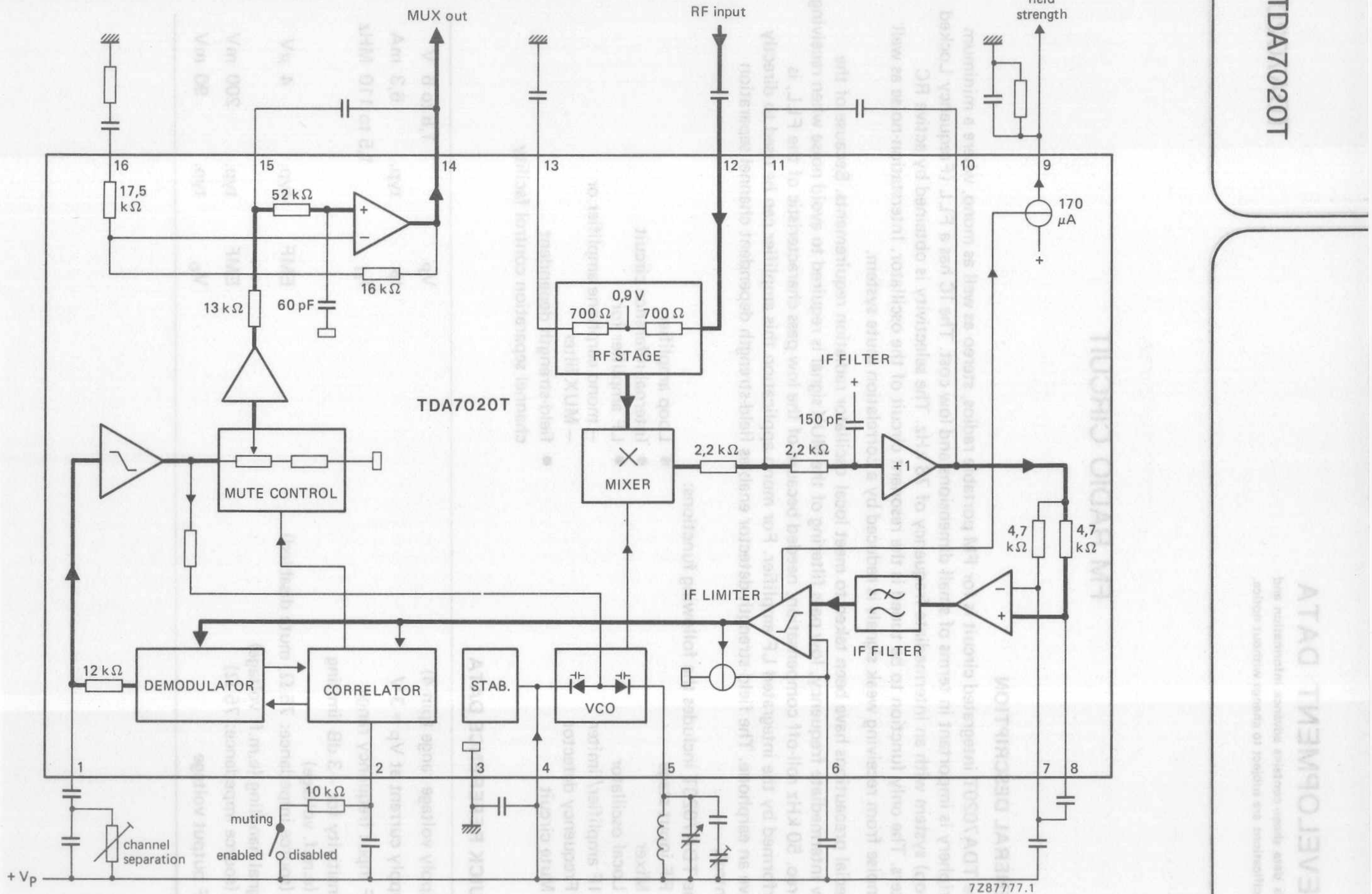



Fig. 1 Block diagram.

DEVELOPMENT DATA

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 4) | $V_P$ | max. | 7 V |
| Oscillator voltage (pin 5) | $V_{6\text{-}5}$ | | $V_P$ −0,5 to $V_P$ +0,5 V |
| Storage temperature range | $T_{stg}$ | | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −10 to +70 °C |

## THERMAL RESISTANCE

| | | |
|---|---|---|
| From junction to ambient | $R_{th\ j\text{-}a}$ | 300 K/W |

## D.C. CHARACTERISTICS

$V_P$ = 3 V; $T_{amb}$ = 25 °C; measured in Fig. 4; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage (pin 4) | $V_{4\text{-}3}$ | 1,8 | 3,0 | 6 | V |
| Supply current at $V_P$ = 3 V | $-I_3$ | – | 6,3 | – | mA |
| Oscillator current (pin 5) | $I_5$ | – | 250 | – | μA |
| Voltage at pin 13 | $V_{13\text{-}3}$ | – | 0,9 | – | V |
| Output voltage (pin 14) | $V_{14\text{-}3}$ | – | 1,3 | – | V |

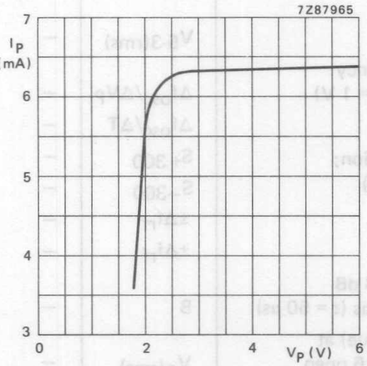



Fig. 2 Supply current as a function of the supply voltage.

## A.C. CHARACTERISTICS (MONO OPERATION)

$V_P$ = 3 V; $T_{amb}$ = 25 °C; measured in Fig. 6; $f_{rf}$ = 96 MHz modulated with Δf = ± 22,5 kHz; $f_m$ = 1 kHz; EMF = 300 μV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Sensitivity (see Fig. 3) (e.m.f. voltage) | | | | | |
| for −3 dB limiting; muting disabled | EMF | – | 4,0 | – | μV |
| for −3 dB muting | EMF | – | 5,0 | – | μV |
| for S/N = 26 dB | EMF | – | 7 | – | μV |
| Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz | EMF | – | 200 | – | mV |
| Signal-to-noise ratio | S/N | – | 60 | – | dB |
| Total harmonic distortion | | | | | |
| at Δf = ± 22,5 kHz | THD | – | 0,7 | – | % |
| at Δf = ± 75 kHz | THD | – | 2,3 | – | % |
| AM suppression of output voltage (ratio of AM signal: $f_m$ = 1 kHz; m = 80% to FM signal: $f_m$ = 1 kHz; Δf = ± 75 kHz) | AMS | – | 50 | – | dB |
| Ripple rejection ($\Delta V_P$ = 100 mV; f = 1 kHz) | RR | – | 30 | – | dB |
| Oscillator voltage (pin 5) r.m.s. value | $V_{5\text{-}3(rms)}$ | – | 250 | – | mV |
| Variation of oscillator frequency | | | | | |
| with supply voltage ($\Delta V_P$ = 1 V) | $\Delta f_{osc}/\Delta V_P$ | – | 5 | – | kHz/V |
| with temperature | $\Delta f_{osc}/\Delta T$ | – | 0,2 | – | kHz/K |
| Selectivity (without modulation; test circuit Fig. 8) | $S_{+300}$ | – | 30 | – | dB |
| | $S_{-300}$ | – | 46 | – | dB |
| AFC range | $\pm\Delta f_{rf}$ | – | 160 | – | kHz |
| Mute range | $\pm\Delta f_{rf}$ | – | 120 | – | kHz |
| Audio bandwidth at $\Delta V_o$ = 3 dB measured with pre-emphasis (t = 50 μs) | B | – | 10 | – | kHz |
| AF output voltage (r.m.s. value) at $R_{L(pin\ 14)}$ = 100 Ω; pin 16 open | $V_{o(rms)}$ | – | 90 | – | mV |
| AF output current | | | | | |
| max. d.c. load | $I_{o(dc)}$ | −100 | – | + 100 | μA |
| max. a.c. load for THD = 10%; peak value | $I_{o(ac)}$ | – | 3 | – | mA |

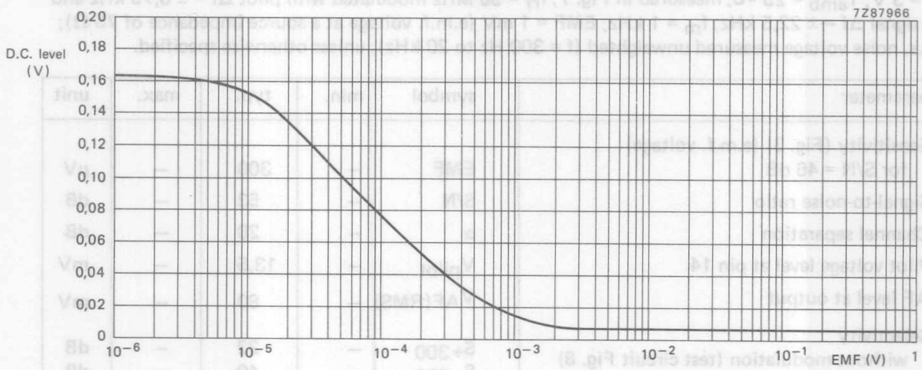



Fig. 3 Fieldstrength voltage ($V_{9\text{-}3}$) at $R_s$ = 1 kΩ; f = 96,75 MHz and supply voltage is 3 V.

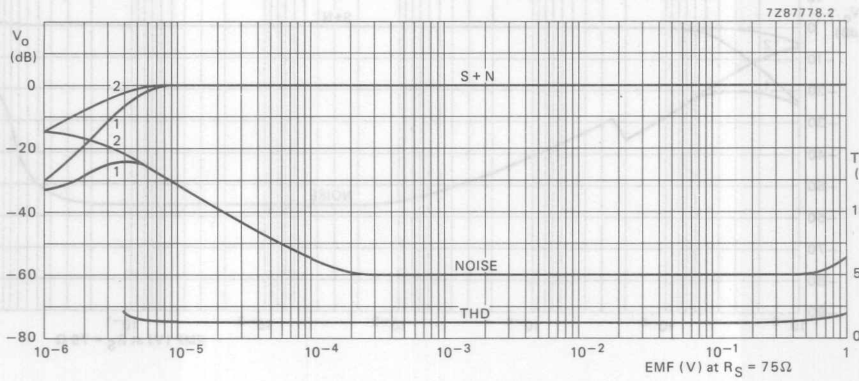



Fig. 4 MONO operation. A.F. output voltage ($V_o$) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance ($R_S$) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 100 mV; $f_{rf}$ = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; $f_m$ = 1 kHz.
for THD curve : Δf = ± 75 kHz; $f_m$ = 1 kHz.

## A.C. CHARACTERISTICS (STEREO OPERATION)

$V_P$ = 3 V; $T_{amb}$ = 25 °C; measured in Fig. 7; $f_{rf}$ = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; $f_m$ = 1 kHz; EMF = 1 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Sensitivity (Fig. 3) (e.m.f. voltage) for S/N = 46 dB | EMF | – | 300 | – | μV |
| Signal-to-noise ratio | S/N | – | 53 | – | dB |
| Channel separation | α | – | 20 | – | dB |
| Pilot voltage level at pin 14 | $V_{pilot}$ | – | 13,5 | – | mV |
| AF level at output | $V_{AF(RMS)}$ | – | 80 | – | mV |
| Selectivity without modulation (test circuit Fig. 8) | $S_{+300}$ | – | 22 | – | dB |
| | $S_{-300}$ | – | 40 | – | dB |

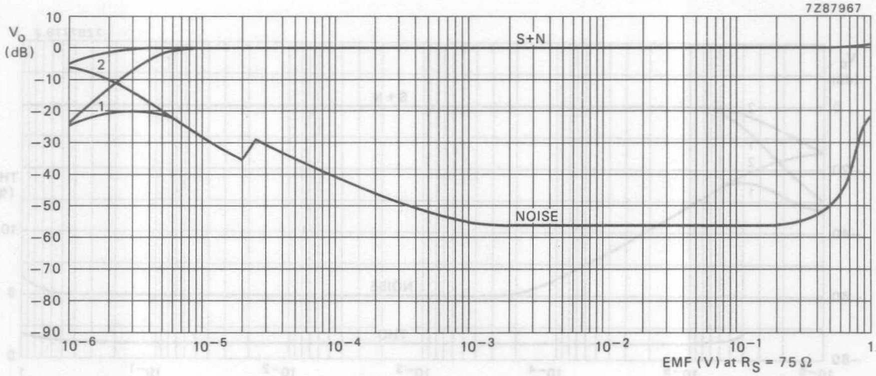



Fig. 5 STEREO operation.

A.F. output Voltage ($V_O$) as a function of the e.m.f. input voltage (EMF). (1) Muting system enabled; (2) muting system disabled.

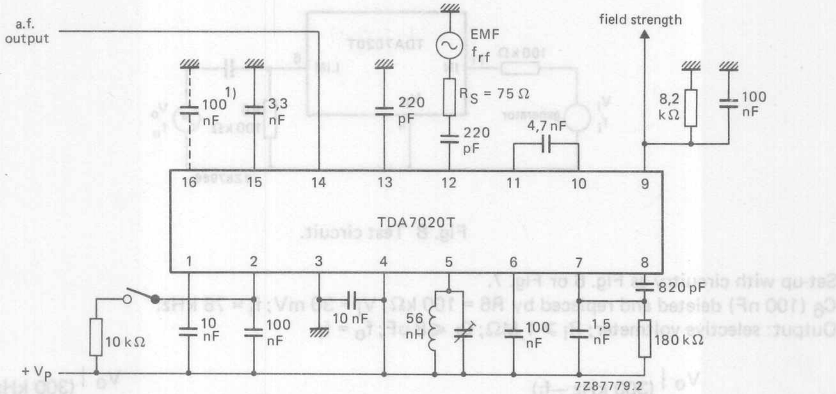



Fig. 6 Test circuit for MONO operation.

1) The AF output can be decreased by 5 dB by disconnection of the 100 nF capacitor of pin 16.

DEVELOPMENT DATA

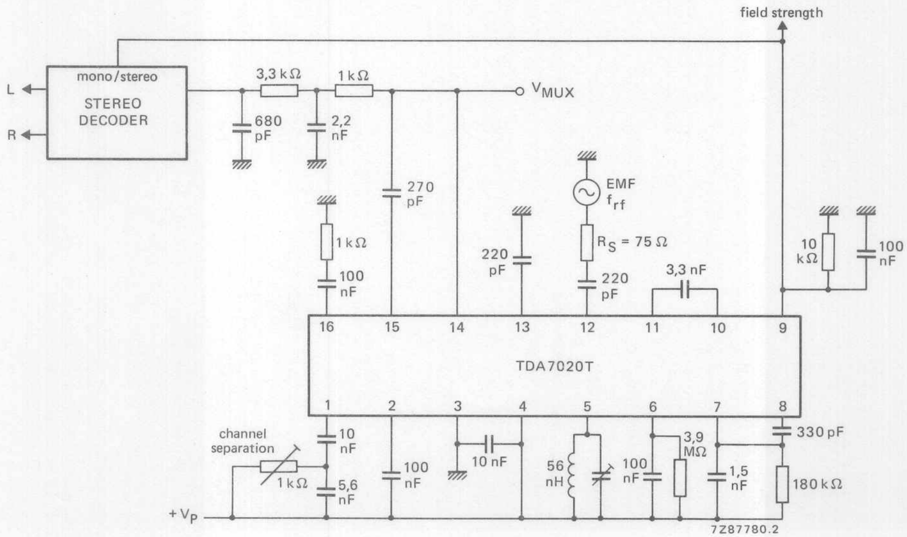



Fig. 7 Test circuit for STEREO operation.

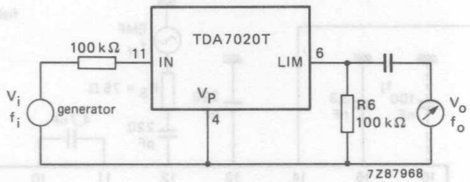



Fig. 8 Test circuit.

Set-up with circuitry as Fig. 6 or Fig. 7.
$C_6$ (100 nF) deleted and replaced by R6 = 100 kΩ; $V_i$ = 30 mV; $f_i$ = 76 kHz.
Output: selective voltmeter; $R_i \geqslant 1$ MΩ; $C_i \leqslant 8$ pF; $f_o = f_i$

$$S_{+300} = 20 \lg \frac{V_o \mid_{(300\ \text{kHz} - f_i)}}{V_o \mid f_i} \qquad S_{-300} = 20 \lg \frac{V_o \mid_{(300\ \text{kHz} + f_i)}}{V_o \mid f_i}$$

# LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

## GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

### Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 1,6 to 6,0 | V |
| Total quiescent current (at $V_P$ = 3 V) | $I_{tot}$ | typ. | 3,2 | mA |
| **Bridge tied load application (BTL)** | | | | |
| Output power at $R_L$ = 32 Ω<br>$V_P$ = 3 V; $d_{tot}$ = 10% | $P_o$ | typ. | 140 | mW |
| D.C. output offset voltage between the outputs | $\|\Delta V\|$ | max. | 70 | mV |
| Noise output voltage (r.m.s. value)<br>at f = 1 kHz; $R_S$ = 5 kΩ | $V_{no(rms)}$ | typ. | 140 | μV |
| **Stereo application** | | | | |
| Output power at $R_L$ = 32 Ω<br>$d_{tot}$ = 10%; $V_P$ = 3 V | $P_o$ | typ. | 35 | mW |
| $d_{tot}$ = 10%; $V_P$ = 4,5 V | $P_o$ | typ. | 75 | mW |
| Channel separation at $R_S$ = 0 Ω; f = 1 kHz | $\alpha$ | typ. | 40 | dB |
| Noise output voltage (r.m.s. value)<br>at f = 1 kHz; $R_S$ = 5 kΩ | $V_{no(rms)}$ | typ. | 100 | μV |

## PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | 6 | V |
| Peak output current | $I_{OM}$ | max. | 150 | mA |
| Total power dissipation | see derating curve Fig. 1 | | | |
| Storage temperature range | $T_{stg}$ | −55 to + 150 | | °C |
| Crystal temperature | $T_c$ | max. | 100 | °C |
| A.C. and d.c. short-circuit duration at $V_P$ = 3,0 V (during mishandling) | $t_{sc}$ | max. | 5 | s |

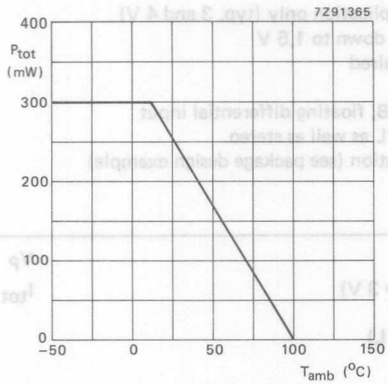



Fig. 1 Power derating curve.

## SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1 \text{ W.}$$

## CHARACTERISTICS

$V_P$ = 3 V; f = 1 kHz; $R_L$ = 32 Ω; $T_{amb}$ = 25 °C; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage | $V_P$ | 1,6 | – | 6,0 | V |
| Total quiescent current | $I_{tot}$ | – | 3,2 | 4 | mA |
| **Bridge-tied load application (BTL)**; see Fig. 4 | | | | | |
| Output power* | | | | | |
| $V_P$ = 3,0 V; $d_{tot}$ = 10% | $P_o$ | – | 140 | – | mW |
| $V_P$ = 4,5 V; $d_{tot}$ = 10% ($R_L$ = 64 Ω) | $P_o$ | – | 150 | – | mW |
| Voltage gain | $G_v$ | – | 32 | – | dB |
| Noise output voltage (r.m.s. value) | | | | | |
| $R_S$ = 5 kΩ; f = 1 kHz | $V_{no(rms)}$ | – | 140 | | μV |
| $R_S$ = 0 Ω; f = 500 kHz; B = 5 kHz | $V_{no(rms)}$ | – | tbf | | μV |
| D.C. output offset voltage (at $R_S$ = 5 kΩ) | $\|\Delta V\|$ | – | – | 70 | mV |
| Input impedance (at $R_S$ = ∞) | $\|Z_i\|$ | 1 | – | – | MΩ |
| Input bias current | $I_i$ | – | 40 | – | nA |
| **Stereo application**; see Fig. 5 | | | | | |
| Output power* | | | | | |
| $V_P$ = 3,0 V; $d_{tot}$ = 10% | $P_o$ | – | 35 | – | mW |
| $V_P$ = 4,5 V; $d_{tot}$ = 10% | $P_o$ | – | 75 | – | mW |
| Voltage gain | $G_v$ | – | 26 | – | dB |
| Noise output voltage (r.m.s. value) | | | | | |
| $R_S$ = 5 kΩ; f = 1 kHz | $V_{no(rms)}$ | – | 100 | – | μV |
| $R_S$ = 0 Ω; f = 500 kHz; B = 5 kHz | $V_{no(rms)}$ | – | tbf | – | μV |
| Channel separation | | | | | |
| $R_S$ = 0 Ω; f = 1 kHz | α | 30 | 40 | – | dB |
| Input impedance (at $R_S$ = ∞) | $\|Z_i\|$ | 2 | – | – | MΩ |
| Input bias current | $I_i$ | – | 20 | – | nA |

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

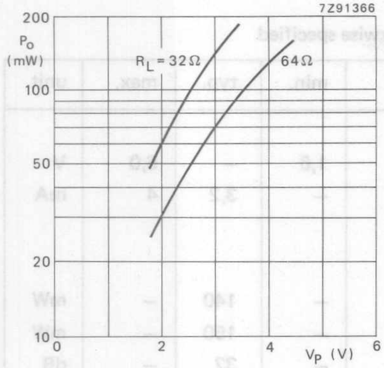



Fig. 2 Output power across the load impedance ($R_L$) as a function of supply voltage ($V_P$) in BTL application. Measurements were made at f = 1 kHz; $d_{tot}$ = 10%; $T_{amb}$ = 25 °C.

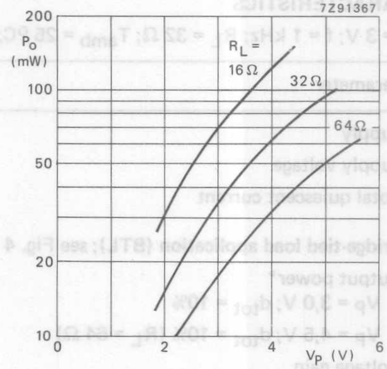



Fig. 3 Output power across the load impedance ($R_L$) as a function of supply voltage ($V_P$) in stereo application. Measurements were made at f = 1 kHz; $d_{tot}$ = 10%; $T_{amb}$ = 25 °C.

## APPLICATION INFORMATION

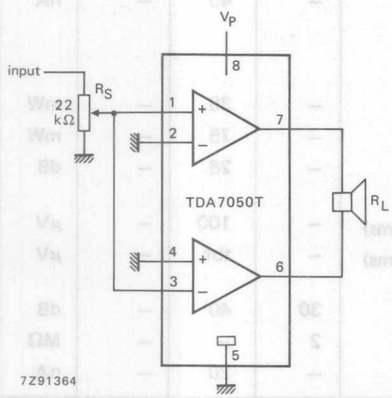



Fig. 4 Application diagram (BTL); also used as test circuit.

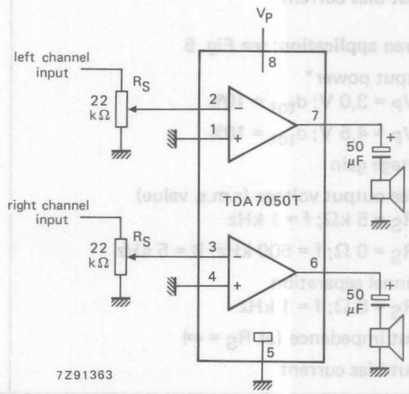



Fig. 5 Application diagram (stereo); also used as test circuit.

# DOLBY* B & C TYPE NOISE REDUCTION CIRCUITS

## GENERAL DESCRIPTION

The TEA0651/TEA0652 and TEA0654 provide both, Dolby B and Dolby C type audio Noise Reduction (NR). The TEA0651/TEA0652 are NR signal processing ICs in 18-lead DIL packages. They can be used either as a stereo Dolby B NR circuit or as one channel of a switchable Dolby B & C NR circuit. In addition they provide NR ON/OFF switching.
The TEA0654 is a switching IC in a 24-lead DIL package. It contains the switching, the pre-amplifiers for playback and recording functions and a multiplex filter buffer amplifier.
The circuits are pin compatible to Signetics NE651, NE652 and NE654 respectively.

### Features

TEA0651/TEA0652

- Dual purpose IC for Dolby B & C NR systems:
  switchable B/C type NR systems, B-type NR systems (stereo without preamplifiers), automotive entertainment systems (playback only) and portable applications
- Dual version for better matching between HIGH and LOW level stages in C-type NR or better channel matching for stereo B-type NR applications
- Full-wave rectifier
- No capacitive divider for side-chain filter needed
- Electronic switching for NR ON/OFF, B and C-type NR
- Dolby level 0 dB = –6 dBm (387,5 mV) offers line output level option of 0 dBm (775 mV)

TEA0654

- Electronic switching for playback/record
- Electronic switching for NR ON/OFF and B/C type NR
- No internal/external matching required for filter networks:
  only one network for spectral skewing and deskewing necessary; only one network for anti-saturation necessary
- Excellent matching between record and playback
- Line output (monitor) level externally set by resistor ratio independent of internal Dolby level
- Playback and record preamplifier and multiplex filter buffer amplifier included

## PACKAGE OUTLINES

TEA0651/TEA0652: 18-lead DIL; plastic (SOT-102HE).
TEA0654: 24-lead DIL; plastic (SOT-101A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Coporation.

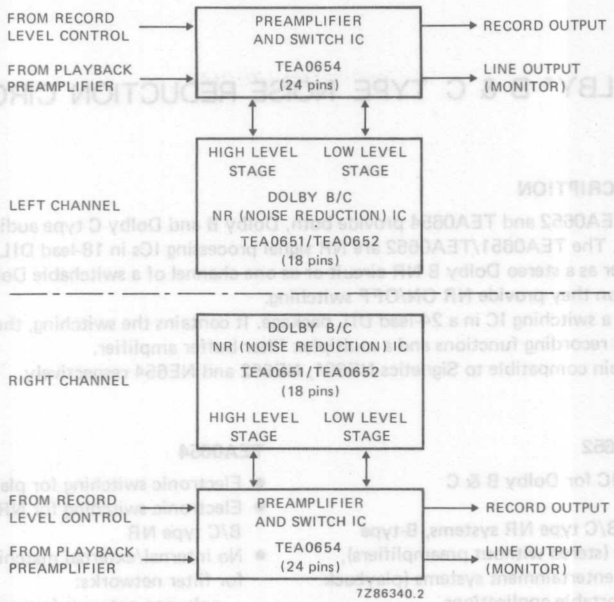
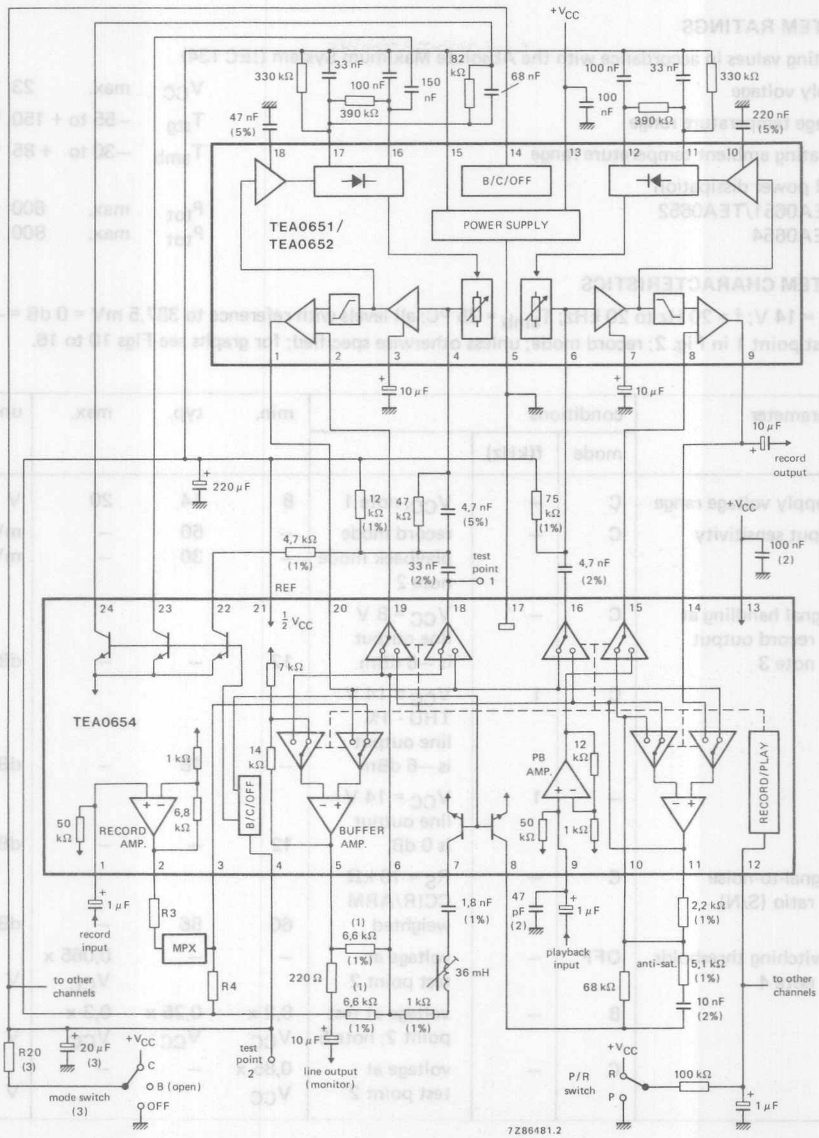



Fig. 1 System block diagram.

Switching levels; see Fig. 2.

| pin condition (test point 2) | functions switched for TEA0654 (pin 4) | functions switched for TEA0651/TEA0652 (pin 14) |
|---|---|---|
| + $V_{CC}$ | Dolby-C, open collector transistors at pins 7 and 8 switched on, at pins 22, 23, 24 switched off | Dolby-C |
| ½$V_{CC}$ | not applicable | stereo Dolby B, both channels active (Figs 15 and 16) |
| open (internally pulled to ¼$V_{CC}$) | Dolby-B, open collector transistors at pins 7 and 8 switched off, at pins 22, 23, 24 switched on | Dolby-B, low level stage side chain muted |
| ground | as pin condition 'open' | NR-OFF both side chains muted |



(1) Line output and record input programming resistors.
(2) Optional capacitors.
(3) Time constant for mode switch is optional, R20 is equal to 6,8 kΩ divided by number of switched channels.

Fig. 2 Dolby B/C NR system; switches shown in record position.

## SYSTEM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | max. | 23 | V |
| Storage temperature range | $T_{stg}$ | −55 to + 150 | | °C |
| Operating ambient temperature range | $T_{amb}$ | −30 to + 85 | | °C |
| Total power dissipation | | | | |
| TEA0651/TEA0652 | $P_{tot}$ | max. | 600 | mW |
| TEA0654 | $P_{tot}$ | max. | 800 | mW |

## SYSTEM CHARACTERISTICS

$V_{CC}$ = 14 V; f = 20 Hz to 20 kHz; $T_{amb}$ = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1 in Fig. 2; record mode; unless otherwise specified; for graphs see Figs 10 to 16.

| parameter | conditions: mode | conditions: f(kHz) | conditions | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| Supply voltage range | C | – | $V_{CC}$; note 1 | 8 | 14 | 20 | V |
| Input sensitivity | C | – | record mode | – | 50 | – | mV |
| | | | playback mode note 2 | – | 30 | – | mV |
| Signal handling at record output note 3 | C | – | $V_{CC}$ = 8 V line output is −6 dBm | 12 | – | – | dB |
| | C | 1 | $V_{CC}$ = 14 V THD - 1% line output is −6 dBm | – | 18 | – | dB |
| | – | 1 | $V_{CC}$ = 14 V line output is 0 dB, | 12 | – | – | dB |
| Signal-to-noise ratio (S/N) | C | – | $R_S$ = 10 kΩ CCIR/ARM weighted | 60 | 66 | – | dB |
| Switching thresholds note 4 | OFF | – | voltage at test point 2 | – | – | 0,065 x $V_{CC}$ | V |
| | B | – | voltage at test point 2; note 5 | 0,2 x $V_{CC}$ | 0,25 x $V_{CC}$ | 0,3 x $V_{CC}$ | V |
| | C | – | voltage at test point 2 | 0,85 x $V_{CC}$ | – | – | V |

## Notes to system characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 6 V.
2. Attenuation between pins 2 and 3 of TEA0654 is 4 dB;
3. System headroom is determined by programmable monitor output level (pin 5 of TEA0654).
4. For a typical application see Fig. 10. Worst case considerations for the $V_{CC}$ range from 8 V to 20 V limit the optional external resistor to maximum 6,8 kΩ, divided by number of switched channels.
5. In the open position (B) of the mode switch pin 14 of TEA0651/TEA0652 is pulled to typical 0,25 x $V_{CC}$ by pin 4 of TEA0654.

## SYSTEM GRAPHS

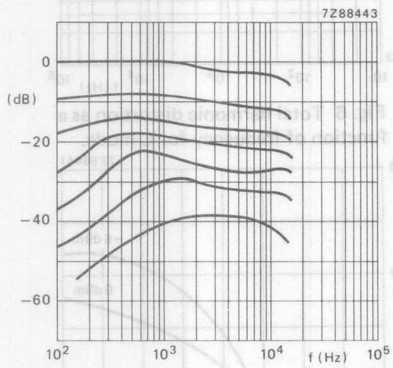



Fig. 3 Encoder frequency response for C-mode.

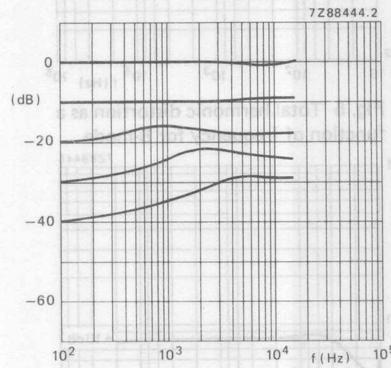



Fig. 4 Encoder frequency response for B-mode.

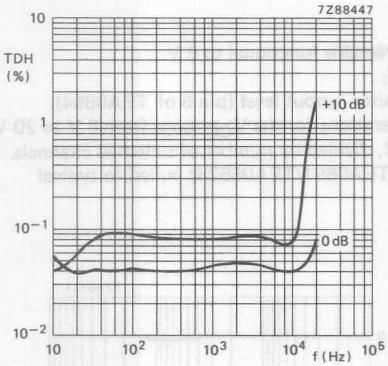



Fig. 5 Total harmonic distortion as a function of frequency for B-mode.

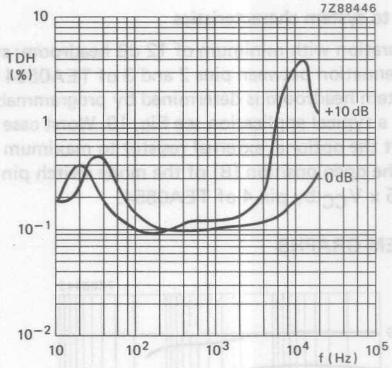



Fig. 6 Total harmonic distortion as a function of frequency for C-mode.

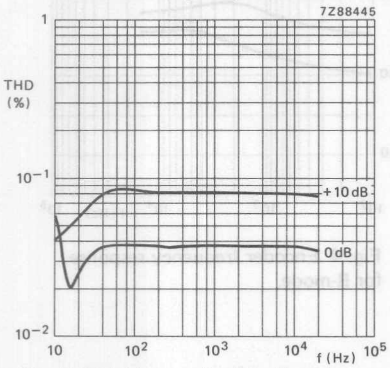



Fig. 7 Total harmonic distortion as a function of frequency for NR OFF-mode.

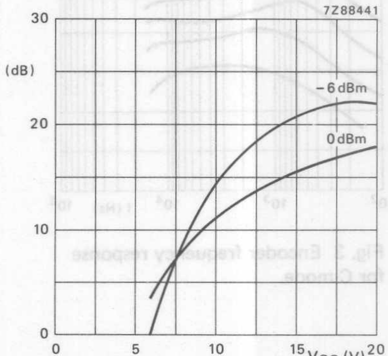



Fig. 8 Headroom at record output and line output (pins 14 and 5 of TEA0654); THD = 1%; f = 1 kHz, at line output levels 0 and −6 dB.

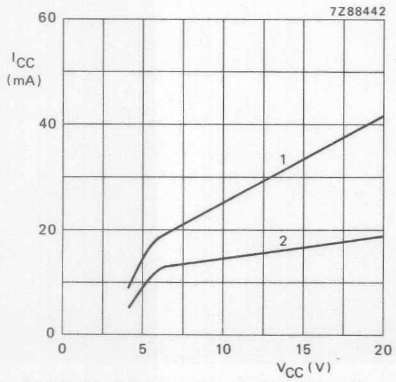



Fig. 9 Supply current as a function of supply voltage. 1: TEA0651/TEA0652 and TEA0654; 2: TEA0651/TEA0652 only.

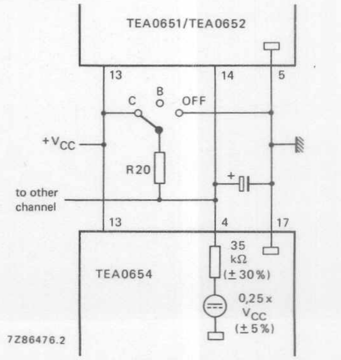



Fig. 10 Optional external time constant for mode switch.

## TEA0651/TEA0652: DOLBY B/C TYPE NOISE REDUCTION PROCESSING CIRCUITS

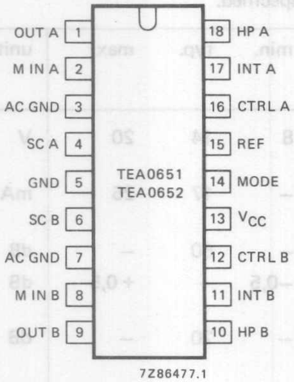



Fig. 11 Pinning diagram of TEA0651/TEA0652.

### PINNING

| | | |
|---|---|---|
| 1 | OUT A | output channel A |
| 2 | M IN A | main chain input channel A |
| 3 | AC GND | a.c. ground channel A |
| 4 | SC A | side chain channel A |
| 5 | GND | ground |
| 6 | SC B | side chain channel B |
| 7 | AC GND | a.c. ground channel B |
| 8 | M IN B | main chain input channel B |
| 9 | OUT B | output channel B |
| 10 | HP B | high-pass filter channel B |
| 11 | INT B | integrating filter channel B |
| 12 | CTRL B | control voltage channel B |
| 13 | $V_{CC}$ | positive supply voltage |
| 14 | MODE | mode B/C/NR OFF switch input |
| 15 | REF | reference voltage |
| 16 | CTRL A | control voltage channel A |
| 17 | INT A | integration filter channel A |
| 18 | HP A | high-pass filter channel A |

### Note

For Dolby-C type application channel A is the HIGH level stage and channel B is the LOW level stage.

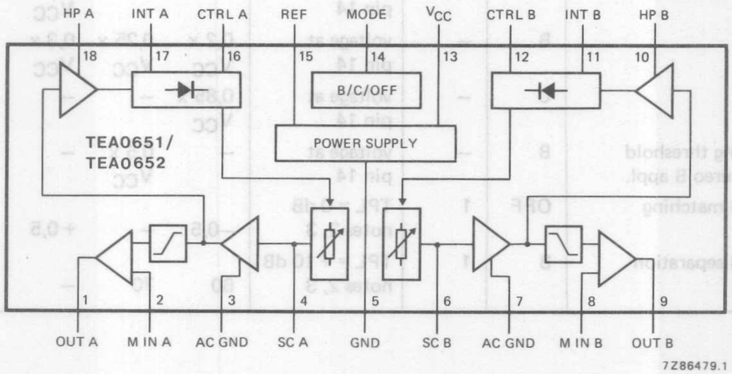



Fig. 12 Block diagram of TEA0651 and TEA0652.

## CHARACTERISTICS FOR TEA0651/TEA0652

$V_{CC}$ = 14 V; f = 20 Hz to 20 kHz; $T_{amb}$ = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1; test circuit Fig. 13; record mode; unless otherwise specified.

| parameter | conditions mode | conditions f(kHz) | conditions | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| Supply voltage range | B | – | $V_{CC}$ | 8 | 14 | 20 | V |
| Supply current $I_{CC}$ | OFF | – | no input signal | – | 17 | 25 | mA |
| Power supply ripple rejection ratio | B | 1 | test circuit Fig. 14 | – | 60 | – | dB |
| Voltage gain | OFF | 1 | note 1 | –0,5 | – | +0,5 | dB |
| Signal handling at record output (note 4) | B | 1 | $V_{CC}$ = 14 V THD = 1% | – | 20 | – | dB |
| | | 1 | $V_{CC}$ = 8 V THD = 1% | 12 | 14 | – | dB |
| | | 1 | $V_{CC}$ = 6 V THD = 1% | – | 11 | – | dB |
| Signal-to-noise ratio (S/N) | B | – | $R_S$ = 10 kΩ, internal CCIR/ARM weighted | – | 90 | – | dB |
| Switching thresholds | OFF | – | voltage at pin 14 | – | – | 0,065 x $V_{CC}$ | V |
| | B | – | voltage at pin 14 | 0,2 x $V_{CC}$ | 0,25 x $V_{CC}$ | 0,3 x $V_{CC}$ | V |
| | C | – | voltage at pin 14 | 0,85 x $V_{CC}$ | – | – | V |
| Switching threshold for stereo B appl. | B | – | voltage at pin 14 | – | 0,5 x $V_{CC}$ | – | V |
| Channel matching | OFF | 1 | TPL = 0 dB notes 2, 3 | –0,5 | – | +0,5 | dB |
| Channel separation | B | 1 | TPL = + 10 dB notes 2, 3 | 60 | 70 | – | dB |

**Notes**

1. Voltage gain is $20 \log \frac{\text{voltage at pin 1 (9)}}{\text{voltage at pin 2 (8)}}$.
2. TPL is Test Point Level.
3. Test circuit Fig. 15, reference level at channel A and channel B test point.
4. Operation with minimum of 12 dB headroom; system remains functional to 6 V.

## CHARACTERISTICS TEA0651 ONLY

| parameter | conditions | | | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| | mode | f(kHz) | | | | | |
| Offset voltage | C | – | $\|V_{9-15}\|$ | – | 3 | 6 | mV |
| Signal-to-noise ratio (S/N) | C | – | $R_S$ = 10 kΩ (internal) CCIR/ARM weighted; pin 9 | 77 | 80 | – | dB |
| Total harmonic distortion (THD) | B | 10 | TPL = 0 dB | – | – | 0,1 | % |
| | | – | TPL = + 10 dB | – | 0,05 | 0,1 | % |
| Total harmonic distortion (THD) | C | 10 | TPL = 0 dB | – | – | 0,1 | % |
| | | 1 | TPL = + 10 dB | – | 0,15 | 0,5 | % |
| B-mode frequency response | B | 1 | TPL = −20 dB | −17,3 | −15,8 | −14,3 | dB |
| | | 2 | TPL = −25 dB | −19,5 | −18,0 | −16,5 | dB |
| | | 5 | TPL = −40 dB | −30,2 | −29,7 | −28,2 | dB |
| | | 10 | TPL = −30 dB | −25,0 | −23,5 | −22,0 | dB |
| C-mode frequency response | C | 0,2 | TPL = −40 dB | −32,9 | −31,9 | −30,9 | dB |
| | | 0,5 | TPL = −20 dB | −14,2 | −13,7 | −13,2 | dB |
| | | 0,5 | TPL = −30 dB | −18,7 | −18,2 | −17,7 | dB |
| | | 1 | TPL = −20 dB | −14,6 | −14,1 | −13,6 | dB |
| | | 1 | TPL = −30 dB | −19,1 | −18,6 | −18,1 | dB |
| | | 1 | TPL = −40 dB | −25,3 | −23,8 | −22,3 | dB |
| | | 5 | TPL = 0 dB | −3,3 | −2,3 | −1,3 | dB |
| | | 5 | TPL = −20 dB | −18,1 | −17,1 | −16,1 | dB |
| | | 5 | TPL = −30 dB | −22,6 | −21,6 | −20,6 | dB |
| | | 5 | TPL = −40 dB | −28,0 | −26,5 | −25,0 | dB |

## CHARACTERISTICS TEA0652 ONLY

| parameter | conditions | | | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| | mode | f(kHz) | | | | | |
| Offset voltage | C | – | $\|V_{9-15}\|$ | – | 10 | – | mV |
| Signal-to-noise ratio (S/N) | C | – | $R_S$ = 10 kΩ (internal) CCIR/ARM weighted; pin 9 | 72 | 80 | – | dB |
| Total harmonic distortion (THD) | B | 10 | TPL = 0 dB | – | 0,05 | 0,1 | % |
| | | | TPL = + 10 dB | – | 0,08 | 0,3 | % |
| Total harmonic distortion (THD) | C | 10 | TPL = 0 dB | – | 0,1 | 0,3 | % |
| | | 1 | TPL = + 10 dB | – | 0,15 | 0,5 | % |
| B-mode frequency response | B | 1 | TPL = –20 dB | –17,3 | –15,8 | –14,3 | dB |
| | | 2 | TPL = –25 dB | –19,5 | –18,0 | –16,5 | dB |
| | | 5 | TPL = –40 dB | –30,2 | –29,7 | –28,2 | dB |
| | | 10 | TPL = –30 dB | –25,0 | –23,5 | –22,0 | dB |
| C-mode frequency response | C | 0,2 | TPL = –40 dB | –33,4 | –31,9 | –30,4 | dB |
| | | 0,5 | TPL = –20 dB | –15,7 | –13,7 | –11,7 | dB |
| | | 0,5 | TPL = –30 dB | –20,2 | –18,2 | –16,2 | dB |
| | | 1 | TPL = –20 dB | –16,1 | –14,1 | –12,1 | dB |
| | | 1 | TPL = –30 dB | –20,1 | –18,6 | –17,1 | dB |
| | | 1 | TPL = –40 dB | –25,8 | –23,8 | –21,8 | dB |
| | | 5 | TPL = 0 dB | –3,8 | –2,3 | –0,8 | dB |
| | | 5 | TPL = –20 dB | –19,1 | –17,1 | –15,1 | dB |
| | | 5 | TPL = –30 dB | –23,6 | –21,6 | –19,6 | dB |
| | | 5 | TPL = –40 dB | –28,5 | –26,5 | –24,5 | dB |

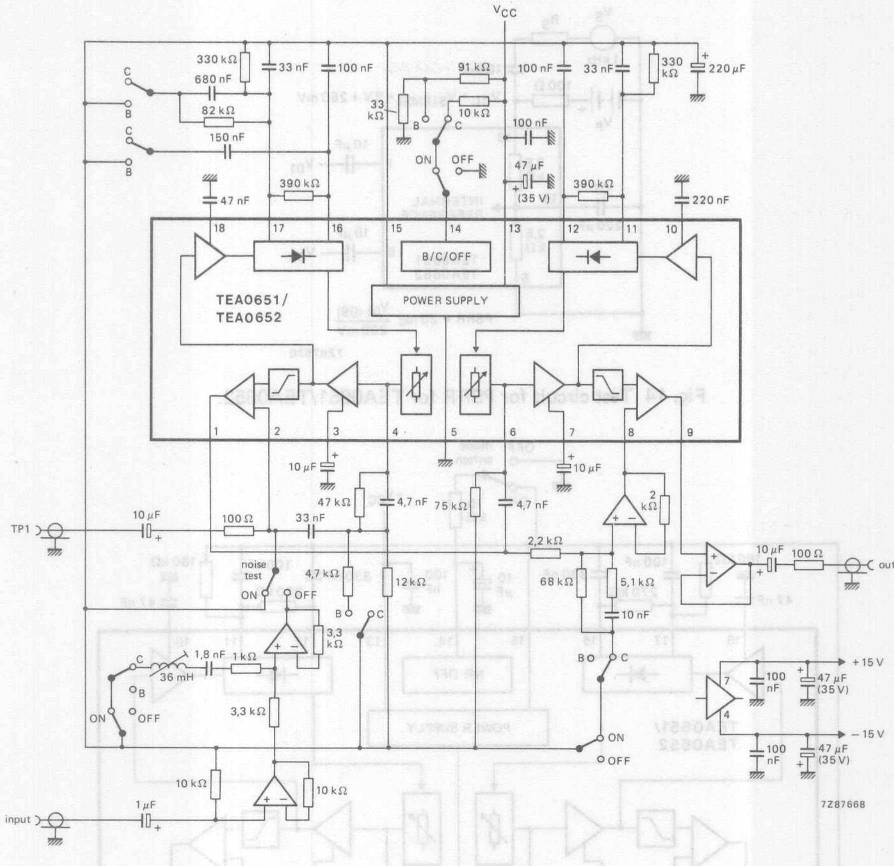



Fig. 13 Test circuit for TEA0651/0652. Encode mode.
Operational amplifiers are NE5535.

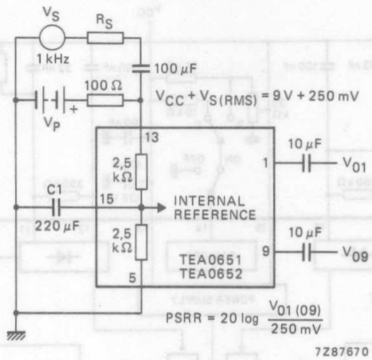



Fig. 14 Test circuit for PSRR for TEA0651/TEA0652.

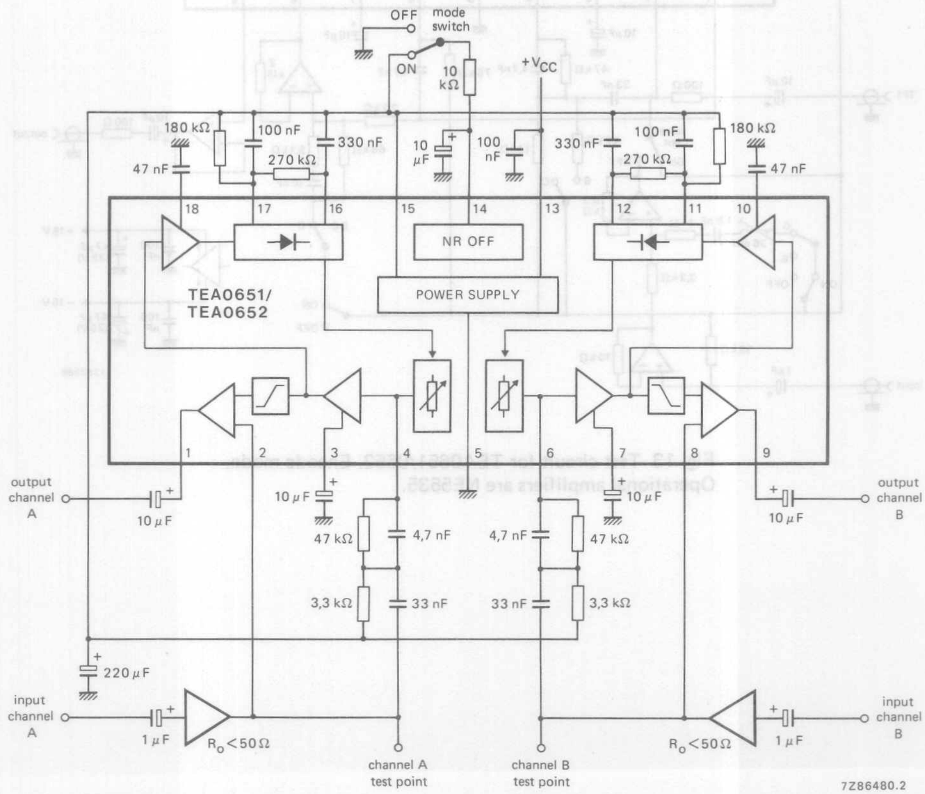



Fig. 15 Test and application circuit of TEA0651/TEA0652 for stereo Dolby B application, shown in encode mode.

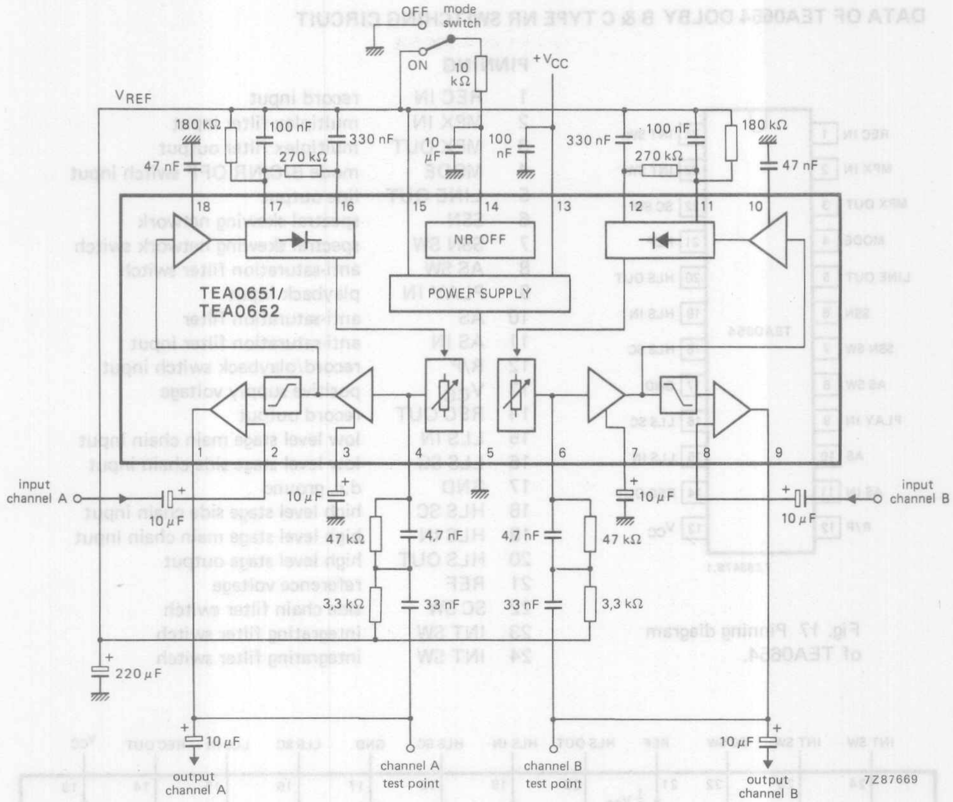



Fig. 16 Typical application circuit for stereo Dolby B noise reduction shown in decode mode.

## DATA OF TEA0654 DOLBY B & C TYPE NR SWITCHING CIRCUIT

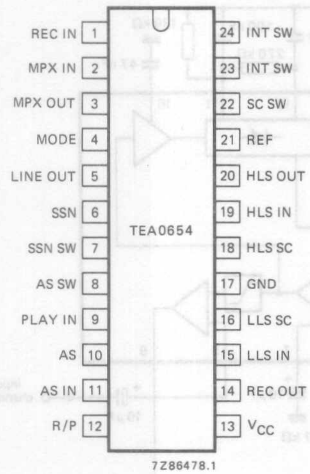



Fig. 17 Pinning diagram of TEA0654.

### PINNING

| | | |
|---|---|---|
| 1 | REC IN | record input |
| 2 | MPX IN | multiplex filter input |
| 3 | MPX OUT | multiplex filter output |
| 4 | MODE | mode B/C/NR OFF switch input |
| 5 | LINE OUT | line output |
| 6 | SSN | spectral skewing network |
| 7 | SSN SW | spectral skewing network switch |
| 8 | AS SW | anti-saturation filter switch |
| 9 | PLAY IN | playback input |
| 10 | AS | anti-saturation filter |
| 11 | AS IN | anti-saturation filter input |
| 12 | R/P | record/playback switch input |
| 13 | $V_{CC}$ | positive supply voltage |
| 14 | REC OUT | record output |
| 15 | LLS IN | low level stage main chain input |
| 16 | LLS SC | low level stage side chain input |
| 17 | GND | d.c. ground |
| 18 | HLS SC | high level stage side chain input |
| 19 | HLS IN | high level stage main chain input |
| 20 | HLS OUT | high level stage output |
| 21 | REF | reference voltage |
| 22 | SC SW | side chain filter switch |
| 23 | INT SW | integrating filter switch |
| 24 | INT SW | integrating filter switch |

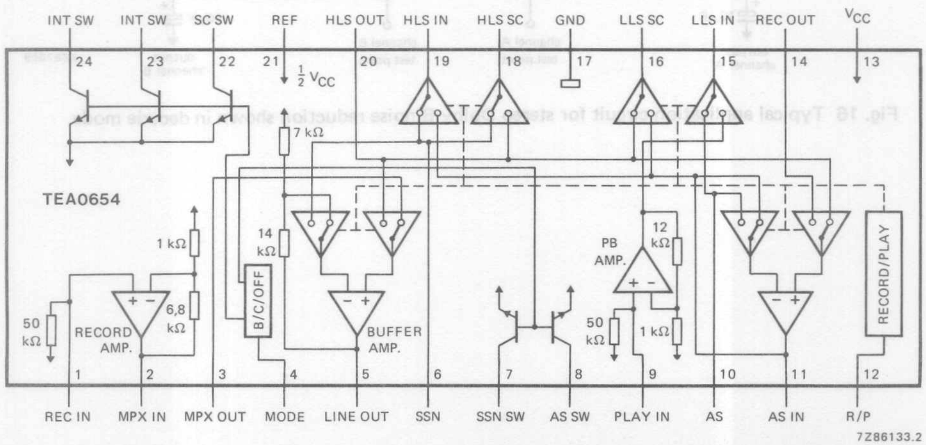



Fig. 18 Block diagram of TEA0654.

## CHARACTERISTICS FOR TEA0654

$V_{CC}$ = 14 V; f = 10 kHz; $T_{amb}$ = 25 °C; test circuit Fig. 20; signals referenced to REF (pin 21); d.c. levels with reference to GND (pin 17); unless otherwise specified.

| parameter | conditions | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ (output level at buffer amplifier is + 6 dBm; Dolby level is –6 dBm) | 8 | 14 | 20 | V |
| Supply current | $I_{CC}$ | 11 | 17 | 23 | mA |
| Voltage gain of record amplifier | pins 1 to 2 | – | 17,85 | – | dB |
| Input sensitivity of record amplifier (pin 1) | buffer amplifier output level (pin 5) is 775 mV r.m.s.; MPX filter insertion loss is 4 dB | 43 | 50 | 58 | mV |
| Voltage gain of playback amplifier | pins 9 to 5 | – | 22,25 | – | dB |
| Input sensitivity of playback amplifier | buffer amplifier output level (pin 5) is 775 mV r.m.s. | 25 | 30 | 35 | mV |
| Input resistance | pin 1 and 9 | 35 | 50 | 65 | kΩ |
| Output noise at record output pin 14 | $R_S$ = 10 kΩ at pin 1; CCIR/ARM weighted; record mode | – | 20 | 40 | μV |
| Signal handling record and buffer amplifier; pins 2 and 5 (r.m.s. value) | THD = 1%; record mode input level at pin 1 | 4 | – | – | V |
| Voltage gain of signal switches | record: pins 6 to 14 | – | 0 | – | dB |
| | playback: pins 14 to 20 | – | 0 | – | dB |
| Output noise at buffer amplifier pin 5 (r.m.s. value) | $R_S$ = 10 kΩ at pin 9; CCIR/ARM weighted; playback mode | – | 65 | 130 | μV |
| Voltage gain difference between main and side chain op-amp | main chain op-amp output: pins 19 and 15; side chain op-amp output: pins 18 and 16; adjacent op-amps: pins 19 and 18, pins 15 and 16 | –0,3 | 0 | + 0,3 | dB |
| Output noise of signal switches pins 11, 15, 16, 18, 19 | $R_S$ = 1 kΩ at pins 6, 14, 20; CCIR/ARM weighted; Fig. 19 | – | 2,5 | – | μV |
| Signal handling of switches (pin 14) (r.m.s. value) | THD = 1% at pin 14; input level at pin 1 | 2 | – | – | V |
| Voltage gain of buffer amplifier | pins 3 to 5 | – | 10 | – | dB |

| parameter | conditions | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Input noise of buffer amplifier pin 3 (r.m.s. value) | $R_S$ = 2,2 kΩ at pin 3; CCIR/ARM weighted; Fig. 19 | – | 2 | – | μV |
| Signal handling buffer amplifier pin 5 (r.m.s. value) | THD = 1% at pin 5; playback mode; input level at pin 9 | 4 | – | – | V |
| Output impedance at buffer amplifier pin 5 | | – | – | 100 | Ω |
| Load resistance at buffer amplifier pin 5 | | 10 | – | – | kΩ |
| Load capacitance at buffer amplifier pin 5 | For large capacitive loads a series resistor of about 220 Ω is necessary (see Fig. 2) | – | – | 200 | pF |
| D.C. switch control levels | playback: pin 12 | 0 | – | 1 | V |
| | record: pin 12 | $V_{CC}-1$ | – | $V_{CC}$ | V |
| | Dolby-C: pin 4 | $\frac{3}{4}V_{CC}+1$ | – | $V_{CC}$ | V |
| | Dolby-B: pin 4 | 0 | – | $\frac{3}{4}V_{CC}-1$ | V |

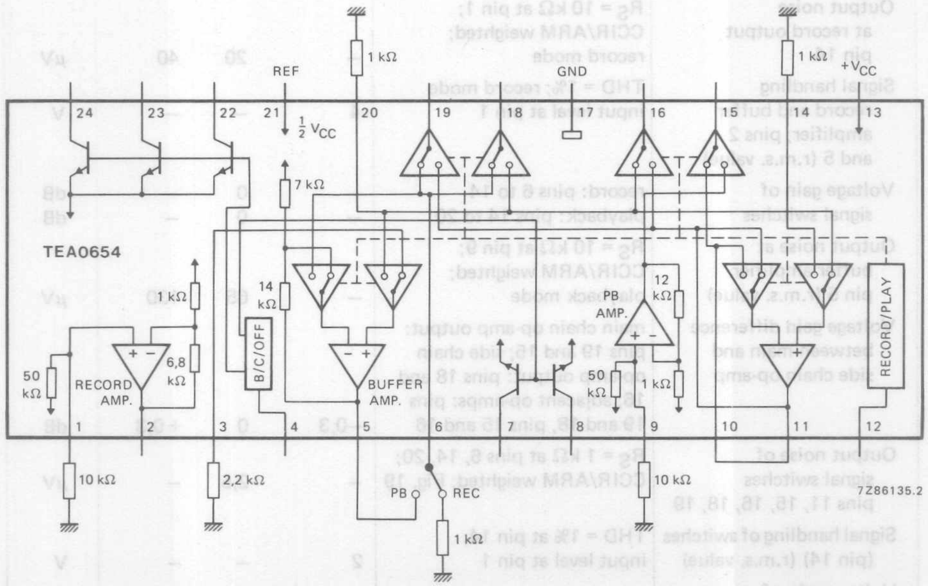



Fig. 19 Test circuit for noise measurements; switch in record position.

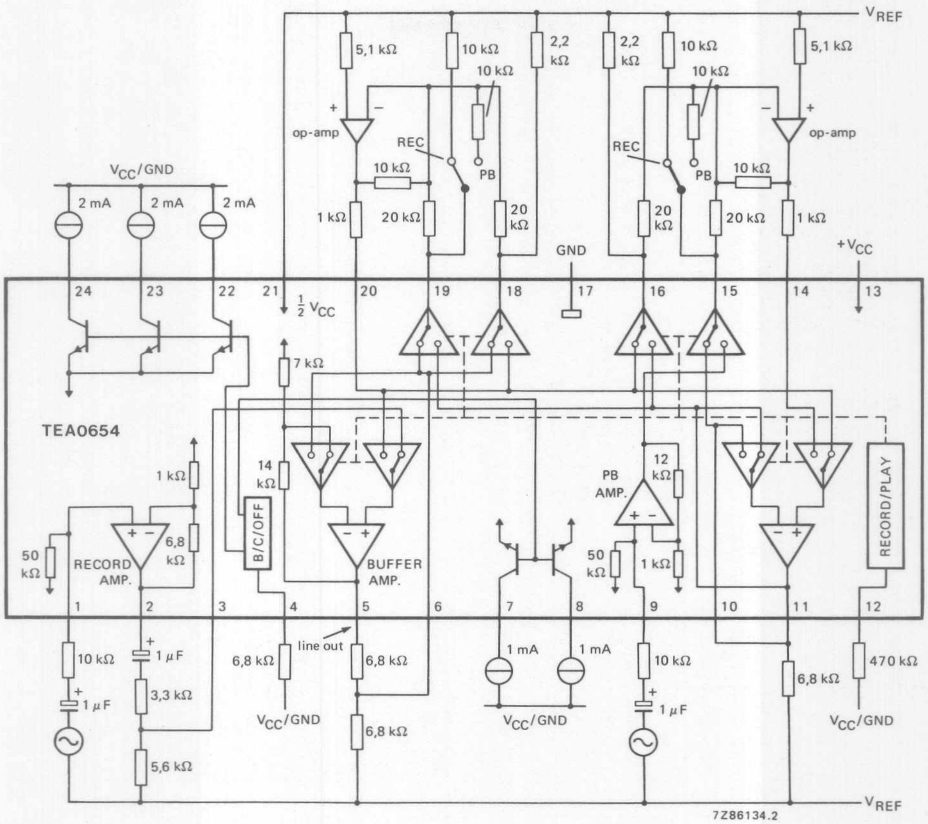



Fig. 20 Test circuit for $V_{CC} \geq 11,5$ V; switches in record position; external operational amplifier e.g. AD506LH.

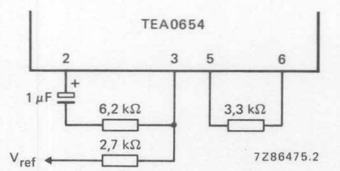



Fig. 21 Modification of Fig. 20 for $V_{CC} \leq 11,5$ V.

# DOLBY B TYPE NOISE REDUCTION CIRCUIT

## GENERAL DESCRIPTION

The TEA0653T is a monolithic bipolar IC designed for use in Dolby B type audio Noise Reduction (NR) systems. The device is a dual channel circuit.

### Applications

- Automotive cassette players
- Home cassette decks
- Portable cassette players
- Video cassette recorders
- FM receivers

### Features

- Dual processors provide optimum matching of channels
- No law adjustments required
- Full wave rectifier
- No capacitor required for side chain filter
- Electronic switching for NR ON/OFF
- Reference level 0 dB = 387,5 mV
- Minimum external components
- Easy to apply in 2 or 3 head systems
- Split supply operation is optional

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage | max. | 20 | V |
| Supply current | typ. | 17 | mA |
| Signal-to-noise ratio | typ. | 90 | dB |
| Storage temperature range | | −55 to +150 | °C |
| Operating ambient temperature range | | −30 to +85 | °C |

## PACKAGE OUTLINES

TEA0653T: 20-lead mini-pack; plastic (SOT-163A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Fancisco, CA94111, U.S.A., from whom licensing and application information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

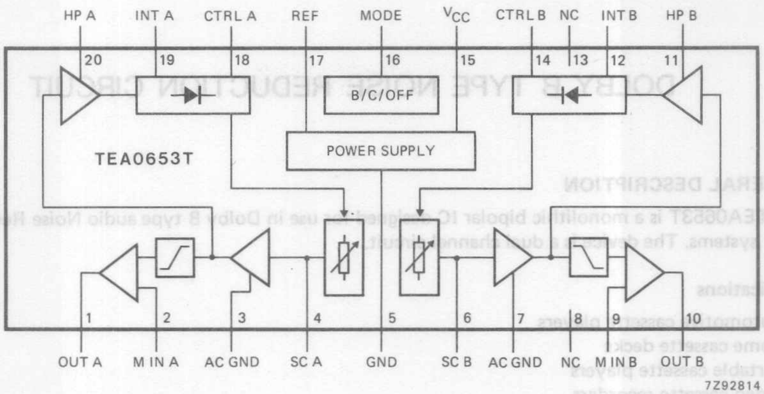



Fig. 1 Block diagram.

## PINNING

| | | |
|---|---|---|
| 1 | OUT A | output channel A |
| 2 | M IN A | main chain input channel A |
| 3 | AC GND | a.c. ground channel A |
| 4 | SC A | side chain channel A |
| 5 | GND | ground |
| 6 | SC B | side chain channel B |
| 7 | AC GND | a.c. ground channel B |
| 8 | N.C. | no connection |
| 9 | M IN B | main chain input channel B |
| 10 | OUT B | output channel B |
| 11 | HP B | high-pass filter channel B |
| 12 | INT B | integrating filter channel B |
| 13 | N.C. | no connection |
| 14 | CTRL B | control voltage channel B |
| 15 | $V_{CC}$ | positive supply voltage |
| 16 | MODE | mode B/NR OFF switch input |
| 17 | REF | reference voltage |
| 18 | CTRL A | control voltage channel A |
| 19 | INT A | integration filter channel A |
| 20 | HP A | high-pass filter channel A |

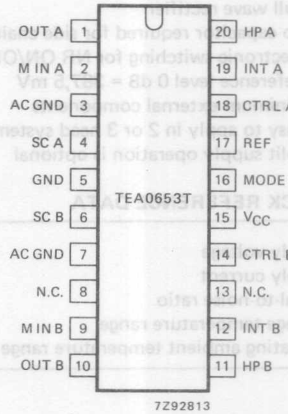



Fig. 2 Pinning diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| | | |
|---|---|---|
| Supply voltage pin 15 | $V_{CC}$ | 8 to 20 V |
| Storage temperature range | $T_{stg}$ | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | −30 to +85 °C |

## CHARACTERISTICS

$V_{CC}$ = 14 V; f = 20 Hz to 15 kHz; $T_{amb}$ = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point A or B; test circuit Fig. 4; encode mode; unless otherwise specified.

| parameter | conditions | | | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| | mode | f(kHz) | | | | | |
| **Supply** | | | | | | | |
| Supply voltage range | B | – | $V_{CC}$ (note 4) | 8 | 14 | 20 | V |
| Supply current $I_{CC}$ | OFF | – | no input signal | – | 17 | 25 | mA |
| Power supply ripple rejection ratio | B | 1 | test circuit Fig. 3 | – | 60 | | dB |
| Voltage gain | OFF | 1 | note 1 | −0,5 | – | +0,5 | dB |
| Signal handling at output (note 4) | B | 1 | $V_{CC}$ = 14 V THD = 1% | – | 20 | – | dB |
| | | 1 | $V_{CC}$ = 8 V THD = 1% | 12 | 14 | – | dB |
| | | 1 | $V_{CC}$ = 6 V THD = 1% | – | 11 | – | dB |
| Signal-to-noise ratio (S/N) | B | – | $R_S$ = 10 kΩ internal CCIR/ARM weighted | – | 90 | – | dB |
| Switching thresholds | OFF | – | voltage at pin 16 | – | – | 0,065 $\times V_{CC}$ | V |
| Switching threshold for stereo B appl. | B | – | voltage at pin 16 | – | 0,5 $\times V_{CC}$ | – | V |
| Channel matching | OFF | – | TPL = 0 dB notes 2, 3 | −0,5 | – | +0,5 | dB |
| Channel separation | B | 1 | TPL = 10 dB notes 2, 3 | 60 | 70 | – | dB |

DEVELOPMENT DATA

**CHARACTERISTICS** (continued)

| parameter | conditions | | | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|
| | mode | f(kHz) | | | | | |
| Total harmonic distortion (THD) | B | 10 | TPL = 0 dB | – | 0,05 | 0,1 | % |
| | | | TPL = +10 dB | – | 0,08 | 0,3 | % |
| B-mode frequency response | B | 1 | TPL = −20 dB | −17,3 | −15,8 | −14,3 | dB |
| | | 2 | TPL = −25 dB | −19,5 | −18,0 | −16,5 | dB |
| | | 5 | TPL = −40 dB | −30,2 | −29,7 | −28,2 | dB |
| | | 10 | TPL = −30 dB | −25,0 | −23,5 | −22,0 | dB |

**Notes**

1. Voltage gain is $20 \log \frac{\text{voltage at pin 1 (10)}}{\text{voltage at pin 2 (9)}}$
2. TPL is Test Point Level.
3. Test circuit Fig. 3, reference level at channel A and channel B test point.
4. Operation with minimum of 12 dB headroom; system remains functional to 6 V.

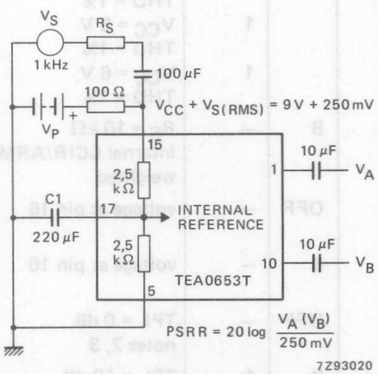



Fig. 3 Test circuit for PSSR for TEA0653T.

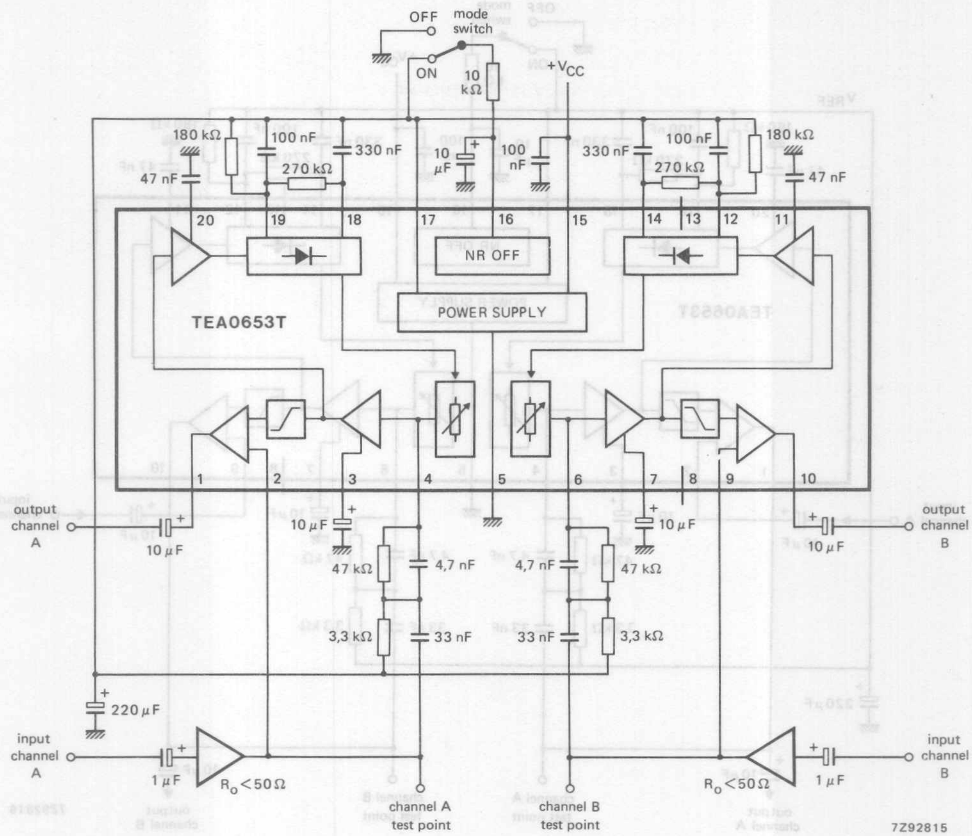



Fig. 4 Test and application circuit for stereo Dolby B, shown in encode mode.

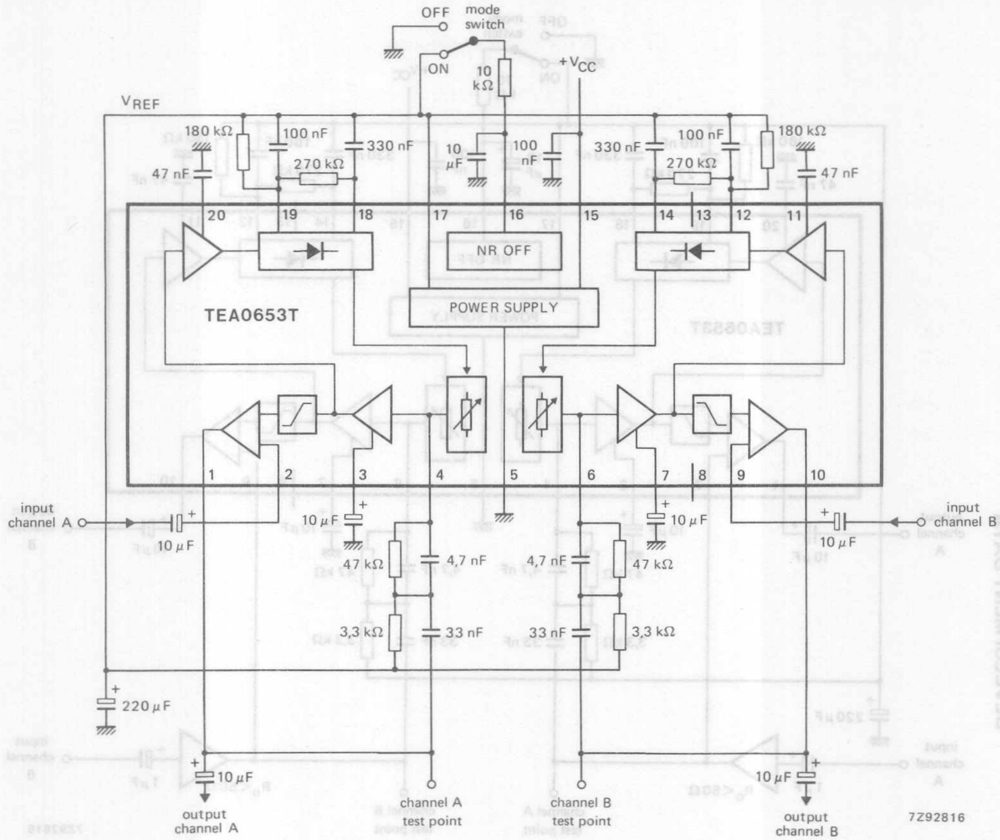



Fig. 5 Application circuit for stereo Dolby B, shown in decode mode.

# DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

## GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

### Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

## PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT-117).
TEA0665T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

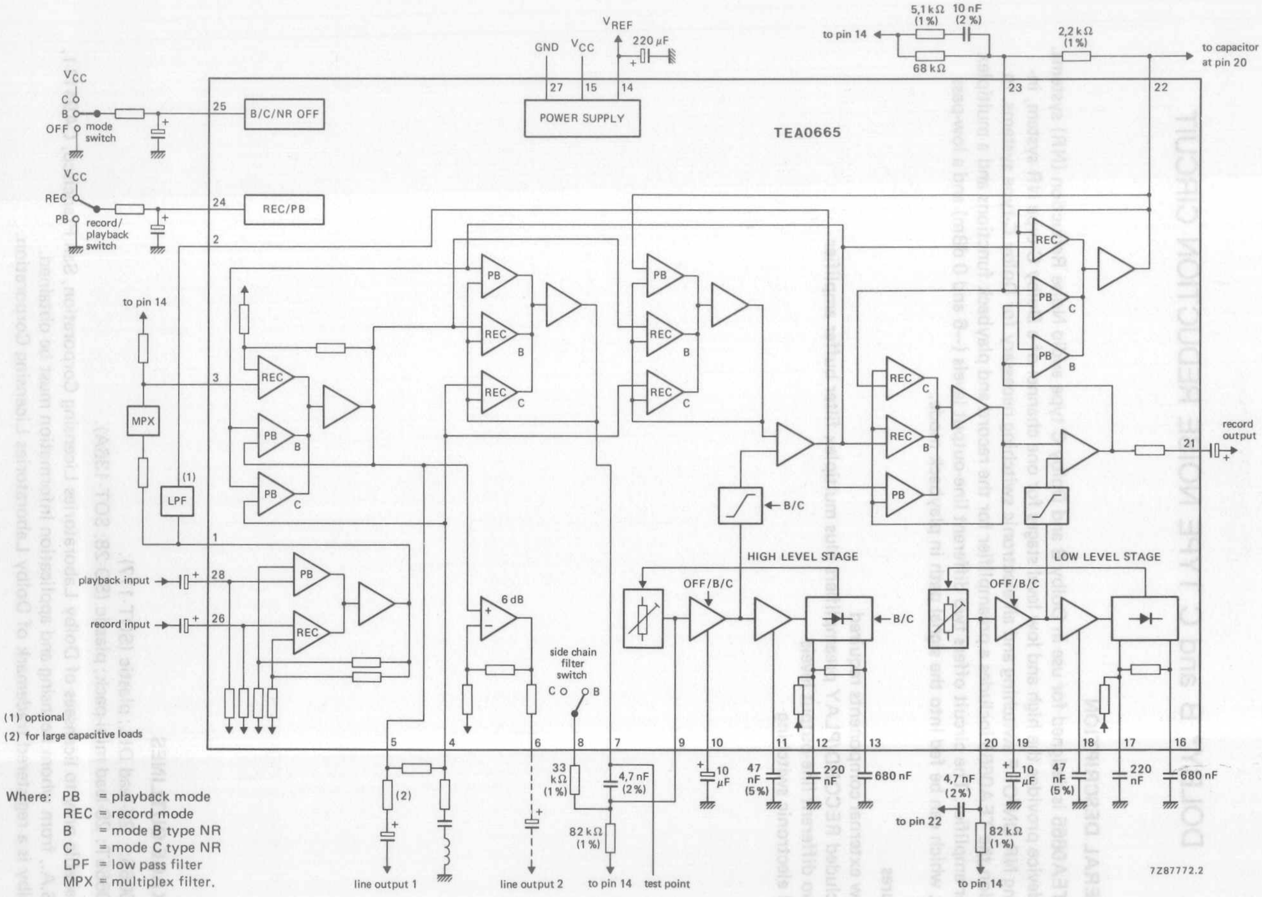



Fig. 1 Block diagram and application circuit.

DEVELOPMENT DATA

## PINNING

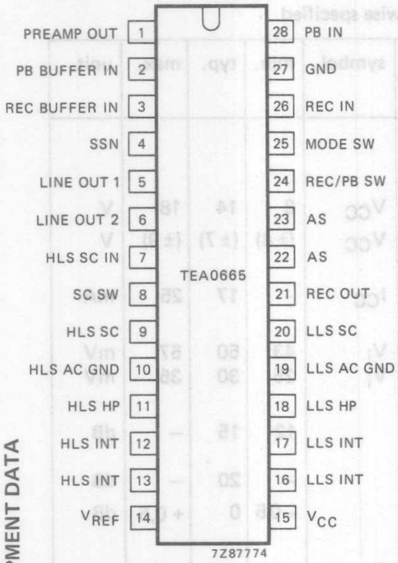



Fig. 2 Pinning diagram.

| | | |
|---|---|---|
| 1 | PREAMP OUT | record/playback preamplifier output |
| 2 | PB BUFFER IN | playback amplifier input buffer |
| 3 | REC BUFFER IN | record amplifier input buffer |
| 4 | SSN | spectral skewing network |
| 5 | LINE OUT 1 | line output 1 |
| 6 | LINE OUT 2 | line output 2 |
| 7 | HLS SC IN | high level stage side chain input |
| 8 | SC SW | side chain filter switch |
| 9 | HLS SC | high level stage side chain |
| 10 | HLS AC GND | high level stage a.c. ground |
| 11 | HLS HP | high level stage high pass filter |
| 12 | HLS INT | high level stage integrating filter |
| 13 | HLS INT | high level stage integrating filter |
| 14 | $V_{REF}$ | reference voltage |
| 15 | $V_{CC}$ | positive supply voltage |
| 16 | LLS INT | low level stage integrating filter |
| 17 | LLS INT | low level stage integrating filter |
| 18 | LLS HP | low level stage high pass filter |
| 19 | LLS AC GND | low level stage a.c. ground |
| 20 | LLS SC | low level stage side chain |
| 21 | REC OUT | record output |
| 22 | AS | anti-saturation filter |
| 23 | AS | anti-saturation filter |
| 24 | REC/PB SW | record/playback switch input |
| 25 | MODE SW | mode switch input |
| 26 | REC IN | record input |
| 27 | GND | ground |
| 28 | PB IN | playback input |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 15) | $V_{CC}$ | max. | 20 | V |
| Input voltage (pins 26 and 28) | $V_I$ | max. | $-0{,}3$ to $V_{CC}$ | V |
| Total power dissipation | $P_{tot}$ | | 600 | mW |
| Storage temperature range | $T_{stg}$ | | $-55$ to $+150$ | $^{o}C$ |
| Operating ambient temperature range | $T_{amb}$ | | $-40$ to $+85$ | $^{o}C$ |

## CHARACTERISTICS

$V_{CC}$ = 14 V; f = 20 Hz to 15 kHz; $T_{amb}$ = 25 °C; all levels with reference to 387,5 mV = 0 dB = –6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

| parameter | conditions mode | f (kHz) | | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | | |
| Supply voltage range | C | – | note 1 | | | | | |
| single | | | | $V_{CC}$ | 8 | 14 | 18 | V |
| (split) | | | | $V_{CC}$ | (± 4) | (± 7) | (± 9) | V |
| Supply current | OFF | – | no input signal | $I_{CC}$ | – | 17 | 25 | mA |
| Input sensitivity | C | | note 2 | | | | | |
| of record amplifier | | | pin 26 | $V_i$ | 43 | 50 | 57 | mV |
| of playback amplifier | | | pin 28 | $V_i$ | 25 | 30 | 35 | mV |
| Signal handling of record output (note 3; see Fig. 8) | C | 1 | $V_{CC}$ = 8 V THD = 1% | | 12 | 15 | – | dB |
| | | 1 | $V_{CC}$ = 14 V THD = 1% | | – | 20 | – | dB |
| Line output 1 | | | note 3 | | –0,5 | 0 | + 0,5 | dB |
| Line output 2; amplifier gain $V_o/V_i$ (pin 6 to pin 5) | | | | $G_v$ | + 5,5 | + 6 | + 6,5 | dB |
| Total harmonic distortion | OFF | 1 | TPL = 0 dB* | THD | – | 0,02 | 0,1 | % |
| | | | TPL = + 10 dB | THD | – | 0,05 | 0,3 | % |
| Total harmonic distortion | B | 1 | TPL = 0 dB | THD | – | 0,1 | 0,15 | % |
| | | | TPL = + 10 dB | THD | – | 0,08 | 0,3 | % |
| | | 10 | TPL = 0 dB | THD | – | 0,06 | 0,1 | % |
| Total harmonic distortion | C | 1 | TPL = 0 dB | THD | – | 0,15 | 0,3 | % |
| | | | TPL = + 10 dB | THD | – | 0,13 | 0,5 | % |
| Signal-to-noise ratio | C | | $R_S$ = 10 kΩ CCIR/ARM weighted | S/N | 62 | 66 | – | dB |

* TPL is Test Point Level.

| parameter | conditions | | | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|---|
| | mode | f (kHz) | | | | | | |
| Frequency response | B | 2 | TPL = −25 dB | | −19,0 | −18,0 | −17,0 | dB |
| | | 5 | TPL = −40 dB | | −30,7 | −29,7 | 28,7 | dB |
| | | 10 | TPL = −30 dB | | −24,5 | −23,5 | −22,5 | dB |
| | C | 0,2 | TPL = −40 dB | | −33,4 | −31,9 | 30,4 | dB |
| | | 1 | TPL = −30 dB | | −20,1 | −18,6 | −17,1 | dB |
| | | 1 | TPL = −20 dB | | −16,1 | −14,1 | −12,1 | dB |
| | | 5 | TPL = −0 dB | | −3,8 | −2,3 | −0,8 | dB |
| | | 5 | TPL = −20 dB | | −19,1 | −17,1 | −15,1 | dB |
| | | 5 | TPL = −40 dB | | −28,5 | −26,5 | −24,5 | dB |
| Switching thresholds | | | note 4; pin 24 | | | | | |
| for record | | | | $V_{24\text{-}27}$ | 8,5 | – | 14 | V |
| for playback | | | | $V_{24\text{-}27}$ | 0 | – | 4 | V |
| Switching thresholds | | | note 5; pin 25 | | | | | |
| | OFF | | | $V_{25\text{-}27}$ | 0 | – | 3,5 | V |
| (switch in open position) | B | | | $V_{25\text{-}27}$ | – | 7 | – | V |
| (external voltage) | B | | | $V_{25\text{-}27}$ | 6,3 | 7 | 7,7 | V |
| | C | | | $V_{25\text{-}27}$ | 10,8 | – | 14 | V |
| Switch input current | | | pin 25 | | | | | |
| | OFF | | $V_{25\text{-}27} = 0$ V | $-I_{25}$ | – | – | 40 | μA |
| | C | | $V_{25\text{-}27} = V_{CC}$ | $I_{25}$ | – | – | 40 | μA |
| Frequency response shift | C | | | | | | | |
| as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C | | | | Δf | – | ± 0,5 | – | dB |
| as a function of voltage deviation, range 8 to 18 V, measured as deviation from 14 V | | | | Δf | – | ± 0,1 | | dB |
| Input resistance | | | | | | | | |
| | | | pin 26 | $R_{26\text{-}27}$ | 35 | 50 | 65 | kΩ |
| | | | pin 28 | $R_{28\text{-}27}$ | 35 | 50 | 65 | kΩ |
| Output resistance | | | | | | | | |
| | | | pin 6 | $R_{6\text{-}27}$ | – | 160 | 220 | Ω |
| | | | pin 21 | $R_{21\text{-}27}$ | – | 60 | 100 | Ω |

DEVELOPMENT DATA

**Notes to the characteristics**

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

   The voltage drop across the external time constant resistor must be taken in to account.

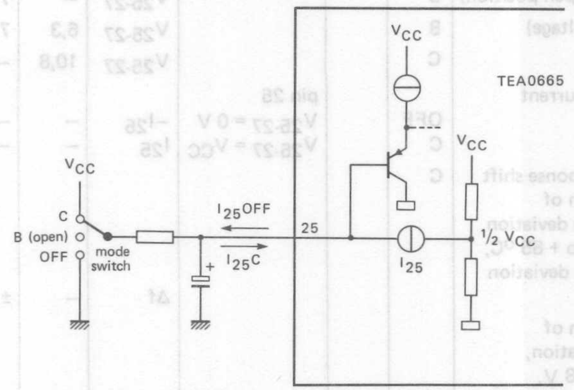



Fig. 3 Mode switch input configuration.

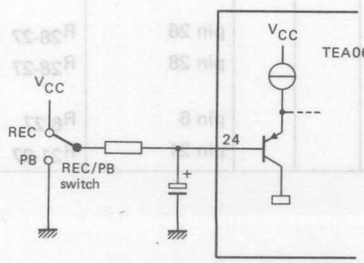
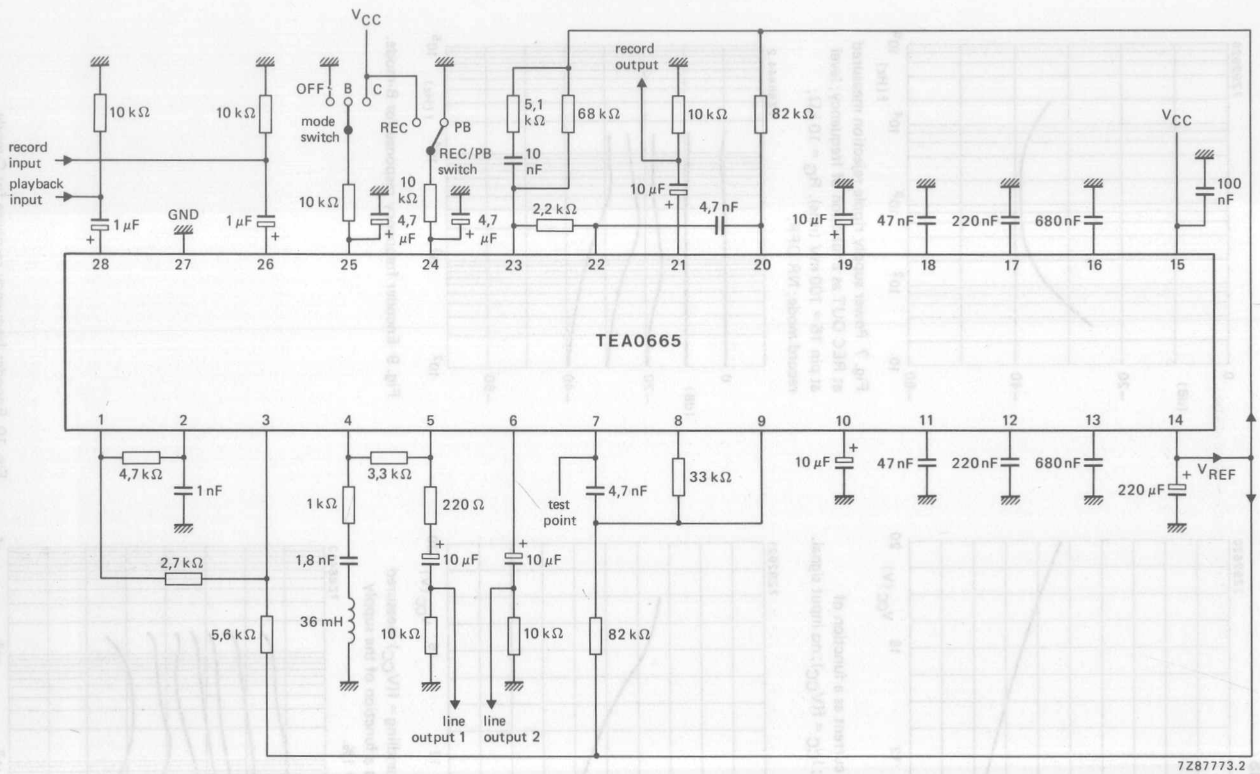



Fig. 4 REC/PB switch input configuration.




REC = record mode
PB = playback mode

Tolerances: resistors 1%
capacitors 1%

Fig. 5 Test circuit.

## SYSTEM GRAPHS

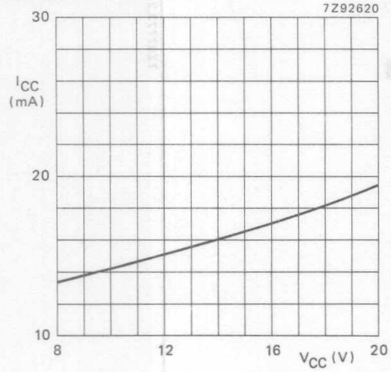



Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

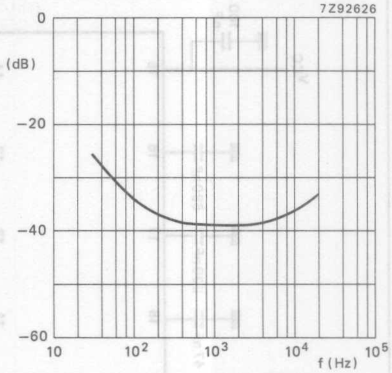



Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). $R_G = 10\ k\Omega$; record mode; NR OFF.

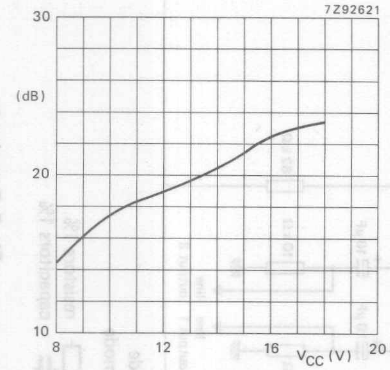



Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

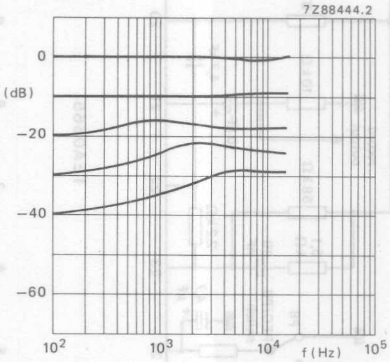



Fig. 9 Encoder frequency response for B-mode.

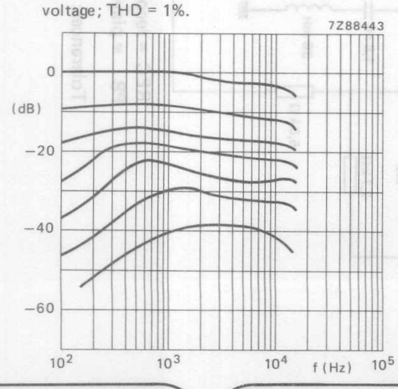



Fig. 10 Encoder frequency response for C-mode.

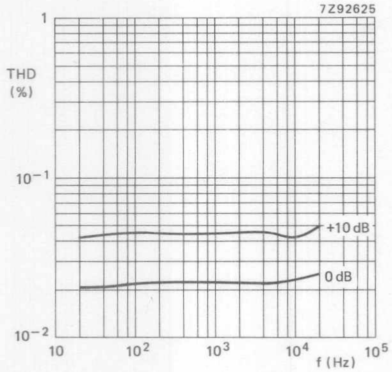



Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; $V_{CC}$ = 14 V; LPF 80 kHz.

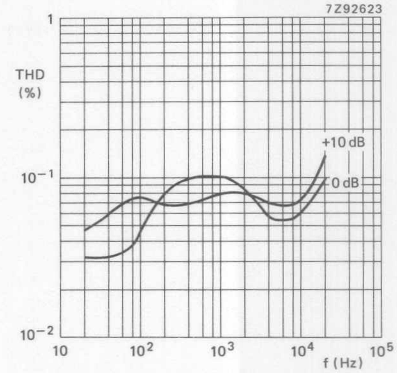



Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

DEVELOPMENT DATA

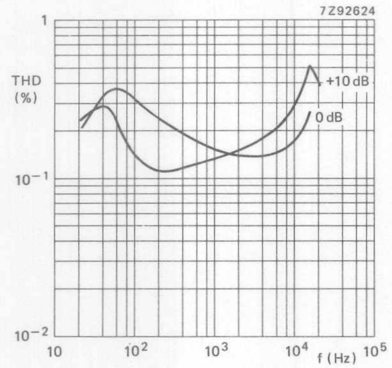



Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

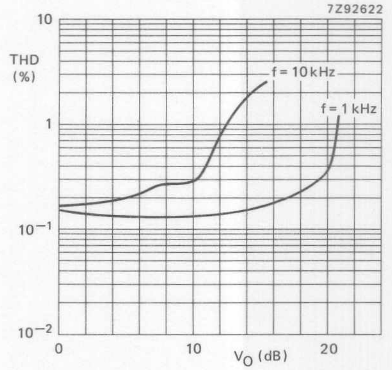



Fig. 14 Total harmonic distortion as a function of the record output level (pin21); for C-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

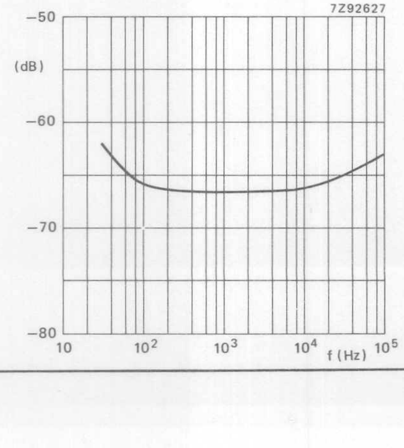



Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; $R_G$ = 10 kΩ.

# DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

## GENERAL DESCRIPTION

The TEA0666 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0666 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

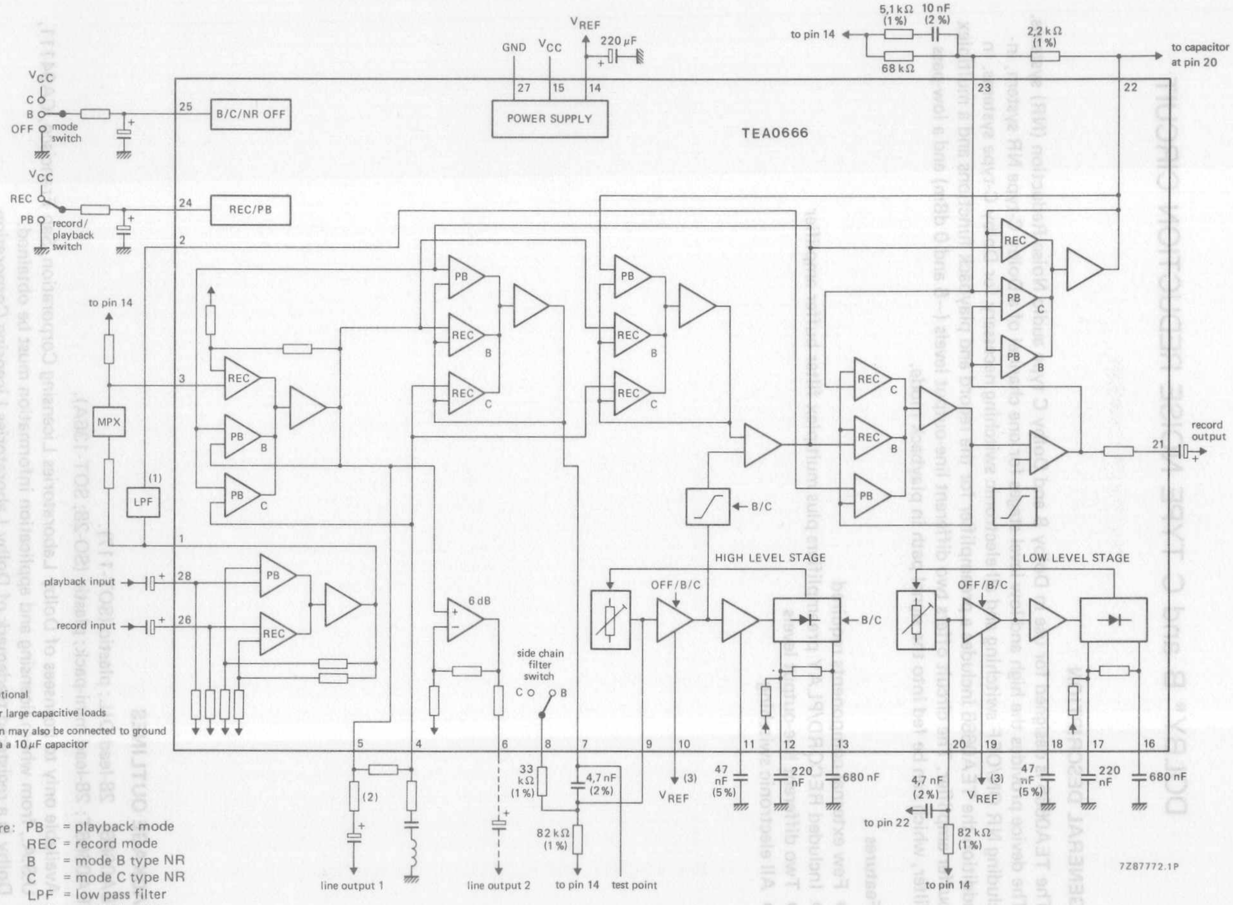
### Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

## PACKAGE OUTLINES

TEA0666: 28-lead DIL; plastic (SOT-117).
TEA0666T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.




(1) optional
(2) for large capacitive loads
(3) pin may also be connected to ground via a 10 μF capacitor

Where: PB = playback mode
REC = record mode
B = mode B type NR
C = mode C type NR
LPF = low pass filter
MPX = multiplex filter.

Fig. 1 Block diagram and application circuit.

## PINNING

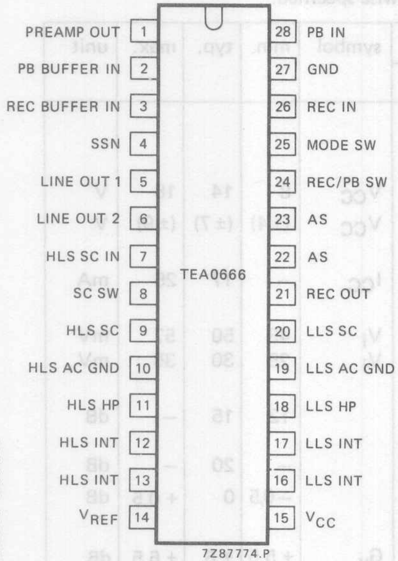



Fig. 2 Pinning diagram.

| | | |
|---|---|---|
| 1 | PREAMP OUT | record/playback preamplifier output |
| 2 | PB BUFFER IN | playback amplifier input buffer |
| 3 | REC BUFFER IN | record amplifier input buffer |
| 4 | SSN | spectral skewing network |
| 5 | LINE OUT 1 | line output 1 |
| 6 | LINE OUT 2 | line output 2 |
| 7 | HLS SC IN | high level stage side chain input |
| 8 | SC SW | side chain filter switch |
| 9 | HLS SC | high level stage side chain |
| 10 | HLS AC GND | high level stage a.c. ground |
| 11 | HLS HP | high level stage high pass filter |
| 12 | HLS INT | high level stage integrating filter |
| 13 | HLS INT | high level stage integrating filter |
| 14 | $V_{REF}$ | reference voltage |
| 15 | $V_{CC}$ | positive supply voltage |
| 16 | LLS INT | low level stage integrating filter |
| 17 | LLS INT | low level stage integrating filter |
| 18 | LLS HP | low level stage high pass filter |
| 19 | LLS AC GND | low level stage a.c. ground |
| 20 | LLS SC | low level stage side chain |
| 21 | REC OUT | record output |
| 22 | AS | anti-saturation filter |
| 23 | AS | anti-saturation filter |
| 24 | REC/PB SW | record/playback switch input |
| 25 | MODE SW | mode switch input |
| 26 | REC IN | record input |
| 27 | GND | ground |
| 28 | PB IN | playback input |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 15) | $V_{CC}$ | max. | 20 | V |
| Input voltage (pins 26 and 28) | $V_I$ | max. | −0,3 to $V_{CC}$ | V |
| Total power dissipation | $P_{tot}$ | | 600 | mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −40 to + 85 | °C |

## CHARACTERISTICS

$V_{CC}$ = 14 V; f = 20 Hz to 15 kHz; $T_{amb}$ = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

| parameter | conditions | | | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|---|
| | mode | f (kHz) | | | | | | |
| **Supply** | | | | | | | | |
| Supply voltage range | C | – | note 1 | | | | | |
| single | | | | $V_{CC}$ | 8 | 14 | 18 | V |
| (split) | | | | $V_{CC}$ | (± 4) | (± 7) | (± 9) | V |
| Supply current | OFF | – | no input signal | $I_{CC}$ | – | 17 | 25 | mA |
| Input sensitivity | C | | note 2 | | | | | |
| of record amplifier | | | pin 26 | $V_i$ | 43 | 50 | 57 | mV |
| of playback amplifier | | | pin 28 | $V_i$ | 25 | 30 | 35 | mV |
| Signal handling of record output (note 3; see Fig. 8) | C | 1 | $V_{CC}$ = 8 V THD = 1% | | 12 | 15 | – | dB |
| | | 1 | $V_{CC}$ = 14 V THD = 1% | | – | 20 | – | dB |
| Line output 1 | | | note 3 | | −0,5 | 0 | + 0,5 | dB |
| Line output 2; amplifier gain $V_o/V_i$ (pin 6 to pin 5) | | | | $G_v$ | + 5,5 | + 6 | + 6,5 | dB |
| Total harmonic distortion | OFF | 1 | TPL = 0 dB* | THD | – | 0,02 | 0,1 | % |
| | | | TPL = + 10 dB | THD | – | 0,05 | 0,3 | % |
| Total harmonic distortion | B | 1 | TPL = 0 dB | THD | – | 0,1 | 0,15 | % |
| | | | TPL = + 10 dB | THD | – | 0,08 | 0,3 | % |
| | | 10 | TPL = 0 dB | THD | – | 0,06 | 0,1 | % |
| Total harmonic distortion | C | 1 | TPL = 0 dB | THD | – | 0,15 | 0,3 | % |
| | | | TPL = + 10 dB | THD | – | 0,13 | 0,5 | % |
| Signal-to-noise ratio | C | | $R_S$ = 10 kΩ CCIR/ARM weighted | S/N | 62 | 66 | – | dB |

* TPL is Test Point Level.

| parameter | conditions mode | f (kHz) | | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|---|---|
| Frequency response | B | 2 | TPL = −25 dB | | −18,7 | −18,0 | −17,3 | dB |
| | | 5 | TPL = −40 dB | | −30,4 | −29,7 | −29,0 | dB |
| | | 10 | TPL = −30 dB | | −24,2 | −23,5 | −22,8 | dB |
| | C | 0,2 | TPL = −40 dB | | −32,9 | −31,9 | −30,9 | dB |
| | | 1 | TPL = −30 dB | | −19,3 | −18,6 | −17,9 | dB |
| | | 1 | TPL = −20 dB | | −14,8 | −14,1 | −13,4 | dB |
| | | 5 | TPL = −0 dB | | −2,8 | −2,3 | −1,8 | dB |
| | | 5 | TPL = −20 dB | | −17,8 | −17,1 | −16,4 | dB |
| | | 5 | TPL = −40 dB | | −27,0 | −26,5 | −26,0 | dB |
| Switching thresholds | | | note 4; pin 24 | | | | | |
| for record | | | | $V_{24\text{-}27}$ | 8,5 | – | 14 | V |
| for playback | | | | $V_{24\text{-}27}$ | 0 | – | 4 | V |
| Switching thresholds | | | note 5; pin 25 | | | | | |
| | OFF | | | $V_{25\text{-}27}$ | 0 | – | 3,5 | V |
| (switch in open position) | B | | | $V_{25\text{-}27}$ | – | 7 | – | V |
| (external voltage) | B | | | $V_{25\text{-}27}$ | 6,3 | 7 | 7,7 | V |
| | C | | | $V_{25\text{-}27}$ | 10,8 | – | 14 | V |
| Switch input current | | | pin 25 | | | | | |
| | OFF | | $V_{25\text{-}27}$ = 0 V | $-I_{25}$ | – | – | 40 | µA |
| | C | | $V_{25\text{-}27} = V_{CC}$ | $I_{25}$ | – | – | 40 | µA |
| Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C | C | | | Δf | – | ± 0,5 | – | dB |
| as a function of voltage deviation, range 8 to 18 V, measured as deviation from 14 V | | | | Δf | – | ± 0,1 | | dB |
| Input resistance | | | pin 26 | $R_{26\text{-}27}$ | 35 | 50 | 65 | kΩ |
| | | | pin 28 | $R_{28\text{-}27}$ | 35 | 50 | 65 | kΩ |
| Output resistance | | | pin 6 | $R_{6\text{-}27}$ | – | 160 | 220 | Ω |
| | | | pin 21 | $R_{21\text{-}27}$ | – | 60 | 100 | Ω |

DEVELOPMENT DATA

**Notes to the characteristics**

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:
   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,
   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:
   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,
   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),
   B: $0{,}5\ V_{CC}$ (switch in open position),
   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.
   The voltage drop across the external time constant resistor must be taken in to account.

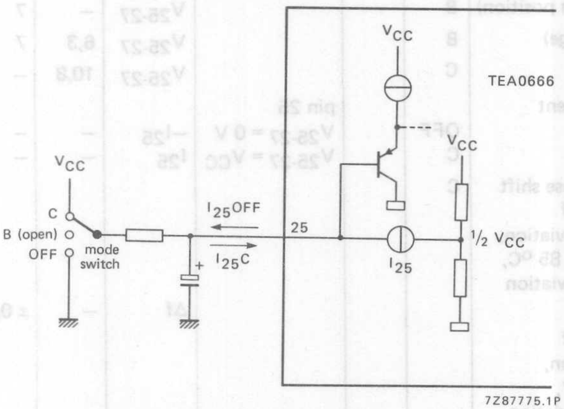



Fig. 3 Mode switch input configuration.

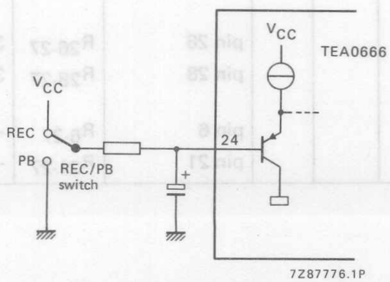
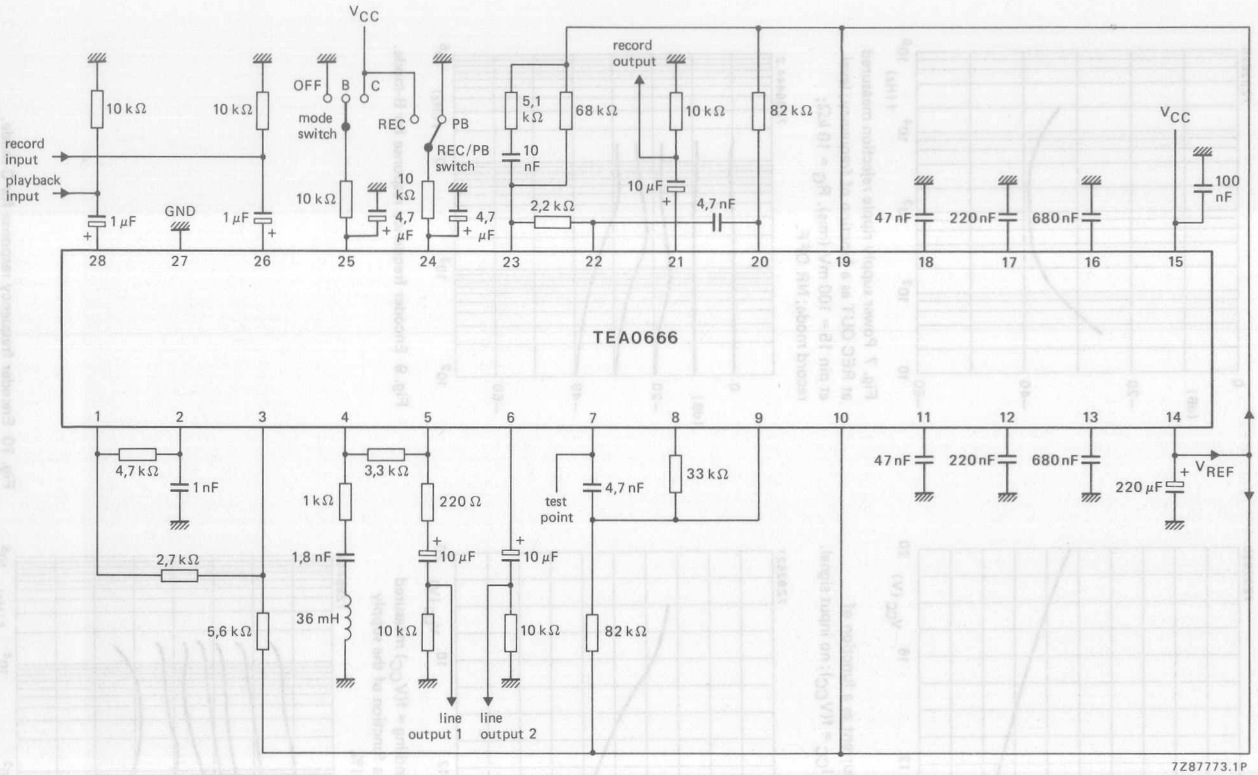



Fig. 4 REC/PB switch input configuration.

**DEVELOPMENT DATA**




REC = record mode
PB = playback mode

Tolerances: resistors 1%
capacitors 1%

Fig. 5 Test circuit.

## SYSTEM GRAPHS

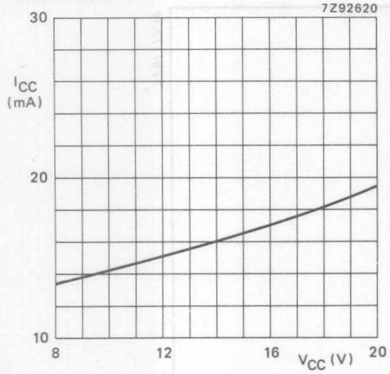



Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

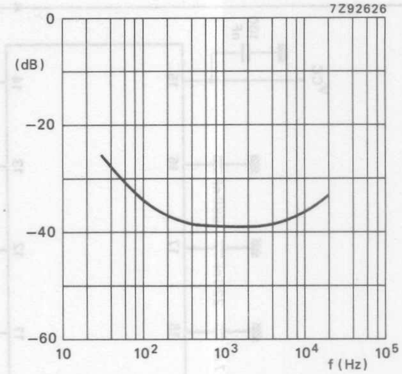



Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). $R_G = 10\ k\Omega$; record mode; NR OFF.

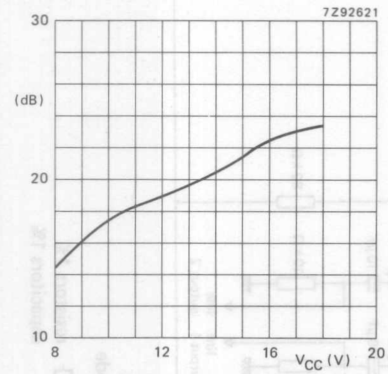



Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

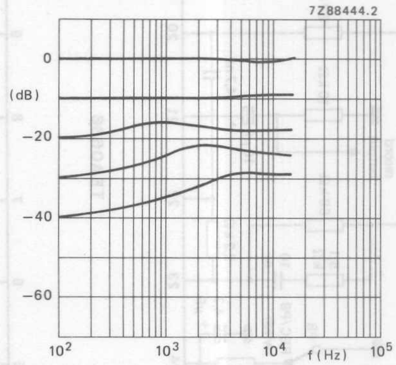



Fig. 9 Encoder frequency response for B-mode.

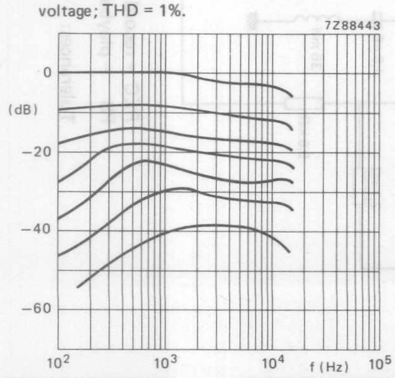



Fig. 10 Encoder frequency response for C-mode.

DEVELOPMENT DATA

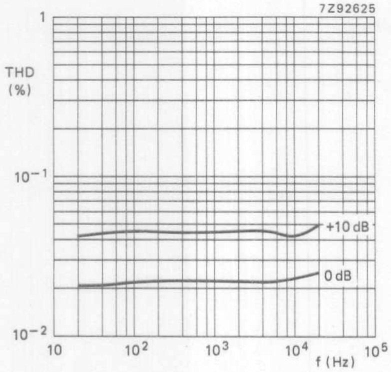



Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; $V_{CC}$ = 14 V; LPF 80 kHz.

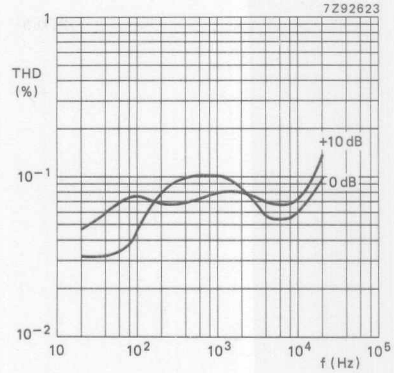



Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

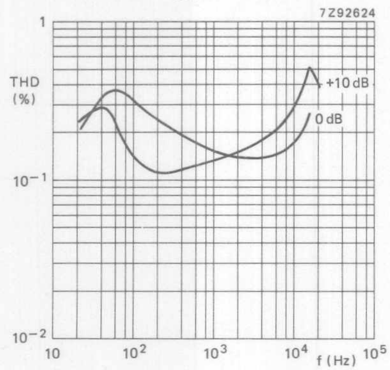



Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

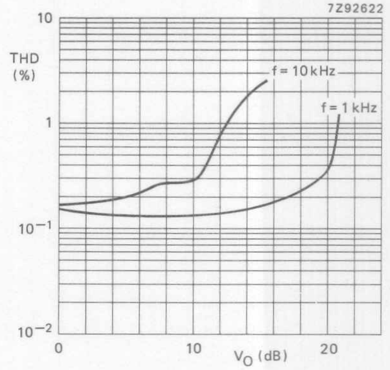



Fig. 14 Total harmonic distortion as a function of the record output level (pin21); for C-mode; $V_{CC}$ = 14 V; LPF 80 kHz.

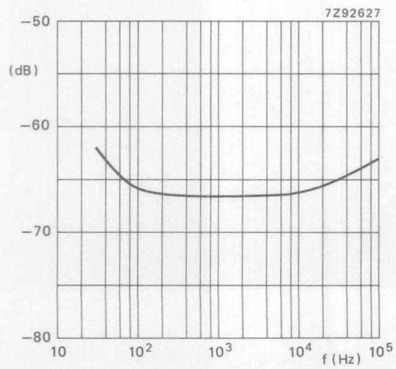



Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; $R_G$ = 10 kΩ.

# AM CAR RADIO RECEIVER CIRCUIT

The TEA5550 is an a.m. radio circuit, primarily intended for use in car radios.
The IC can reduce the costs in a car radio due to the following features:

- minimum periphery
- no extra r.f.-prestage is necessary
- ceramic i.f. filter is used
- simple on/off switching method allows inexpensive band switching in a.m./f.m. radios

The TEA5550 incorporates the following functions:

- a double balanced mixer with large signal handling range and common mode rejection properties
- a 'one-pin' oscillator, permitting the use of variable capacitance diode tuning
- an i.f. amplifier, designed for ceramic filters
- an a.m. envelope detector
- a.g.c. stages
- a voltage stabilizer, for supplying the internal circuit current and an external current up to 20 mA
- a simple d.c. switch for a.m./f.m. radios

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range; unstabilized (pin 8) | $V_P$ | | 10,2 to 18 | V |
| Supply voltage; stabilized (pin 9)* | $V_{stab}$ | typ. | 7,5 to 9 | V |
| Ambient temperature | $T_{amb}$ | typ. | 25 | °C |
| Supply voltage (pin 8) | $V_P$ | typ. | 14,4 | V |
| R.F. condition: $f_i$ = 1 MHz; m = 0,3; $f_m$ = 1 kHz | | | | |
| R.F. input voltage (pin 1) | | | | |
| $V_o$ = 30 mV | $V_i$ | typ. | 4 | μV |
| S/N = 26 dB | $V_i$ | typ. | 16 | μV |
| S/N = 46 dB | $V_i$ | typ. | 160 | μV |
| A.F. output voltage (pin 10) | | | | |
| $V_i$ = 10 mV | $V_o$ | typ. | 180 | mV |
| Total harmonic distortion over most of the a.g.c. range; m = 0,8 | THD | typ. | 1,2 | % |
| R.F. signal handling | | | | |
| THD = 10%; m = 0,8 | $V_i$ | typ. | 400 | mV |
| A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1}$ = 200 mV) | $V_{i1}/V_{i2}$ | typ. | 86 | dB |

* Pins 8 and 9 have to be short-circuited externally.

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

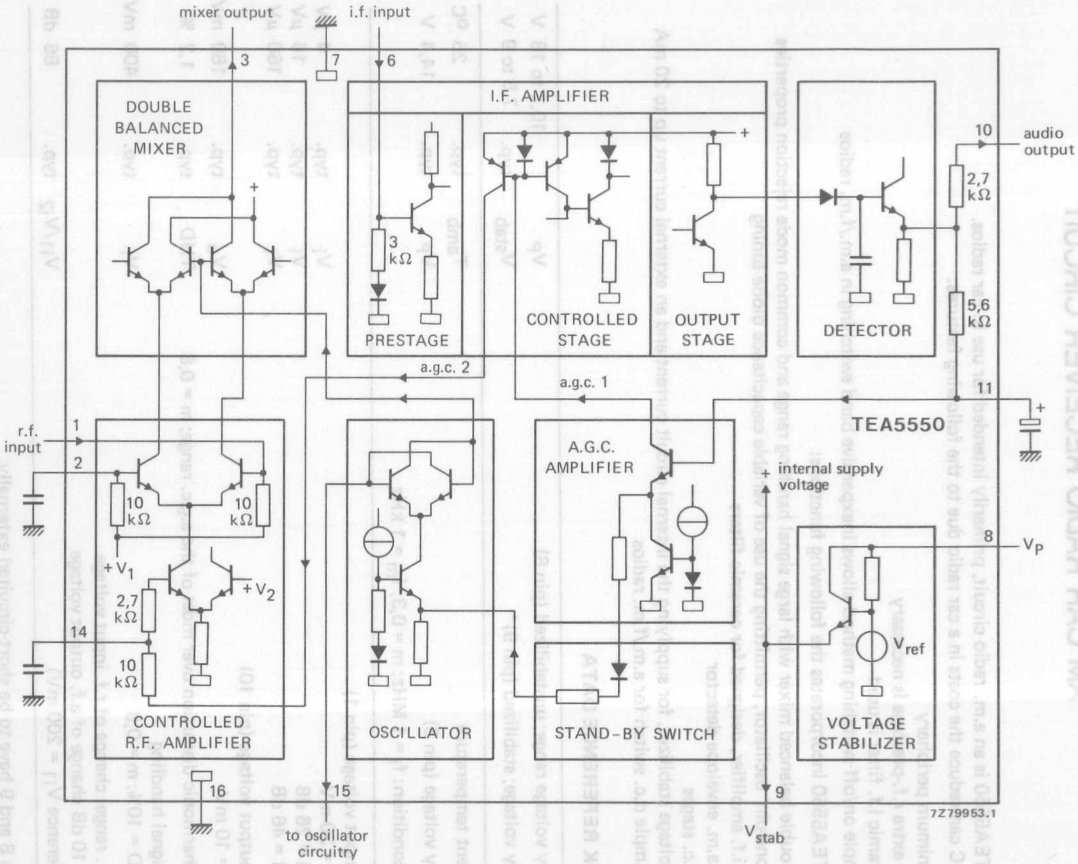



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltages | | | |
| pin 8 | $V_P = V_{8\text{-}16}$ | max. | 24 V |
| pin 3 | $V_{3\text{-}16}$ | max. | 24 V |
| Non-repetitive peak output current (pin 9) | $I_{9SM}$ | max. | 100 mA |
| Total power dissipation | $P_{tot}$ | max. | 1100 mW |
| Storage temperature | $T_{stg}$ | | −65 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 85 °C |

**Note**

Pins 4, 5, 12 and 13 are not allowed to be connected.

**D.C. CHARACTERISTICS** at $V_i = 0$

$V_P = 14{,}4$ V; $T_{amb} = 25$ °C; measured in Fig. 2

| | | | |
|---|---|---|---|
| Supply voltage range (unstabilized)* | $V_P$ | | 10,2 to 18 V |
| Voltage at pin 9; $-I_9 = 0$ | $V_{9\text{-}16} = V_{stab}$ | typ. | 8,7 V |
| | | | 8 to 9,2 V |
| Change in stabilization voltage (pin 9) | | | |
| at $-I_9 = 0$ to 20 mA | $\Delta V_{9\text{-}16} = \Delta V_{stab}$ | typ. | 50 mV |
| at $V_P = 10{,}2$ to 14,4 V | $\Delta V_{9\text{-}16} = \Delta V_{stab}$ | typ. | 300 mV |
| Voltage at pin 10 | $V_{10\text{-}16}$ | typ. | 1,1 V |
| Voltage at pins 1 and 2 | $V_{1\text{-}16} = V_{2\text{-}16}$ | typ. | 5,0 V |
| Voltage at pin 15 | $V_{15\text{-}16}$ | typ. | $V_{stab}$ |
| Total supply current; $-I_9 = 0$ | $I_{tot}$ | typ. | 20 mA |
| Current drain | | | |
| pin 3 | $I_3$ | typ. | 1 mA |
| pin 15 | $I_{15}$ | typ. | 0,2 mA |
| Current supplied from pin 9 | $-I_9$ | < | 20 mA |
| Power consumption; $-I_9 = 0$ | P | typ. | 300 mW |

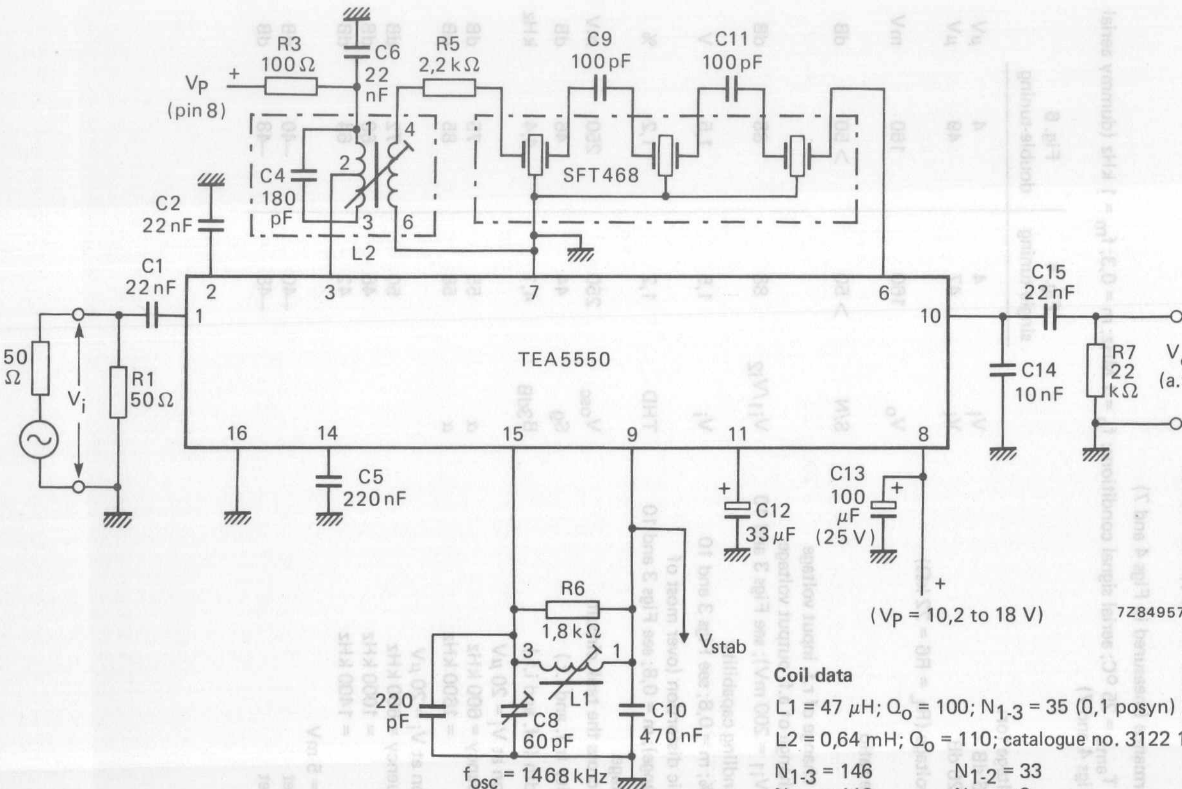
* A stabilized supply voltage of 7,5 to 9 V can also be applied at pin 9 (pin 8 short-circuited to pin 9).

## A.C. CHARACTERISTICS

$V_P$ = 14,4 V; $T_{amb}$ = 25 °C; r.f. condition: $f_i$ = 1 MHz, m = 0,3, $f_m$ = 1 kHz; transfer impedance of the i.f. filter $Z_{tr} = v_6/i_3$ = 850 Ω (loaded with 3 kΩ); measured in Fig. 2; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| R.F. input voltage; $V_o$ = 30 mV | $V_i$ | | 1,5 to 6,5 | μV |
| R.F. sensitivity at $R_S$ = 25 Ω for: | | | | |
| S + N/N = 6 dB | $V_i$ | typ. | 1,3 | μV |
| S + N/N = 20 dB | $V_i$ | typ. | 8 | μV |
| S + N/N = 26 dB | $V_i$ | typ. | 16 | μV |
| | | < | 20 | μV |
| S + N/N = 46 dB | $V_i$ | typ. | 160 | μV |
| S + N/N = 50 dB | $V_i$ | typ. | 350 | μV |
| Input conductance at pin 1 | | | | |
| $V_i$ = 0,1 mV | $g_{ie}$ | typ. | 0,2 | mS |
| $V_i$ = 100 mV | $g_{ie}$ | typ. | 0,1 | mS |
| Input conductance at pin 6 | $g_{ie}$ | typ. | 0,3 | mS |
| Output capacitance at pin 15 | $C_{oe}$ | typ. | 20 | pF |
| A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1}$ = 200 mV) | $V_{i1}/V_{i2}$ | typ. | 86 | dB |
| A.F. output voltage | | | | |
| $V_i$ = 10 mV | $V_o$ | > | 140 | mV |
| | | typ. | 180 | mV |
| Spread of a.f. output voltage | $\Delta V_o$ | typ. | ± 2 | dB |
| A.F. output impedance (pin 10) | $\|Z_o\|$ | typ. | 2,7 | kΩ |
| Total harmonic distortion at m = 0,8 | | | | |
| $V_i$ = 16 μV | THD | < | 2,5 | % |
| over most of the a.g.c. range (see also Figs 3 and 10) | THD | typ. | 1,2 | % |
| $V_i$ = 25 mV | THD | typ. | 3,5 | % |
| R.F. signal handling capability | | | | |
| THD = 10%; m = 0,8 | $V_i$ | > | 350 | mV |
| | | typ. | 400 | mV |
| I.F. suppression at $V_o$ = 30 mV | α | > | 20 | dB* |
| | | typ. | 35 | dB* |
| Oscillator voltage | | | | |
| $V_{9\text{-}16}$ = 8 V; $f_{osc}$ = 1468 kHz | $V_{15\text{-}8}$ | typ. | 250 | mV |
| | | < | 300 | mV |

* $\alpha = 20 \log \frac{V_{ia}}{V_{ib}}$, where: $V_{ia}$ is input voltage at f = 468 kHz and $V_{ib}$ is input voltage at f = 1 MHz.




**Coil data**

L1 = 47 $\mu$H; $Q_o$ = 100; $N_{1\text{-}3}$ = 35 (0,1 posyn) BR7

L2 = 0,64 mH; $Q_o$ = 110; catalogue no. 3122 138 91481

$N_{1\text{-}3}$ = 146 $N_{1\text{-}2}$ = 33

$N_{2\text{-}3}$ = 113 $N_{4\text{-}6}$ = 9

The transfer impedance of the i.f. filter is:

$Z_{tr} = v_6/i_3$ = 850 Ω ($R_L$ = 3 kΩ).

Fig. 2 AM test circuit.

## APPLICATION INFORMATION

Figures 4 and 7 show the circuit diagrams of single-tuned and double-tuned AM channels respectively, using the TEA5550 and an r.f.-tuning unit (type ALPS). The i.f. filter consists of a single-tuned coil in combination with a ceramic filter (type SFT468).

**Typical performance** (measured in Figs 4 and 7)

$V_P$ = 14,4 V; $T_{amb}$ = 25 °C; aerial signal conditions: $f_o$ = 1 MHz; m = 0,3; $f_m$ = 1 kHz (dummy aerial as shown in Figs 4 and 7)

| | | Fig. 4 single-tuning | Fig. 6 double-tuning | |
|---|---|---|---|---|
| R.F. input voltage for: | | | | |
| S + N/N = 6 dB | $V_i$ | 4 | 4 | μV |
| S + N/N = 26 dB | $V_i$ | 47 | 49 | μV |
| A.F. output voltage ($R_L$ = R6 = 22 kΩ) | | | | |
| $V_i$ = 1 mV | $V_o$ | 160 | 160 | mV |
| Signal-to-noise ratio | | | | |
| $V_i$ = 1 mV | S/N | > 50 | > 50 | dB |
| A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1}$ = 200 mV); see Figs 3 and 10 | $V_{i1}/V_{i2}$ | 88 | 88 | dB |
| R.F. signal handling capability | | | | |
| THD < 10%; m = 0,8; see Figs 3 and 10 | $V_i$ | 1,5 | 1,5 | V |
| Total harmonic distortion (over most of the a.g.c. range); m = 0,8; see Figs 3 and 10 | THD | 1,2 | 1,2 | % |
| Oscillator voltage measured across the tank circuit | $V_{osc}$ | 250 | 250 | mV |
| Total selectivity (r.f. and i.f.) | $S_9$ | 44 | 46 | dB |
| Total bandwidth (r.f. and i.f.) | $B_{3dB}$ | 4,1 | 4,4 | kHz |
| I.F. suppression at $V_i$ = 20 μV | | | | |
| tuned frequency = 600 kHz | α | 55 | 75 | dB |
| = 1600 kHz | α | 58 | 85 | dB |
| Image rejection at $V_i$ = 20 μV | | | | |
| tuned frequency = 600 kHz | | 50 | 72 | dB |
| = 1000 kHz | | 46 | 68 | dB |
| = 1400 kHz | | 42 | 64 | dB |
| Whistle at $V_i$ = 5 mV | | | | |
| 2 x i.f.-tweet | | –40 | –40 | dB |
| 3 x i.f.-tweet | | –48 | –48 | dB |

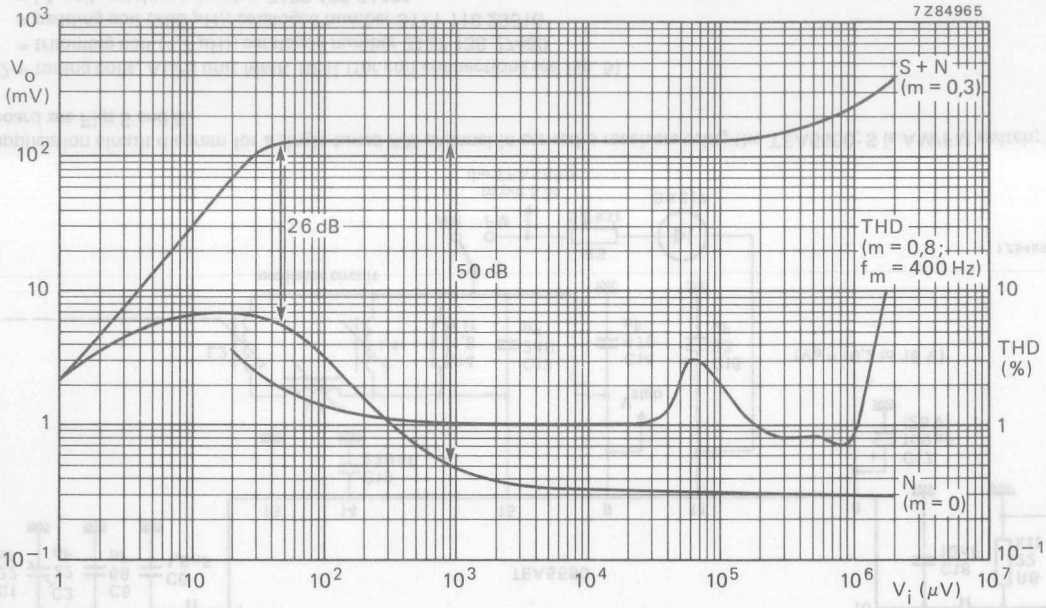



Fig. 3 Typical signal and noise output voltages ($V_o$ is a.f. output voltage) as a function of the input voltage $V_i$. Also shown is the total harmonic distortion (THD). These curves are for a single-tuned AM channel; the dummy aerial is as shown in Fig. 4; $f_o$ = 1 MHz; $f_m$ = 1 kHz; m = 0,3 (unless otherwise specified).

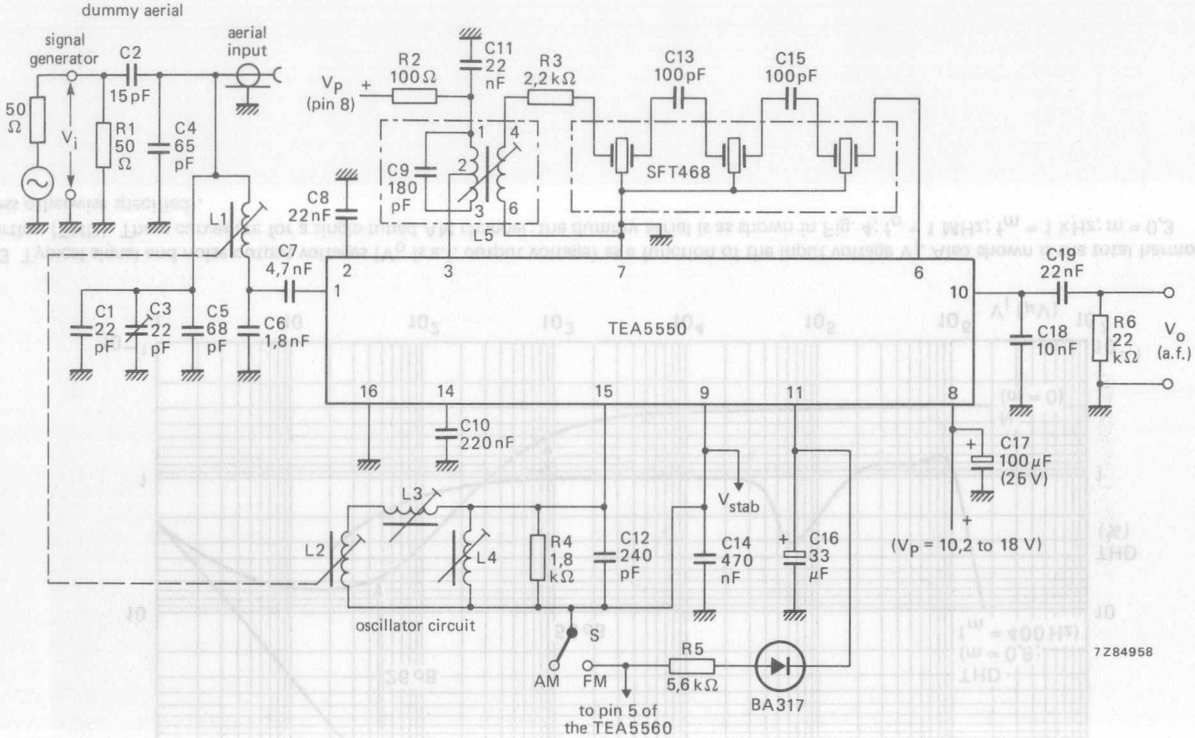



Fig. 4 Typical application circuit diagram for a single-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 5 and 6.

Coil data: L1, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 5)

L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460

L4 = padding coil (200 μH); catalogue number 3111 118 23510

L5 = i.f. coil; catalogue number 3122 138 91481

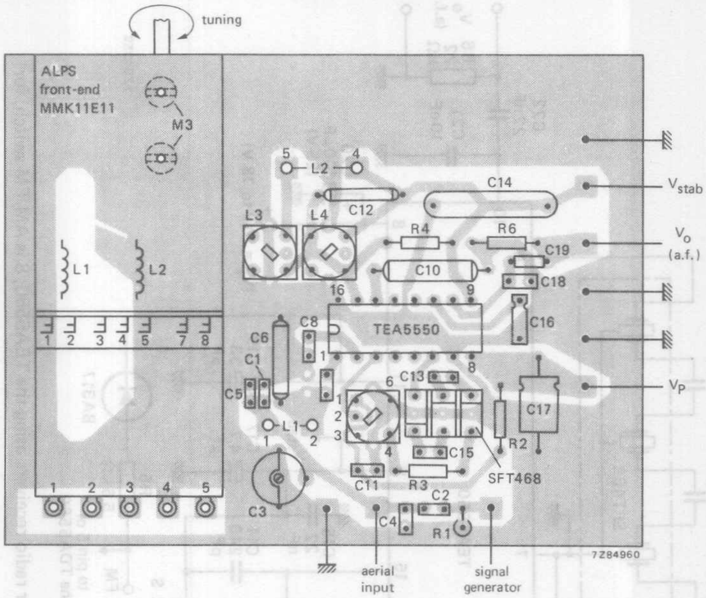



Fig. 5 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 4.

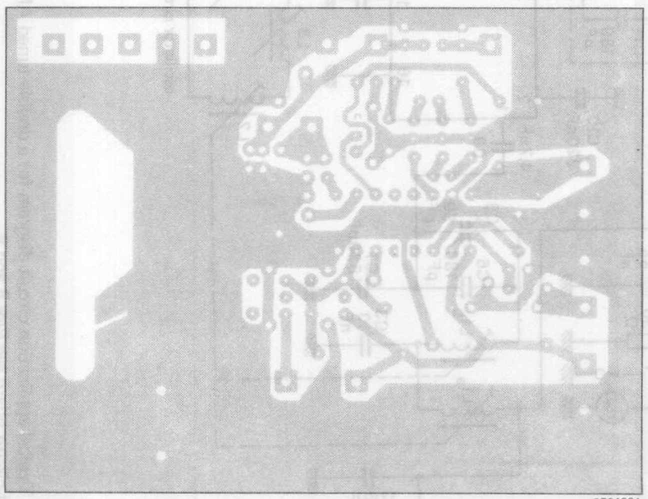



Fig. 6 Printed-circuit board showing track side.

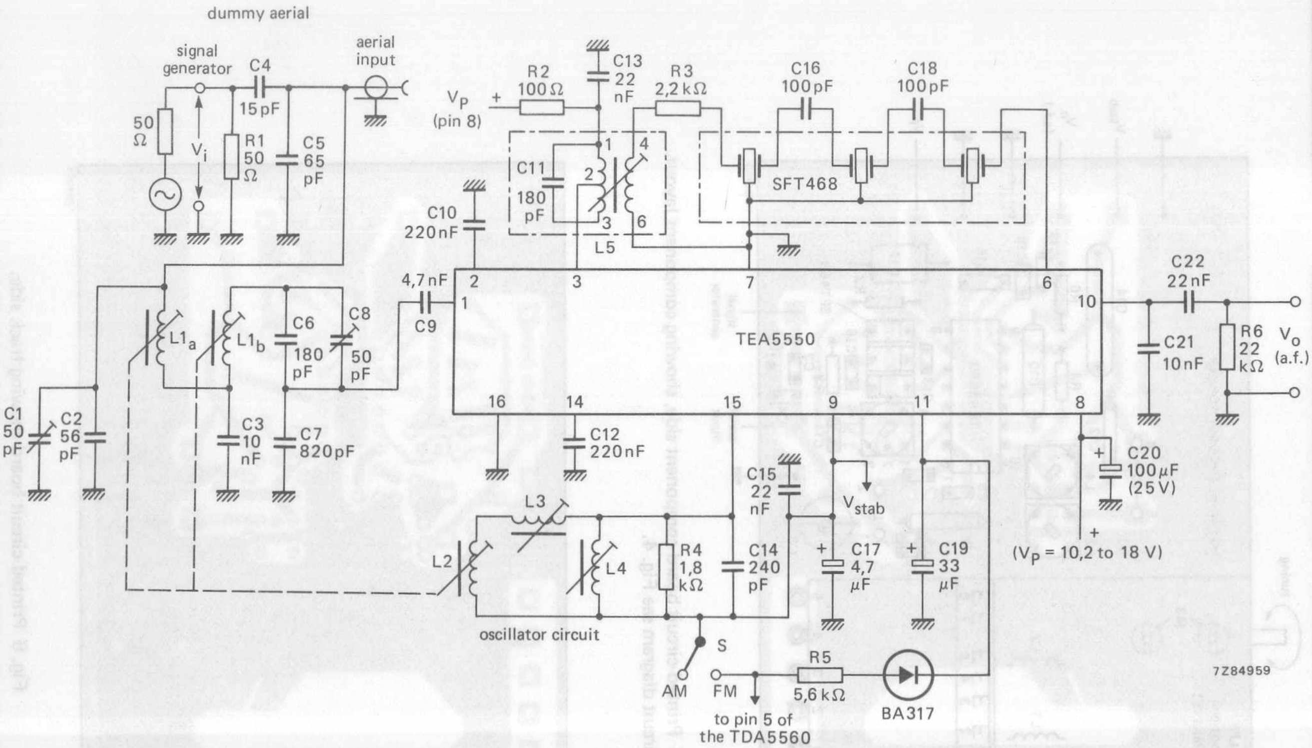



Fig. 7 Typical application circuit diagram for a double-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 8 and 9.

Coil data: $L1_a$, $L1_b$, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 8)
L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460
L4 = padding coil (200 μH); catalogue number 3111 118 23510
L5 = i.f. coil; catalogue number 3122 138 91481

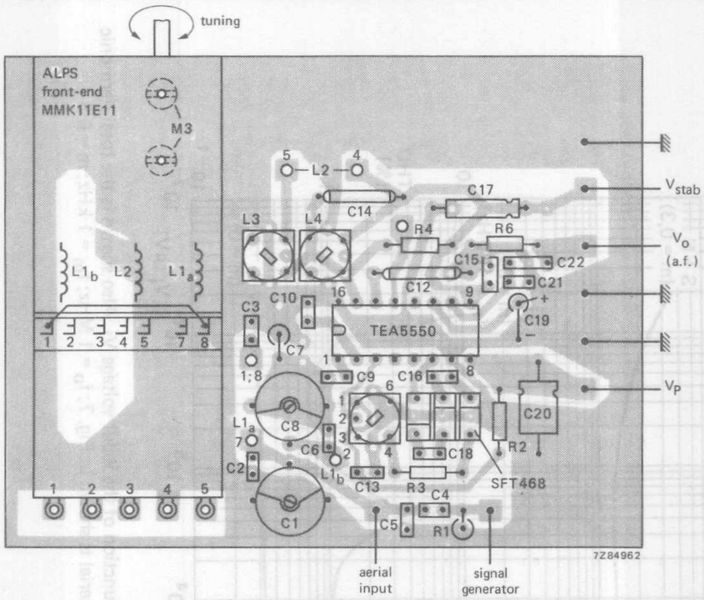



Fig. 8 Printed-circuit board component side, showing component layout.
For circuit diagram see Fig. 7.

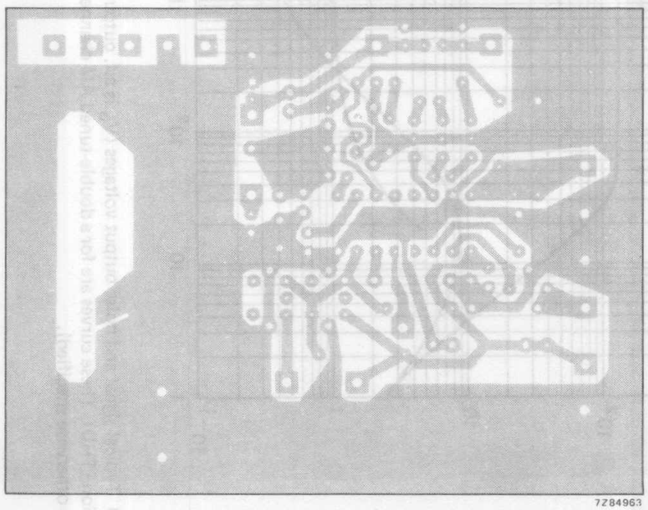



Fig. 9 Printed-circuit board showing track side.

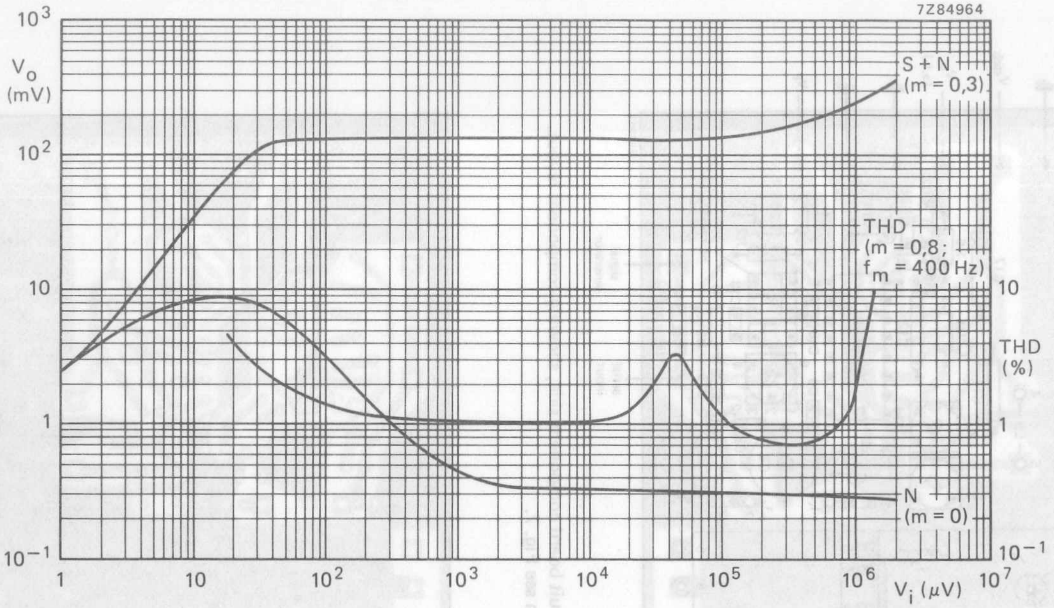



Fig. 10 Typical signal and noise output voltages ($V_o$ is a.f. output voltage) as a function of the input voltage $V_i$. Also shown is the total harmonic distortion (THD). These curves are for a double-tuned AM channel; the dummy aerial is shown in Fig. 7; $f_o$ = 1 MHz; $f_m$ = 1 kHz; m = 0,3 (unless otherwise specified).

# FM/IF SYSTEM

## GENERAL DESCRIPTION

The TEA5560 is a monolithic integrated FM/IF system circuit, intended for car radios and home-receivers equipped with a ratio detector.
The system incorporates the following functions:

- a three-stage i.f. limiting amplifier
- a 15 dB field-strength dependent muting circuit
- a field-strength dependent d.c. voltage for e.g.:
  mono/stereo switching
  channel separation control of a stereo decoder
  an indicator ($I_{max} \leqslant 1$ mA)
- standby ON/OFF switching circuit
- a voltage stabilizer, for the internal circuit current and an external current up to 15 mA
- adjustable gain ($\Delta G = 15$ dB)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 6) | $V_P$ | | 10,2 to 18 | V |
| Ambient temperature | $T_{amb}$ | typ. | 25 | °C |
| Supply voltage (pin 6) | $V_P$ | typ. | 14,4 | V |
| Frequency | $f_o$ | | 10,7 | MHz |
| Sensitivity (3 dB limiting) | $V_i$ | typ. | 150 | µV |
| Signal-to-noise ratio for $V_i = 10$ mV | S/N | typ. | 80 | dB |
| A.F. output voltage at $\Delta f = \pm 22,5$ kHz | $V_o$ | typ. | 200 | mV |
| Total harmonic distortion; $\Delta f = \pm 22,5$ kHz | THD | typ. | 0,3 | % |
| A.M. suppression<br>AM signal: $m = 0,3$; $f_m = 1$ kHz<br>FM signal: $\Delta f = \pm 22,5$ kHz; $f_m = 70$ Hz for $V_i = 1$ mV | AMS | typ. | 50 | dB |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142). The tab (on top of the package) is connected to pin 9.

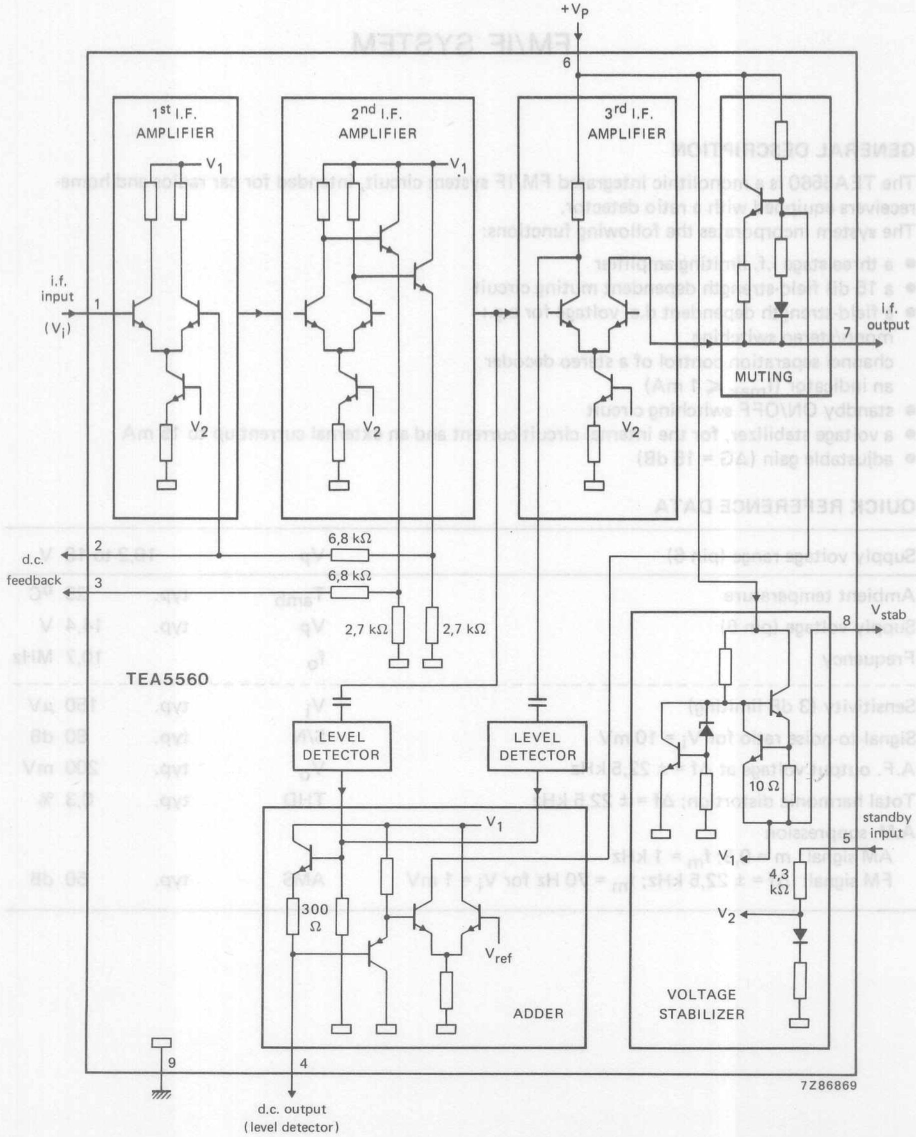



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltages | | | | |
| pin 6 | $V_P = V_{6\text{-}9}$ | max. | 24 | V |
| pin 7 | $V_{7\text{-}9}$ | max. | 24 | V |
| Voltage at pin 4 | $V_{4\text{-}9}$ | max. | 6 | V |
| Voltage at pin 5 | $V_{5\text{-}9}$ | max. | 9 | V |
| Non-repetitive peak output current (pin 8) | $-I_{8SM}$ | max. | 100 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1000 | mW |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to + 85 | °C |

## THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}amb}$ = 75 K/W

## D.C. CHARACTERISTICS

$V_P$ = 14,4 V; $T_{amb}$ = 25 °C; measured in Fig. 2; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 6) | | | | | |
| Supply voltage * | $V_P = V_{6\text{-}9}$ | 10,2 | 14,4 | 18,0 | V |
| **Voltages** | | | | | |
| at pin 8; $-I_8 = 0$ ** | $V_{8\text{-}9}$ | 7,5 | 8,0 | 8,5 | V |
| at pin 8 when $-I_8$ increases from 0 to 15 mA | $\Delta V_{8\text{-}9}$ | – | 200 | 300 | mV |
| at pin 8 when $V_P$ reduces from 14,4 V to 10,2 V | $\Delta V_{8\text{-}9}$ | – | – | 1,0 | V |
| at pin 8 when $V_P$ increases from 14,4 V to 18,0 V | $\Delta V_{8\text{-}9}$ | – | – | 200 | mV |
| at pin 4 (level detector) | $V_{4\text{-}9}$ | – | – | 100 | mV |
| at pins 1, 2 and 3 | $V_{1,2,3\text{-}9}$ | – | 2,4 | – | V |
| **Currents** | | | | | |
| Total supply current; $-I_8 = 0$ | $I_{tot}$ | 15 | 20 | 30 | mA |
| Current supplied from pin 8 | $-I_8$ | – | – | 15 | mA |
| Stand-by current; $V_{5\text{-}9} = 0$ | $I_{sb}$ | 8 | 11 | 14 | mA |
| Current into pin 5 | $I_5$ | 1,0 | 1,5 | 2,0 | mA |
| Current into pin 7 | $I_7$ | – | 3,0 | – | mA |
| **Power consumption** | | | | | |
| at $-I_8 = 0$ | P | – | 300 | – | mW |

* A stabilized supply voltage of 7 to 9 V can also be applied at pin 5 and 6 (linked); for this application pin 8 must not be connected.

** The temperature coefficient of the stabilized voltage at pin 8 is typical –2,3 mV/K.

## A.C. CHARACTERISTICS

$V_P$ = 14,4 V; $T_{amb}$ = 25 °C; $V_i$ = 1 mV; $f_o$ = 10,7 MHz; Δf = ± 22,5 kHz; $f_m$ = 1 kHz; measured in Fig. 2; unless otherwise specified

| parameter | symbpl | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **I.F. part and ratio detector** | | | | | |
| Sensitivity | | | | | |
| at –3 dB before limiting (pin 1); (without muting) * | $V_i$ | 105 | 150 | 210 | μV |
| Signal-to-noise S + N/S measured in a bandwidth of 60 Hz to 15 kHz | | | | | |
| at $V_i$ = 20 μV | S/N | 40 | 45 | – | dB |
| at $V_i$ = 150 μV | S/N | – | 65 | – | dB |
| at $V_i$ = 1 mV | S/N | – | 78 | – | dB |
| at $V_i$ = 10 mV | S/N | – | 80 | – | dB |
| A.F. output voltage | | | | | |
| Δf = ± 22,5 kHz | $V_o$ | – | 200 | – | mV |
| Δf = ± 75 kHz | $V_o$ | – | 600 | – | mV |
| Total harmonic distortion | | | | | |
| Δf = ± 22,5 kHz | THD | – | 0,3 | – | % |
| Δf = ± 75 kHz | THD | – | 2,0 | – | % |
| AM suppression | | | | | |
| $f_m$ = 1 kHz; m = 0,3 (for AM) | | | | | |
| $f_m$ = 70 kHz; Δf = ± 22,5 kHz (for FM) | | | | | |
| at $V_i$ = 150 μV | AMS | – | 40 | – | dB |
| at $V_i$ = 1 mV | AMS | – | 50 | – | dB |
| at $V_i$ = 10 mV | AMS | – | 55 | – | dB |
| **Level detector circuit** | | | | | |
| D.C. output voltage (pin 4) | | | | | |
| at $V_i$ = 200 μV | $V_{4\text{-}9}$ | – | 1,9 | – | V |
| at $V_i$ = 500 μV | $V_{4\text{-}9}$ | – | 2,8 | – | V |
| at $V_i$ = 1 mV | $V_{4\text{-}9}$ | – | 3,5 | – | V |
| at $V_i$ = 3 mV | $V_{4\text{-}9}$ | – | 5,0 | – | V |
| at $V_i$ = 10 mV | $V_{4\text{-}9}$ | – | 5,7 | – | V |
| **Muting circuit** (see also Fig. 5) | | | | | |
| Change in output voltage at $V_i$ = 3 μV (with and without muting) * | $\alpha_{vo}$ | 10 | 15 | – | dB |
| Input voltage at a change in output voltage of ⩽ 1 dB* ($V_i$ at $\alpha_{vo}$ ⩽ 1 dB) | $V_i$ | – | – | 250 | μV |

* With muting $V_{4\text{-}9}$ < 0,3 V; without muting $V_{4\text{-}9}$ = 1,2 to 6 V.

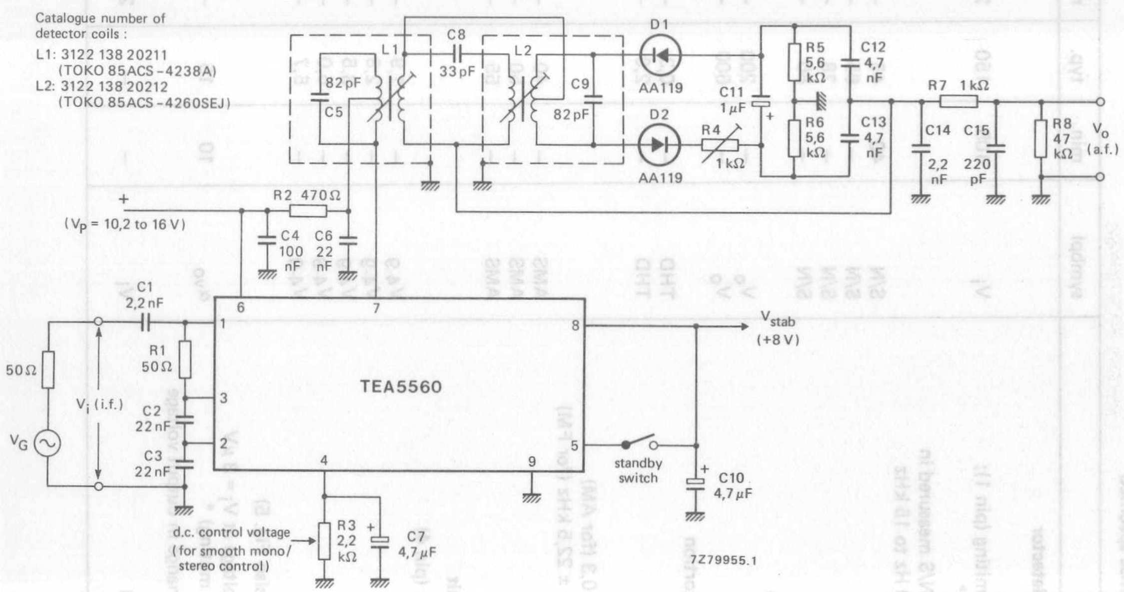



Fig. 2 FM test circuit.

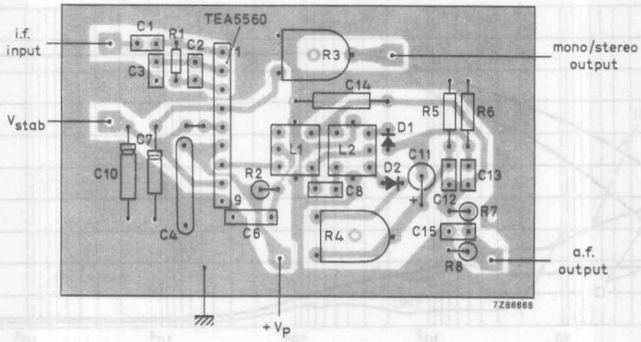



Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

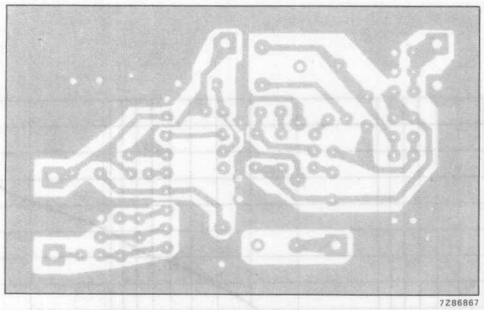
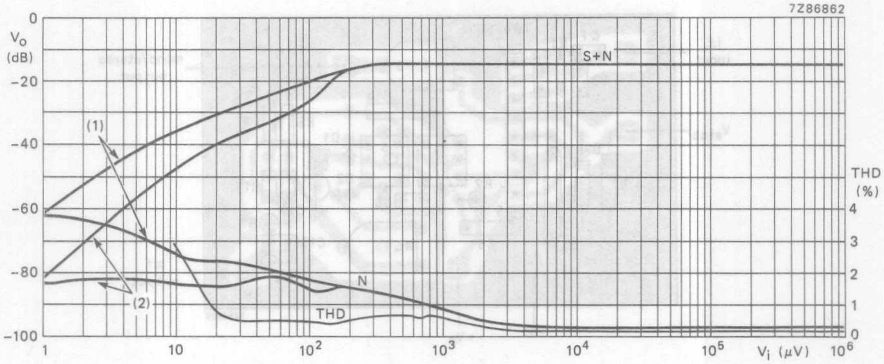



Fig. 4 Printed-circuit board showing track side.




(1) Without muting.
(2) With muting.

Fig. 5 A.F. output voltage ($V_o$); reference level 0 dB = 1 V, and the total harmonic distortion (THD) as a function of the i.f. input voltage ($V_i$). Measured in the test circuit Fig. 2 at $\Delta f = \pm$ 22,5 kHz; $f_m$ = 1 kHz.

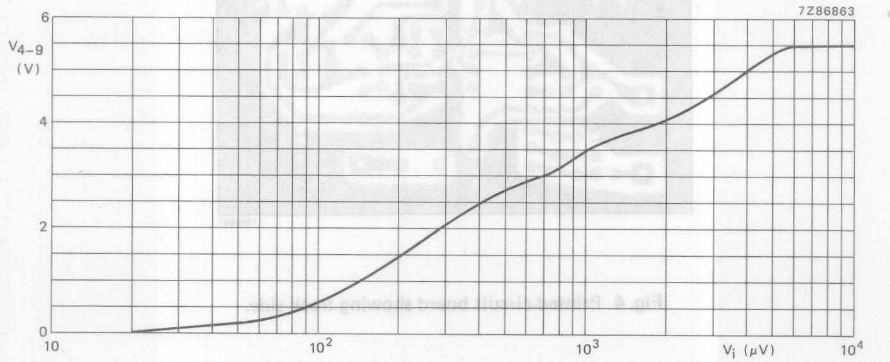
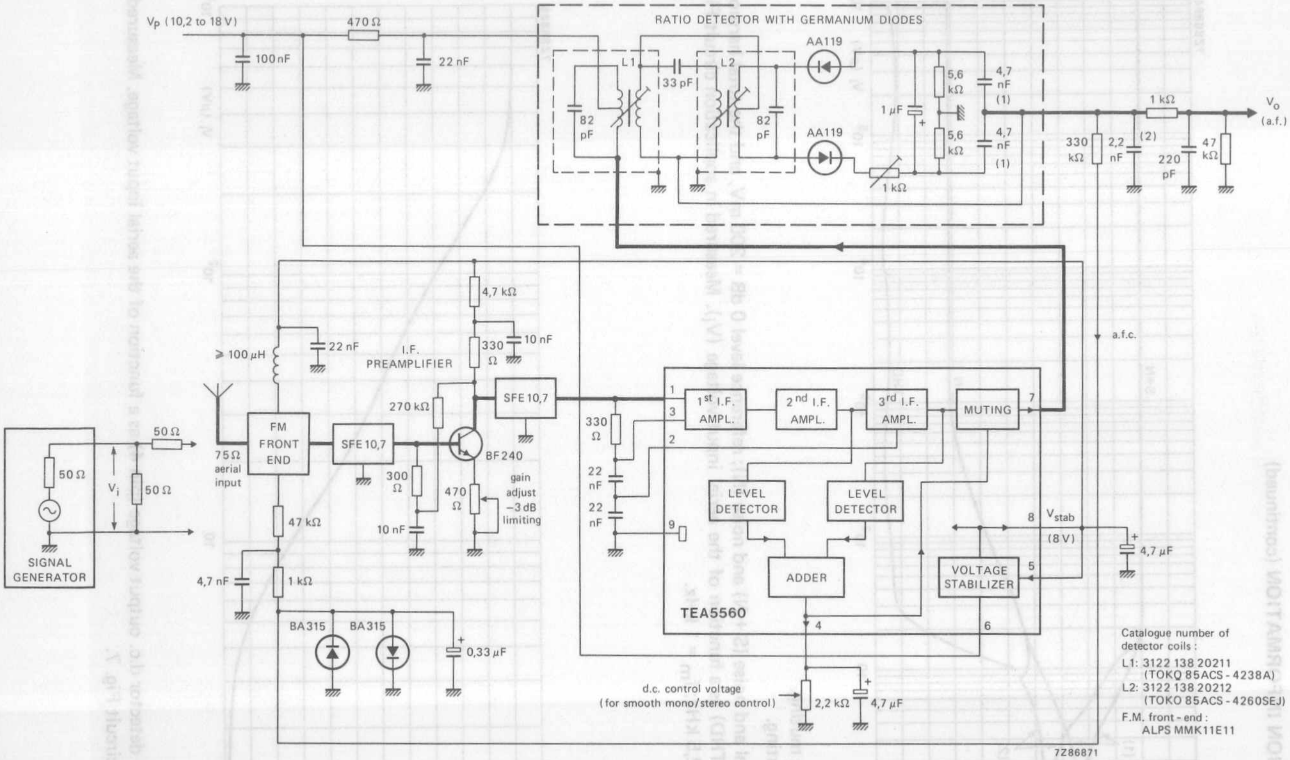



Fig. 6 Level detector d.c. output voltage (pin 4) as a function of the i.f. input voltage. Measured in test circuit Fig. 2.

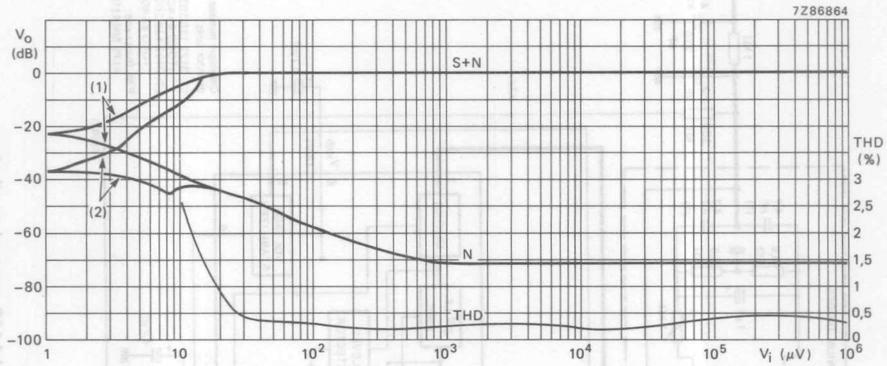
## APPLICATION INFORMATION




(1) Stereo application 220 pF.
(2) Stereo application 390 pF.

Fig. 7 FM channel for (car) radios using the TEA5560 and a ratio detector with AA119 germanium diodes.

APPLICATION INFORMATION (continued)




(1) Without muting.
(2) With muting.

Fig. 8 Signal and noise (S + N) and noise (N); reference level 0 dB = 200 mV, and the total harmonic distortion (THD) as a function of the aerial input voltage ($V_i$). Measured in application circuit Fig. 7 at $\Delta f = \pm$ 22,5 kHz; $f_m$ = 1 kHz.

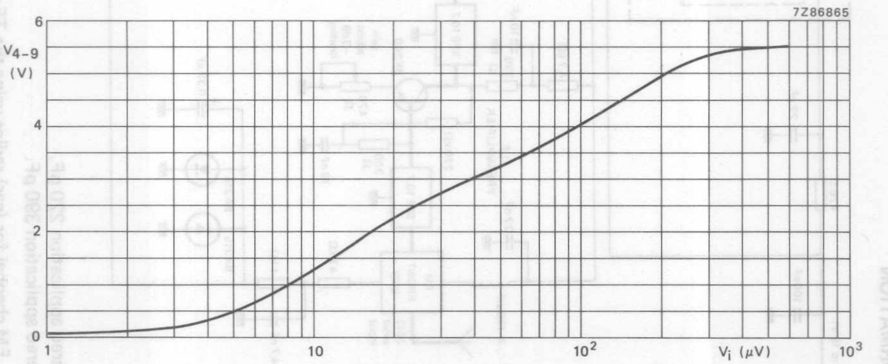
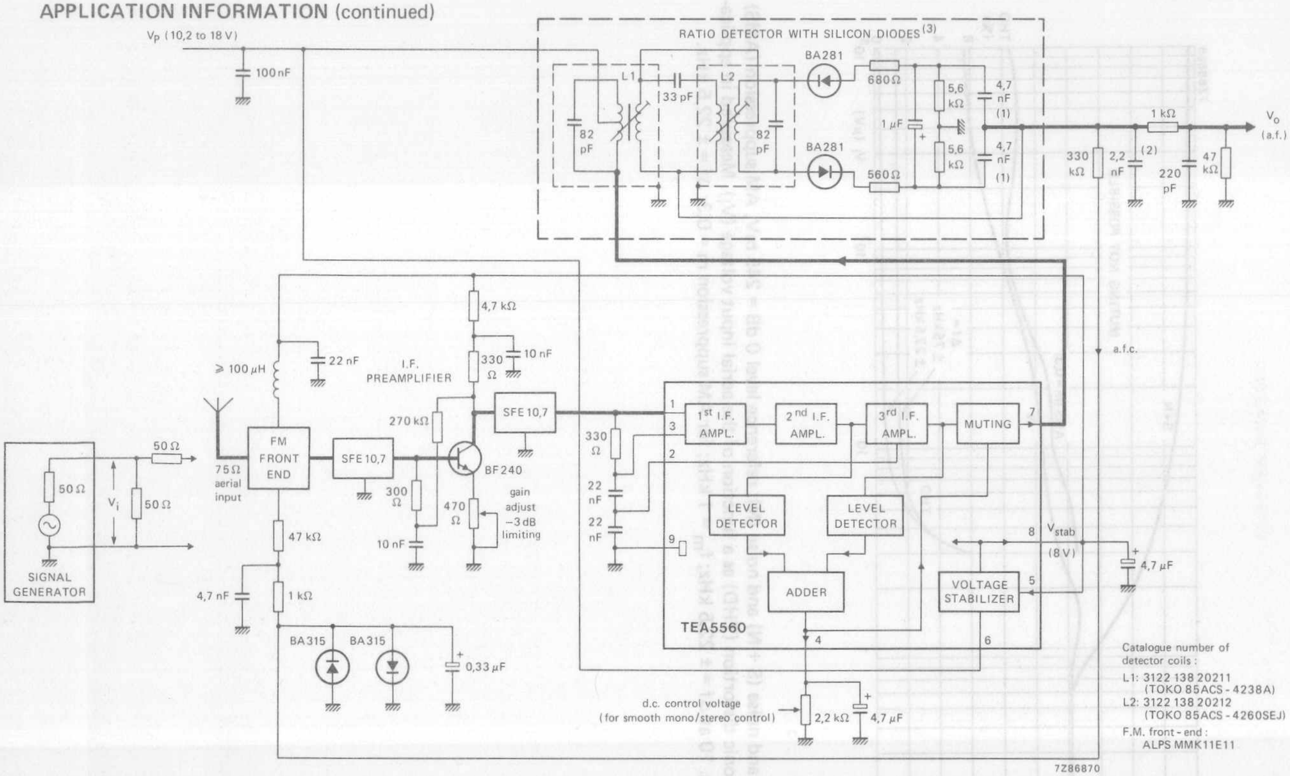



Fig. 9 Level detector d.c. output voltage (pin 4) as a function of the aerial input voltage. Measured in application circuit Fig. 7.

## APPLICATION INFORMATION (continued)




(1) Stereo application 220 pF.
(2) Stereo application 390 pF.
(3) Further detailed information of using silicon diodes is available on request.

Fig. 10 FM channel for (car) radios using the TEA5560 and a ratio detector with BA281 silicon diodes.

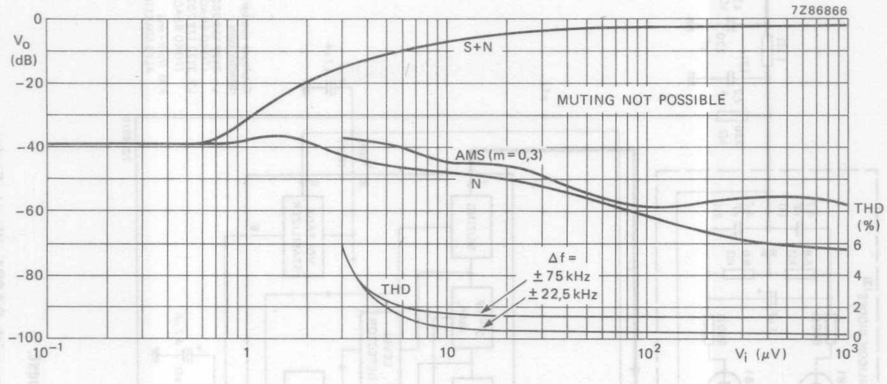



Fig. 11 Signal and noise (S + N) and noise (N); reference level 0 dB = 245 mV, AM suppression (AMS) and total harmonic distortion (THD) as a function of the aerial input voltage ($V_i$). Measured in application circuit Fig. 10 at Δf = ± 22,5 kHz; $f_m$ = 1 kHz; for AM suppression m = 0,3; Δf = ± 22,5 kHz.

# RF/IF CIRCUIT FOR AM/FM RADIO

## GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

### Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption ($I_{tot}$ = 6 mA)
- Low voltage operation ($V_P$ = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

## QUICK REFERENCE DATA (at $T_{amb}$ = 25 °C)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{7\text{-}16}$ | typ. | 5,4 | V |
| Supply current | $I_7$ | typ. | 6,2 | mA |
| **AM performance** (pin 2) for m = 0,3 | | | | |
| Sensitivity | | | | |
| at $V_o$ = 10 mV | $V_i$ | typ. | 1,7 | μV |
| at S/N = 26 dB | $V_i$ | typ. | 16 | μV |
| A.F. output voltage at $V_i$ = 1 mV | $V_o$ | typ. | 100 | mV |
| Total harmonic distortion at $V_i$ = 1 mV | THD | typ. | 0,5 | % |
| **FM performance** (pin 1) for Δf = ± 22,5 kHz | | | | |
| limiting sensitivity, −3 dB | $V_i$ | typ. | 110 | μV |
| Signal-to-noise ratio for $V_i$ = 1 mV | S/N | typ. | 65 | dB |
| A.F. output voltage at $V_i$ = 1 mV | $V_o$ | typ. | 100 | mV |
| Total harmonic distortion at $V_i$ = 1 mV | THD | typ. | 0,3 | % |
| AM suppression at $V_i$ = 10 mV | AMS | typ. | 50 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

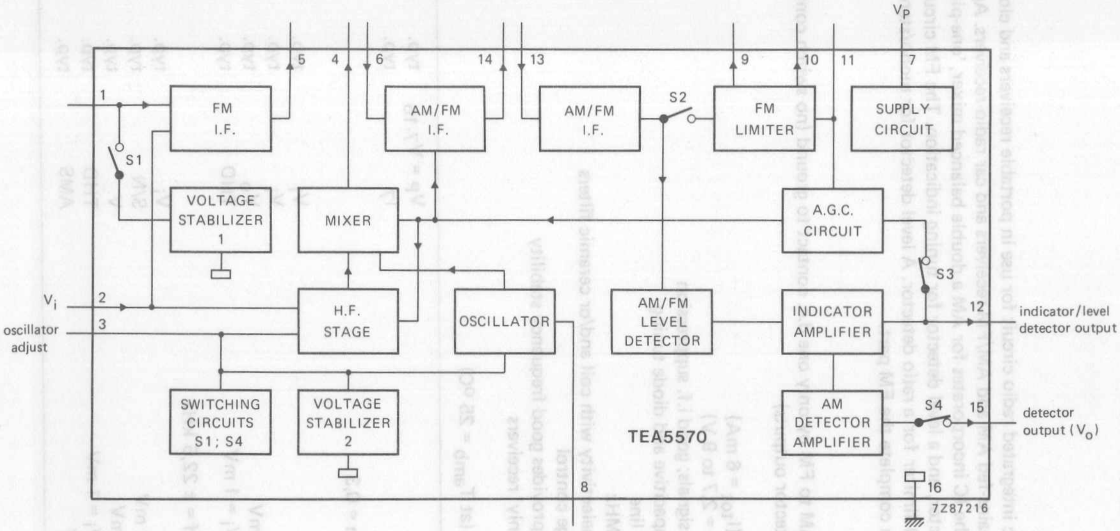



Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 7) | $V_P = V_{7\text{-}16}$ | max. | 12 V |
| Voltage at pins 4, 5, 9 and 10 to pin 16 (ground) | $V_{n\text{-}16}$ | max. | 12 V |
| Voltage range at pin 8 | $V_{8\text{-}16}$ | | $V_P \pm 0{,}5$ V |
| Current into pin 5 | $I_5$ | max. | 3 mA |
| Total power dissipation | $P_{tot}$ | see Fig. 2 | W |
| Storage temperature range | $T_{stg}$ | | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −30 to +85 °C |

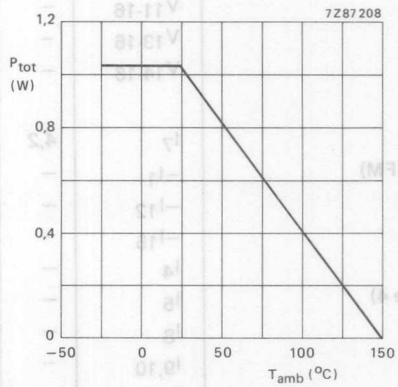



Fig. 2 Power derating curve.

## D.C. CHARACTERISTICS

$V_P$ = 6 V; $T_{amb}$ = 25 °C; measured in Fig. 10; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 7) | | | | | |
| Supply voltage (note 1) | $V_P = V_{7-16}$ | 2,4 | 5,4 | 9,0 | V |
| **Voltages** | | | | | |
| at pin 1 (FM) | $V_{1-16}$ | – | 1,42 | – | V |
| at pin 1; $-I_1$ = 50 μA (FM) | $V_{1-16}$ | – | 1,28 | – | V |
| at pins 2 and 3 (AM) | $V_{2,3-16}$ | – | 1,42 | – | V |
| at pin 6 | $V_{6-16}$ | – | 0,7 | – | V |
| at pin 11 | $V_{11-16}$ | – | 1,4 | – | V |
| at pin 13 | $V_{13-16}$ | – | 0,7 | – | V |
| at pin 14 | $V_{14-16}$ | – | 4,3 | – | V |
| **Currents** | | | | | |
| Supply current | $I_7$ | 4,2 | 6,2 | 8,2 | mA |
| Current supplied from pin 1 (FM) | $-I_1$ | – | – | 50 | μA |
| Current supplied from pin 12 | $-I_{12}$ | – | – | 20 | μA |
| Current supplied from pin 15 | $-I_{15}$ | – | 30 | – | μA |
| Current into pin 4 (AM) | $I_4$ | – | 0,6 | – | mA |
| Current into pin 5 (FM) (note 4) | $I_5$ | – | 0,35 | – | mA |
| Current into pin 8 (AM) | $I_8$ | – | 0,3 | – | mA |
| Current into pins 9, 10 (FM) | $I_{9,10}$ | – | 0,65 | – | mA |
| Current into pin 14 | $I_{14}$ | – | 0,4 | – | mA |
| **Power consumption** | P | – | 40 | – | mW |

## A.C. CHARACTERISTICS

### AM performance

$V_P$ = 6 V; $T_{amb}$ = 25 °C; r.f. condition: $f_i$ = 1 MHz, m = 0,3, $f_m$ = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| R.F. sensitivity (pin 2) | | | | | |
| at $V_o$ = 30 mV | $V_i$ | 3,5 | 5,0 | 7,0 | μV |
| at S + N/N = 6 dB | $V_i$ | | 1,3 | | μV |
| at S + N/N = 26 dB | $V_i$ | – | 16 | 20 | μV |
| at S + N/N = 50 dB | $V_i$ | – | 1 | – | mV |
| Signal handling (THD ⩽ 10% at m = 0,8) | $V_i$ | 200 | – | – | mV |
| A.F. output voltage at $V_i$ = 1 mV | $V_o$ | 80 | 100 | 125 | mV |
| Total harmonic distortion | | | | | |
| at $V_i$ = 100 μV to 100 mV (m = 0,3) | THD | – | 0,5 | – | % |
| at $V_i$ = 2 mV (m = 0,8) | THD | – | 1,0 | 2,5 | % |
| at $V_i$ = 200 mV (m = 0,8) | THD | – | 4,0 | 10 | % |
| I.F. suppression at $V_o$ = 30 mV (note 2) | α | 26 | 35 | – | dB |
| Oscillator voltage (pin 8; note 3) | | | | | |
| at $f_{osc}$ = 1455 kHz | $V_{8-16}$ | 120 | 160 | 200 | mV |
| Indicator current (pin 12) at $V_i$ = 1 mV | $I_{12}$ | – | 200 | 230 | μA |

### FM performance

$V_P$ = 6 V; $T_{amb}$ = 25 °C; i.f. condition: $f_i$ = 10,7 MHz, Δf = ± 22,5 kHz, $f_m$ = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **I.F. part** | | | | | |
| I.F. sensitivity (adjustable; note 4) | | | | | |
| Input voltage | | | | | |
| at −3 dB before limiting | $V_i$ | 90 | 110 | 130 | μV |
| at S + N/N = 26 dB | $V_i$ | – | 6 | – | μV |
| at S + N/N = 65 dB | $V_i$ | – | 1 | – | mV |
| A.F. output voltage at $V_i$ = 1 mV | $V_o$ | 80 | 100 | 125 | mV |
| Total harmonic distortion at $V_i$ = 1 mV | THD | – | 0,3 | – | % |
| AM suppression (note 5) | AMS | – | 50 | – | dB |
| **Indicator/level detector** (pin 12) | | | | | |
| Indicator current | $I_{12}$ | – | 250 | 325 | μA |
| D.C. output voltage | | | | | |
| at $V_i$ = 300 μV | $V_{12-16}$ | – | 0,25 | – | V |
| at $V_i$ = 2 mV | $V_{12-16}$ | – | 1,0 | – | V |
| **AM to FM switch** | | | | | |
| Switching current at $V_{3-16}$ < 1 V | $-I_3$ | – | – | 400 | μA |

**Notes to characteristics**

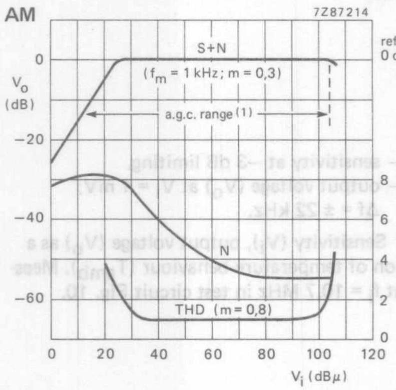
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: $V_{i1}$ is the input voltage at f = 455 kHz and $V_{i2}$ is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by $R_{osc}$ (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
$I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

**Facility adaptation**

Facility adaptation is achieved as follows (see Fig. 10):

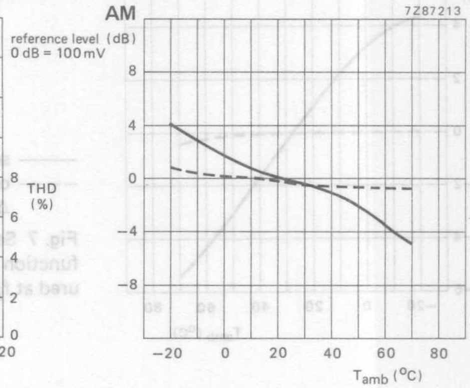
| Facility | Component |
|---|---|
| FM sensitivity | R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A)<br>(gain adjustable ± 10 dB; see note 4) |
| AM sensitivity | R11 and coil tapping |
| AM oscillator biasing | $R_{osc}$ |
| AM output voltage | R7, R11 |
| AM a.g.c. setting | R7 |

## Typical graphs



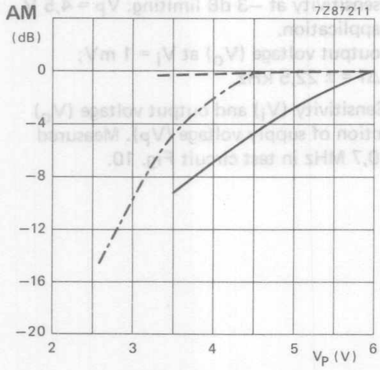

(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage ($V_i$). Measured at $f_i$ = 1 MHz in test circuit Fig. 10.




——— sensitivity ($V_i$) at $V_o$ = 30 mV; m = 0,3.
– – – – output voltage ($V_o$) at $V_i$ = 2 mV; m = 0,3.

Fig. 4 Sensitivity ($V_i$), output voltage ($V_o$) as a function of temperature behaviour ($T_{amb}$). Measured at $f_i$ = 1 MHz in test circuit Fig. 10.




——— sensitivity ($V_i$) at $V_o$ = 30 V; m = 0,3: 6,0 V application.
–·–·–· sensitivity ($V_i$) at $V_o$ = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage ($V_o$) at $V_i$ = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity ($V_i$) and output voltage ($V_o$) as a function of supply voltage ($V_P$). Measured at $f_i$ = 1 MHz in test circuit Fig. 10, for application $V_P$ = 6 V. Also shown is the sensitivity for $V_P$ = 4,5 V application (Fig. 16).

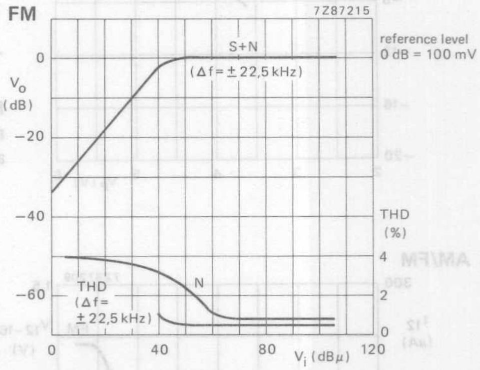
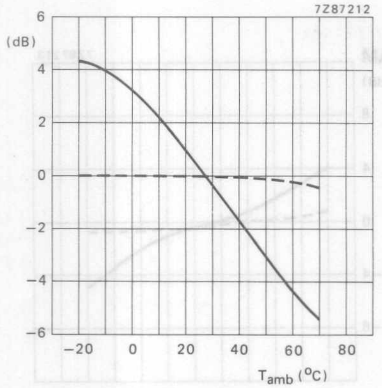



Fig. 6 Signal, noise and distortion as a function of input voltage ($V_i$). Measured at $f_i$ = 10,7 MHz in test circuit Fig. 10.

FM

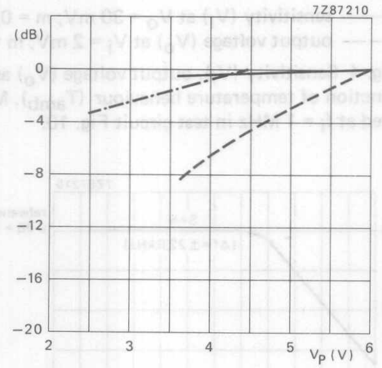



——— sensitivity at −3 dB limiting.

– – – output voltage ($V_o$) at $V_i$ = 1 mV; $\Delta f$ = ± 22 kHz.

Fig. 7 Sensitivity ($V_i$), output voltage ($V_o$) as a function of temperature behaviour ($T_{amb}$). Measured at $f_i$ = 10,7 MHz in test circuit Fig. 10.

FM




——— sensitivity at −3 dB limiting: $V_P$ = 6,0 V application.

–·–·– sensitivity at −3 dB limiting: $V_P$ = 4,5 V application.

– – – – output voltage ($V_o$) at $V_i$ = 1 mV; $\Delta f$ = ± 22,5 kHz.

Fig. 8 Sensitivity ($V_i$) and output voltage ($V_o$) as a function of supply voltage ($V_P$). Measured at $f_i$ = 10,7 MHz in test circuit Fig. 10.

AM/FM

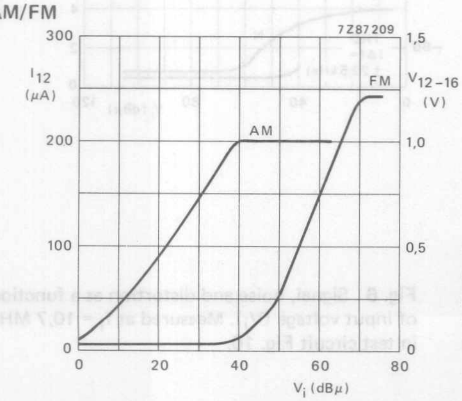



Fig. 9 Indicator output current ($I_{12}$) and d.c. output voltage ($V_{12\text{-}16}$): AM $f_i$ = 1 MHz; FM $f_i$ = 10,7 MHz as a function of input voltage ($V_i$). Measured in Fig. 10; $V_P$ = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

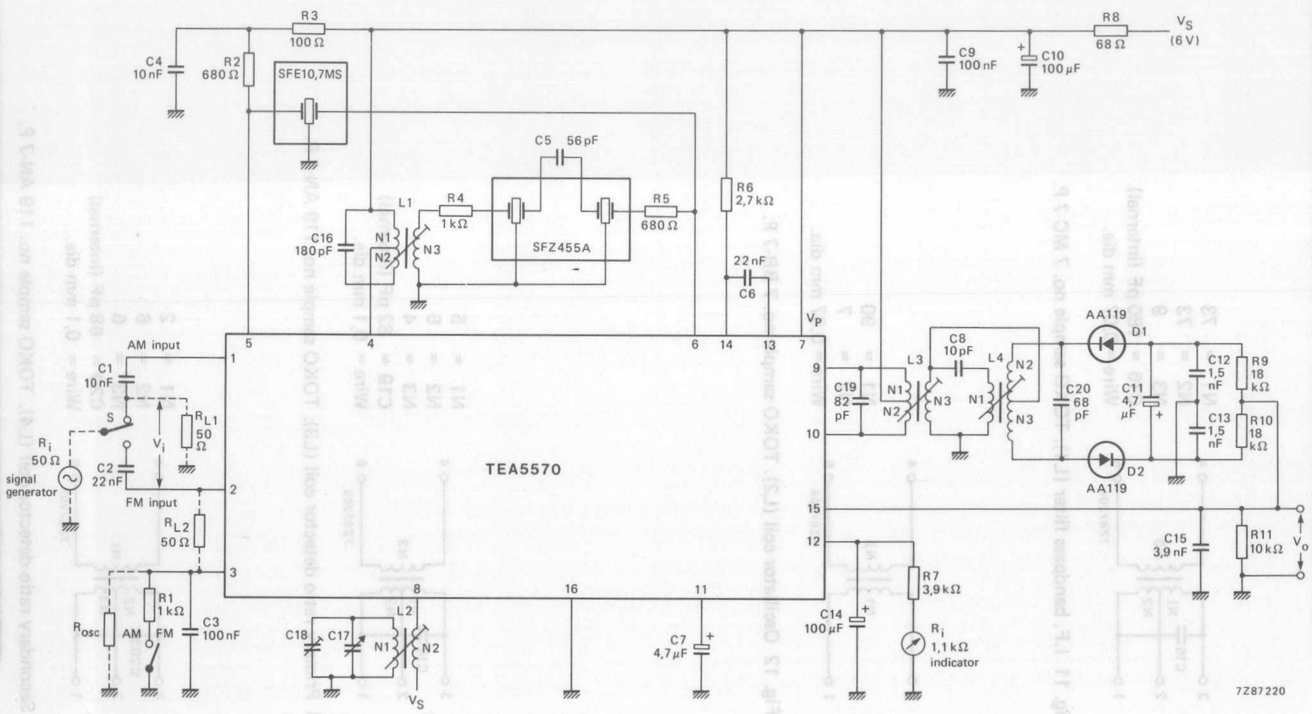


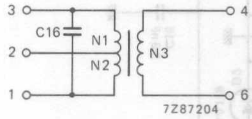

Fig. 10 Test circuit.

**Coil data**

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 =$ 2,7 kΩ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 =$ 275 Ω (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

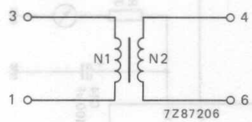
## COIL DATA

**AM i.f. coils** (Fig. 10)




N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

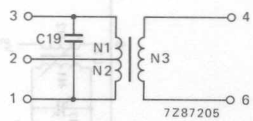
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.




N1 = 90
N2 = 7
Wire = 0,07 mm dia.

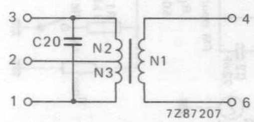
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

**FM i.f. coils** (Fig. 10)




N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

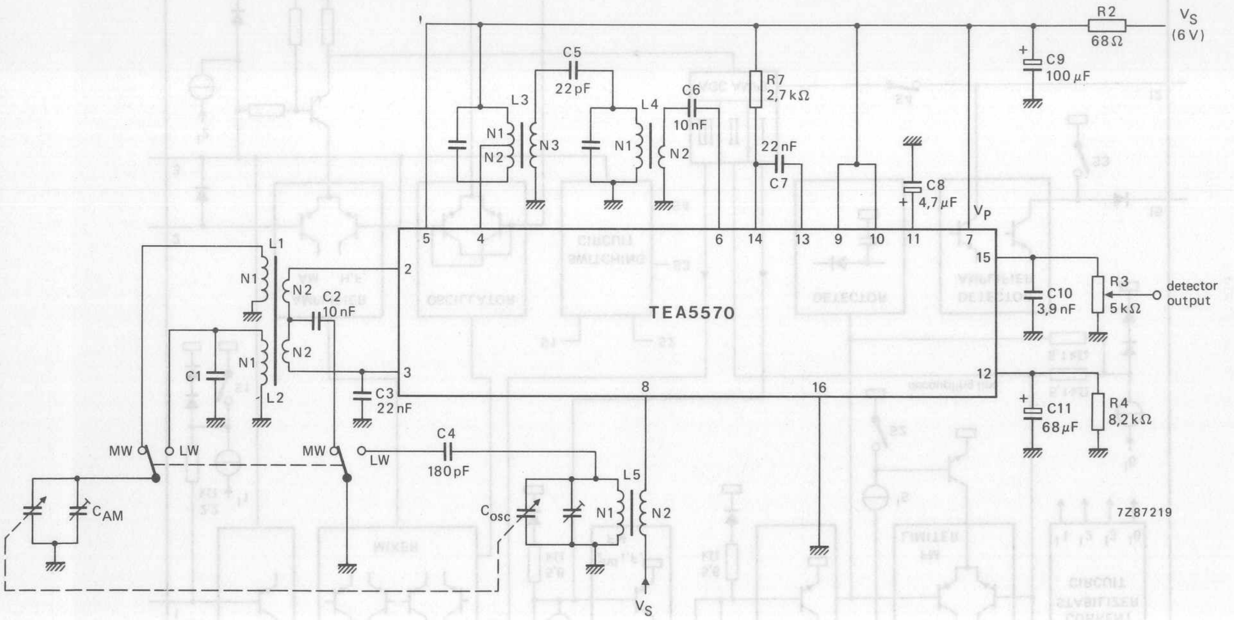



N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

## APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.




**Coil data**

| | | | |
|---|---|---|---|
| L3 | N1 = 73<br>N2 = 73<br>N3 = 9<br>C = 180 pF | L4 | N1 = 146<br>N2 = 9<br>C = 180 pF |
| L5 | N1 = 90<br>N2 = 6 | | |

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

APPLICATION INFORMATION (continued)

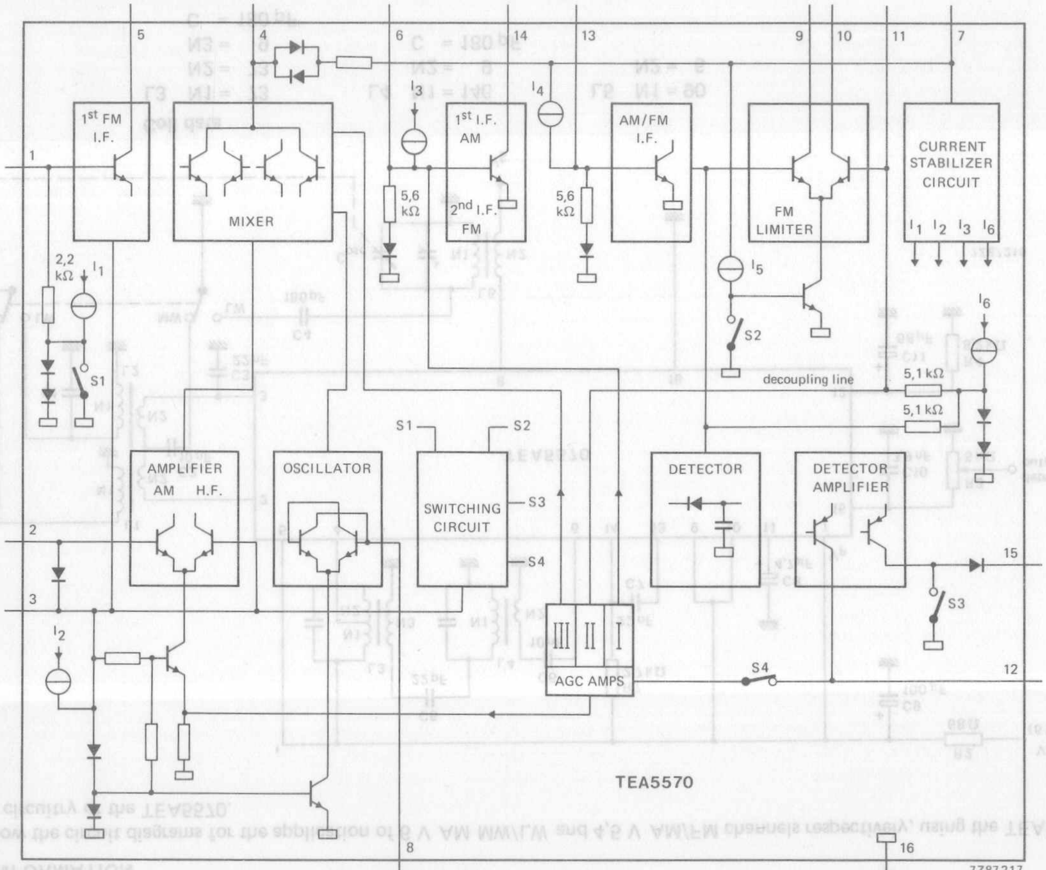
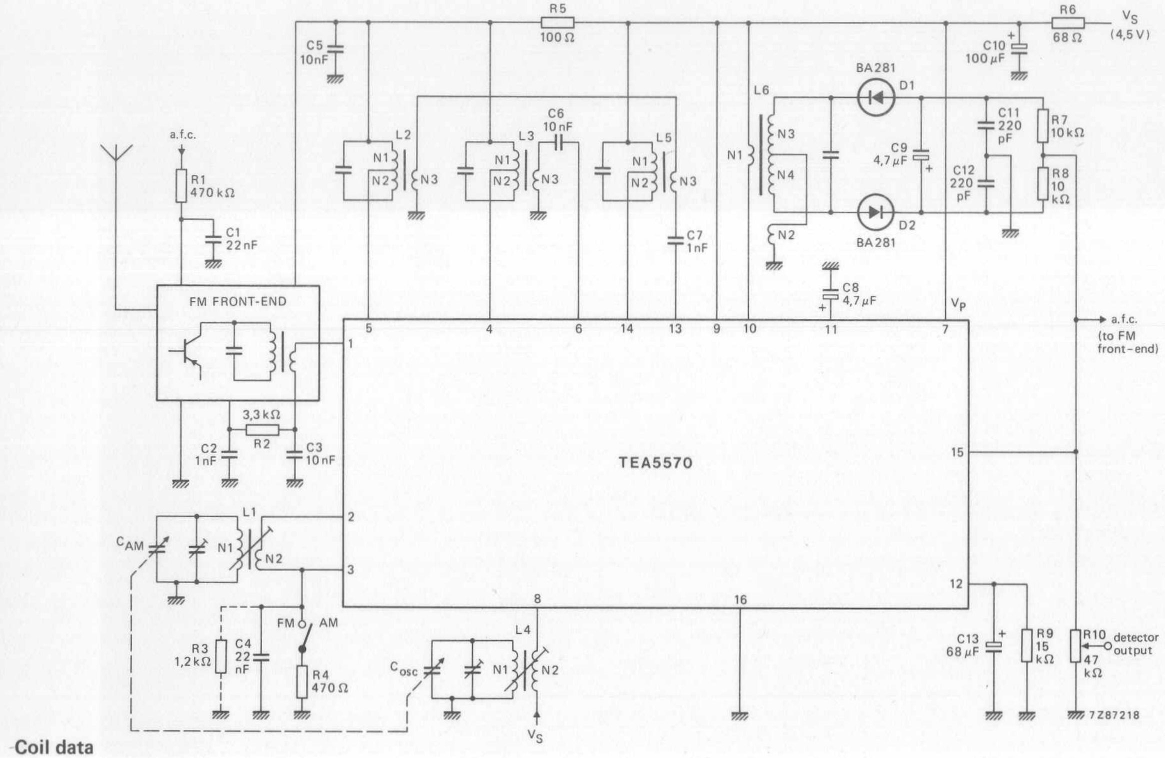



Fig. 16 TEA5570 circuit diagram.




**Coil data**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| L2 | N1 = 3 | L3 | N1 = 33 | L4 | N1 = 90 | L5 | N1 = 33 | L6 | N1 = 50 |
| | N2 = 8 | | N2 = 113 | | N2 = 6 | | N2 = 113 | | N2 = 50 |
| | N3 = 1 | | N3 = 9 | | | | N3 = 9 | | N3 = 4,5 |
| | C = 82 pF | | C = 180 pF | | | | | | N4 = 6,5 |
| | | | | | | | | | C = 82 pF |

Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

**DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.**

# PLL STEREO DECODER

The TEA5580 is a PLL stereo decoder. It is suitable for portable radios, radio recorders, medium-fi and car radio receivers. The circuit incorporates the following functions.

- **A voltage-controlled oscillator** (f = 228 kHz) from which the 19, 38, 57 and 114 kHz signals are obtained via $I^2L$ logic.
- **A phase-locked-loop system** to lock the VCO to the 19 kHz pilot tone in the stereo signal. The phase detector in the loop system also suppresses phase distortion due to the 57 kHz pilot signal from VWF transmitters (traffic warning system in Germany).
- **A pilot presence detector and an automatic mono/stereo switch.**
- **Two demodulators**, one driven by the 38 kHz decoding signal for the stereo matrix, the second driven by a 114 kHz signal which suppresses the third harmonic of the multiplex signal (MUX). These prevent distortion caused by strong adjacent transmitters.
- **A matrix and two output buffers**, for the left and right output signals.
- **An input amplifier**, the gain of which can be adjusted by the external input resistor.
- **A pilot cancelling circuit**, for extra suppression of the pilot signal.
- **An SDS circuit (signal dependent stereo)** for a smooth changeover from stereo to mono on weak signals.
- **A driver output stage** for a stereo LED indicator.
- **A stabilizer**, for operation over a wide supply voltage range.

The stereo decoder is compensated for a typical i.f. filter with a roll-off frequency of 50 kHz (2 dB down at 38 kHz).

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Applicable supply voltage range | $V_S$ | | 3,6 to 16 | V |
| Supply voltage (pin 9) | $V_P$ | nom. | 6 | V |
| Ambient temperature | $T_{amb}$ | typ. | 25 | °C |
| Total quiescent current | $I_{tot}$ | typ. | 10 | mA |
| Measured at $V_{i(p-p)}$ = 1 V (MUX with 27 mV pilot) | | | | |
| Overall gain | $G_o$ | typ. | 0 to 20 | dB |
| Output channel unbalance | $V_{1-5}/V_{2-5}$ | < | ± 1 | dB |
| Output voltage (r.m.s. value) | $V_{1-5}/V_{2-5}$ | typ. | 0,4 | V |
| Total harmonic distortion (300 Hz to 20 kHz) | THD | typ. | 0,2 | % |
| Signal-to-noise ratio, DIN A-curve | S/N | typ. | 80 | dB |
| Channel separation | $\alpha$ | typ. | 40 | dB |
| Carrier suppression at: f = 19 kHz (adjusted) | $\alpha_{19}$ | typ. | 50 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

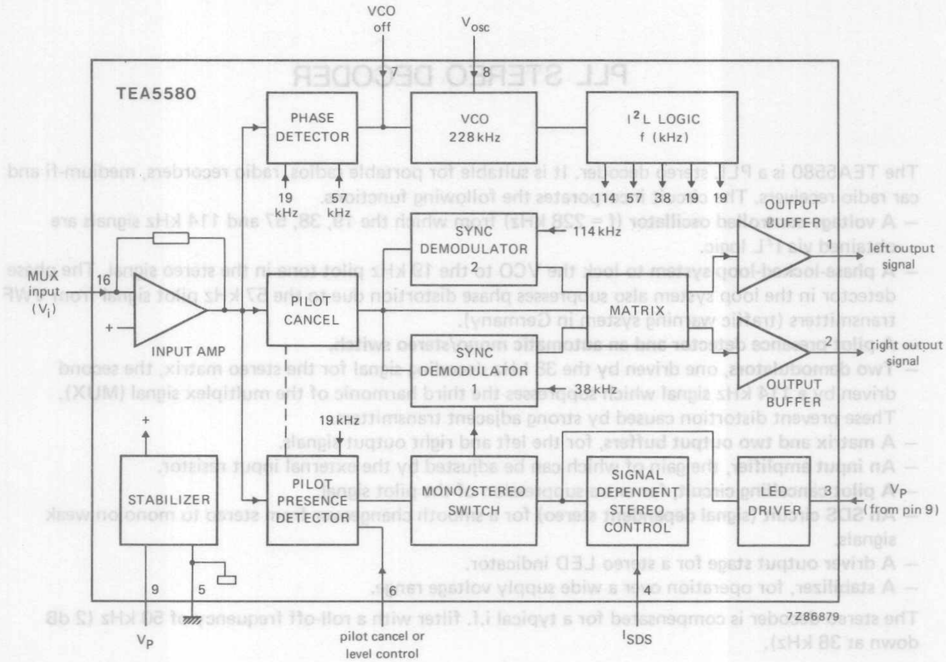



Fig. 1 Block diagram.

## A.C. CHARACTERISTICS

Measured in circuit of Fig. 2 at $V_P$ = 6 V, $V_{i(p-p)}$ = 1 V (MUX with 27 mV pilot)

| | | | | |
|---|---|---|---|---|
| Input impedance (external) | $\|Z_i\|$ | typ. | 47 | kΩ |
| Output impedance (external) | $\|Z_o\|$ | typ. | 5,1 | kΩ |
| Output voltage (r.m.s. value) | $V_{o(rms)}$ | typ. | 400 | mV |
| Total harmonic distortion (300 Hz to 10 kHz) (mono, stereo and mono + pilot) | THD | typ. | 0,2 | % |
| Total harmonic distortion at $V_{o(rms)}$ = 0,6 V | THD | < | 1 | % |
| Signal-to-noise ratio (DIN A-curve) | S/N | typ. | 80 | dB |
| Channel separation (for L = 1 and R = 0) | $\alpha$ | typ. | 40 | dB |
| SDS control | | | | |
| 10 dB channel separation | $I_4$ | typ. | 50 | μA |
| full stereo (channel separation ⩾ 26 dB) | $I_4$ | > | 100 | μA |
| full mono (channel separation ⩽ 1 dB) | $I_4$ | < | 10 | μA |
| Stereo/mono switch (for R2 = ▲kΩ) | | | | |
| for switching to stereo | $V_i$ | < | 18 | mV |
| for switching to mono | $V_i$ | > | 5 | mV |
| | | typ. | 13 | mV |
| hysteresis | $\Delta V_i$ | typ. | 2,5 | dB |
| VCO frequency (adjustable) | $f_{VCO}$ | typ. | 228 | kHz |
| Capture range (deviation from 228 kHz centre frequency) | | | | |
| $V_{pilot}$ = 32 mV | | typ. | 3,5 | % |
| Temperature coefficient (uncompensated) | TC | typ. | ▲ | kHz/K |
| VCO off switching voltage (pin 7) | $V_{off}$ | > | 3 | V |
| Carrier suppression (adjusted by R2) at: | | | | |
| f = 19 kHz | $\alpha_{19}$ | typ. | 50 | dB |
| f = 38 kHz | $\alpha_{38}$ | typ. | 50 | dB |
| f = 228 kHz | $\alpha_{228}$ | typ. | 70 | dB |
| ACI suppression at: * | | | | |
| f = 114 kHz | $\alpha_{114}$ | typ. | 80 | dB |
| f = 190 kHz | $\alpha_{190}$ | typ. | 60 | dB |
| SCA suppression at f = 67 kHz | $\alpha_{67}$ | typ. | 66 | dB |
| VWF suppression** | $\alpha_{VWF}$ | typ. | 70 | dB |
| Ripple rejection at f = 100 Hz | | | | |
| $V_S$ = 3,6 V | RR | typ. | 20 | dB |
| $V_S$ = 8 V | RR | typ. | 26 | dB |

* ACI suppression: $\alpha_{114} = 20 \log \frac{V_o \text{ (at 1 kHz)}}{V_o \text{ (at 4 kHz)}}$.

90% S-signal (L = –R, $f_m$ = 1 kHz); 9% pilot signal; 1% spurious signal (f = 110 kHz).

** VWF suppression: $\alpha_{VWF} = 20 \log \frac{V_o \text{ (at 1 kHz + 23 Hz)}}{V_o \text{ (at 1 kHz)}}$.

90% S-signal (L = –R, $f_m$ = 1 kHz); 9% pilot signal; 5% VWF signal (f = 57 kHz, $f_m$ = 23 Hz AM, m = 60%).

▲ Value to be established.

## APPLICATION INFORMATION

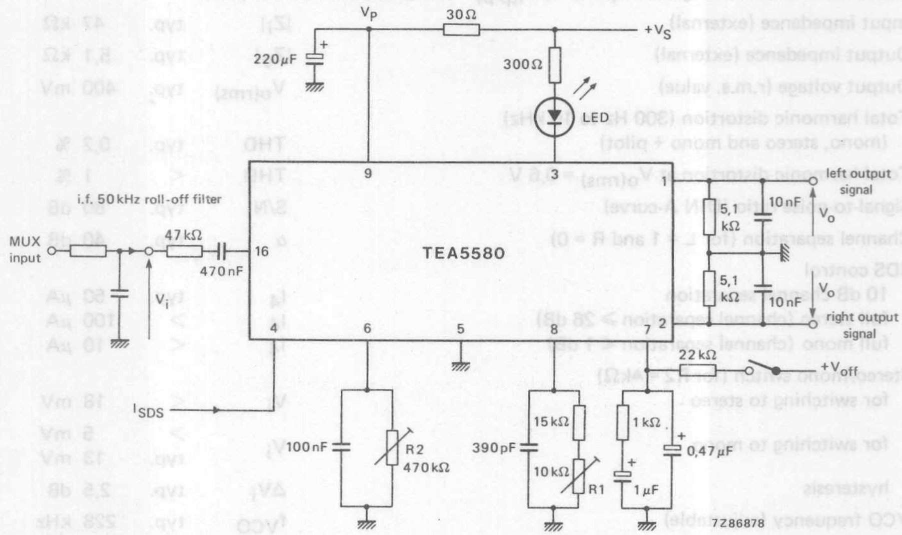



Fig. 2 Test and application diagram.

**Notes**

R1: VCO frequency adjustment; f = 228 kHz.
R2: pilot cancelling and pilot level.

# FM/IF SYSTEM

# AND MICROCOMPUTER-BASED TUNING INTERFACE

## GENERAL DESCRIPTION

The TEA6000 is an FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

### Features

- 3-stage IF limiter for driving a ratio detector
- 2-stage level detector with current output
- operational amplifier for active filtering (e.g. multipath detector)
- high resolution frequency counter for FM and AM IF-signals
- time base reference from crystal oscillator or external source (SAA1057)
- serial two wire bidirectional computer interface ($I^2C$-bus)
- multiplexed 3 bit A/D converter for two input signals
- software controlled sensitivity for both ADC inputs

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltages ($V_{P1}$ and $V_{P2}$) | $V_P$ | typ. | 8,4 | V |
| Supply current; ($I_{P1} + I_{P2}$) | $I_P$ | typ. | 36 | mA |
| FM/IF sensitivity | | | | |
| at −3 dB before limiting | $V_i$ | typ. | 150 | μV |
| Signal to noise ratio for $V_i$ = 10 mV | S/N | typ. | 80 | dB |
| Audio output voltage | | | | |
| Δf = 22,5 kHz; $V_i$ = 1 mV | $V_O$ | typ. | 170 | mV |
| Δf = 75 kHz; $V_i$ = 1 mV | $V_O$ | typ. | 520 | mV |
| AM suppression at $V_i$ = 10 mV | AMS | typ. | 58 | dB |
| Frequency counter sensitivity | | | | |
| AM (pin 18) | $V_{i(am)}$ | typ. | 60 | μV |
| FM (pin 16) | $V_{i(fm)}$ | typ. | 80 | μV |
| Resolution frequency counter | | | | |
| AM | $f_{s(am)}$ | typ. | 250 | Hz |
| FM | $f_{s(fm)}$ | typ. | 6,4 | kHz |
| Power dissipation | $P_{tot}$ | max. | 1300 | mW |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 85 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

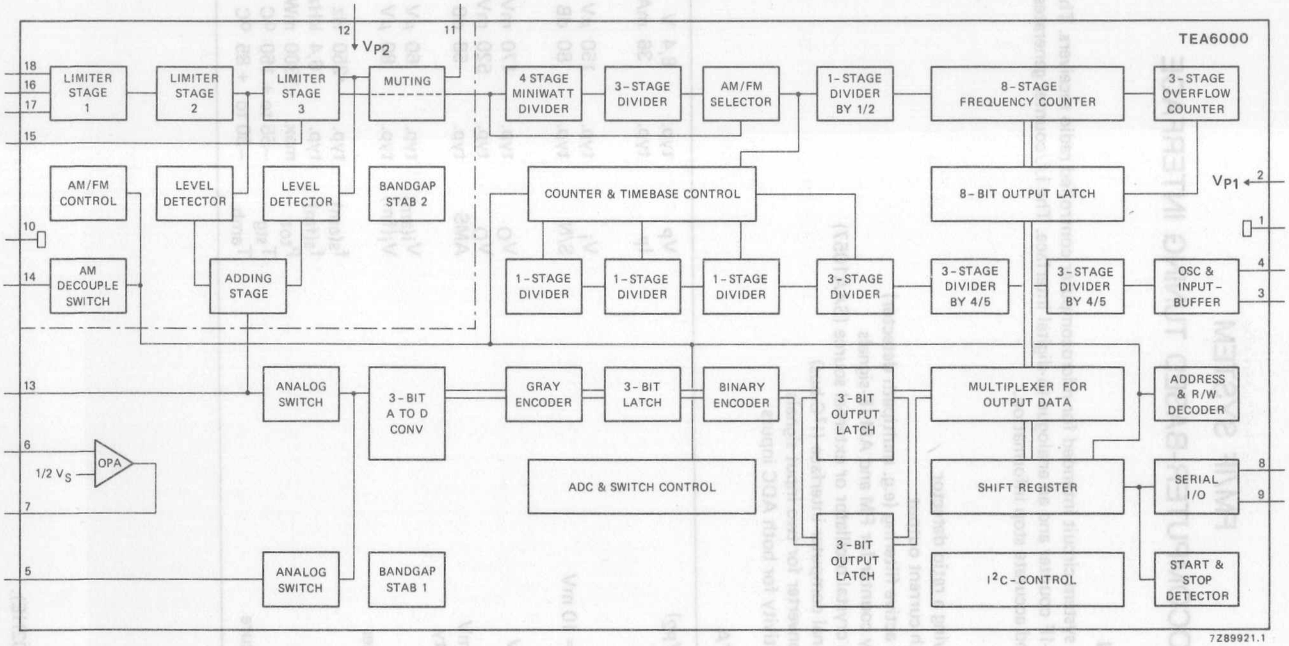



Fig. 1 Block diagram.

## FUNCTIONAL DESCRIPTION

The IF SECTION consists of three balanced differential stages with separated FM and AM inputs, directly coupled by emitter followers. The last stage also has separated outputs, which are intended for driving a ratio detector and the frequency measuring system respectively.

The last two stages are coupled via low-value capacitors to two LEVEL DETECTORS which generate a signal-dependent d.c. current for controlling channel separation and frequency response of a stereo decoder, multipath detector circuitry, AGC and the internal ADC.

The IF MUTING circuit has been incorporated to decrease the interstation noise by about 15 dB.

The 3-bit A/D CONVERTER has two inputs, which are selected via two multiplexed analogue switches. One of these switches is internally connected to the level detector output but can also serve as an external input, as the level detector output can be switched off. The outputs of the ADC are converted to a Gray code, latched and reconverted to a binary code to obtain glitch-free output data. The sensitivity of both inputs can be selected independently via software on two levels.

The reference for the ADC is derived from a BAND-GAP STABILIZER circuit. Multipath distortion on FM will generate an AM modulation on the d.c. voltage from the level detectors. This AM modulation can be filtered and rectified to obtain a multipath-dependent d.c. voltage. This voltage can be applied to the other input of the ADC.

To facilitate filtering an OPERATIONAL AMPLIFIER (OPA) is incorporated on the chip. The typical circuit diagram for a multipath filter is given in Fig. 4.

The FREQUENCY COUNTER is preceded by a 7-stage prescaler for FM, and FM/AM selector stage and a divider by 1 or 2. The actual counter is a presetable and resetable 8-stage counter with a 3-stage data disable overflow counter, which can be switched off. The eight significant output bits are situated symmetrically around 10,7 MHz and 460 kHz, when the external timebase source is used (e.g. SAA1057). See Table 1.

The reference for the TIMEBASE is primarily thought to be the SAA1057. This circuit generates from its 4 MHz crystal oscillator a 32 or 40 kHz signal. This signal is buffered and applied to the timebase circuitry (mode I). The circuit diagram for this mode I is given in Fig. 5a.
In the timebase, the selection is made for reference frequency (32 to 40 kHz), FM or AM mode and the width of the measuring window, all under software control. Accuracy ± ½ bit when the window is set to wide (see Fig. 2) and ± 1 bit when set to narrow. A special feature is the synchronization of the measuring cycle with the input DATA of the $I^2C$-bus, meaning the measuring cycle starts immediately after a "WRITE" instruction via the $I^2C$-bus.

For those who do not use the SAA1057 as reference, a $2^{15}$ Hz crystal (32 768 Hz) can be connected to the reference inputs directly, obtaining a quartz-oscillator reference. See Fig. 5b for the circuit diagram for this mode II.

When the circuit is used in mode II a correction has to be made to the values of window width and resolution as the cheap watch crystals differ by about 2,4% from the frequency generated by the SAA1057 (32 768 and 32 000 kHz respectively) See Table 2.

Communication between MUSTI and the microcomputer is accomplished via the two-wire bidirectional $I^2C$-bus (slave transceiver version); the SDA (serial data) and SCL (serial clock).

To prevent crosstalk between the digital and analogue parts of the circuit the power supply lines are fully isolated.

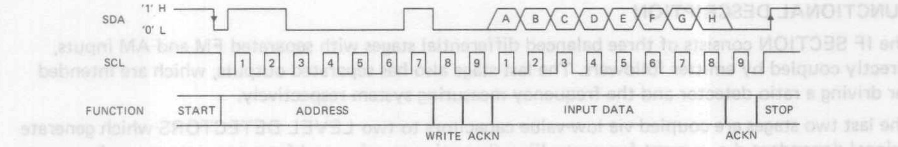



Fig. 2 Input data format waveforms.

**Input bits**

| bit | function | "0" | "1" | reference to Fig. 2 |
|---|---|---|---|---|
| 1 | reference frequency | 32 kHz | 40 kHz | A |
| 2 | sensitivity ADC2 | LOW | HIGH | B |
| 3 | sensitivity ADC1 | LOW | HIGH | C |
| 4 | level detector output | off | on | D |
| 5 | AM/FM | AM | FM | E |
| 6 | overflow counter | off | on | F |
| 7 | measuring window | narrow | wide | G |
| 8 | test mode | off | on | H |

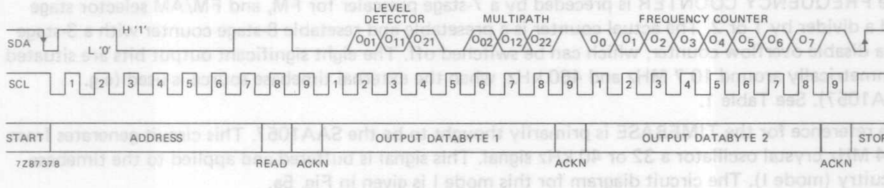



Fig. 3 Output data format waveforms.

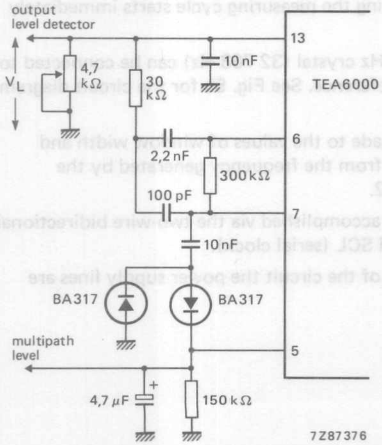



Fig. 4 Multipath detector circuit.

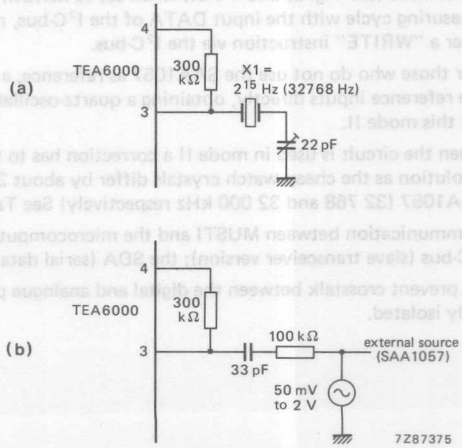



Fig. 5 Oscillator/buffer circuits.
X1 = $2^{15}$ Hz (32 768 Hz).

DEVELOPMENT DATA

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | | | |
| pin 2 | $V_{P1}$ | max. | 13,2 V |
| pin 12 | $V_{P2}$ | max. | 13,2 V |
| Power dissipation | $P_{tot}$ | max. | 1300 mW |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 85 °C |

## THERMAL RESISTANCE

From crystal to ambient $R_{th\ c\text{-}a}$ = 50 K/W

## D.C. CHARACTERISTICS

$V_{P1} = V_{P2} = 8{,}4$ V; $T_{amb} = 25$ °C, unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | | | | | |
| (pin 2) | $V_{P1}$ | 7,6 | 8,4 | 9,2 | V |
| (pin 12) | $V_{P2}$ | 7,6 | 8,4 | 9,2 | V |
| Supply current AM mode | | | | | |
| pin 2 | $I_{P1}$ | – | 18,5 | – | mA |
| pin 12 | $I_{P2}$ | – | 17,4 | – | mA |
| Supply current FM mode | | | | | |
| pin 2 | $I_{P1}$ | – | 19,2 | – | mA |
| pin 12 | $I_{P2}$ | – | 16,4 | – | mA |
| Power dissipation | $P_{tot}$ | – | 350 | – | mW |

## A.C. CHARACTERISTICS (see Fig. 6)

$V_{P1} = V_{P2} = 8{,}4$ V; $V_{16\text{-}10} = 1$ mV; f = 10,7 MHz; Δf = 22,5 kHz; $f_m = 1$ kHz; unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Sensitivity | | | | | |
| at −3 dB before limiting | $V_{I(FM)}$ | – | 150 | – | μV |
| Signal-to-noise ratio, FM input | | | | | |
| $V_i$ = 20 μV | S/N | 40 | 46 | – | dB |
| $V_i$ = 150 μV | S/N | – | 64 | – | dB |
| $V_i$ = 1 mV | S/N | – | 76 | – | dB |
| $V_i$ = 10 mV | S/N | – | 80 | – | dB |
| Noise output voltage | | | | | |
| $V_i$ = 0 V; with muting, switch S1 on | $V_{no}$ | – | 55 | – | μV |
| $V_i$ = 0 V; without muting, S1 off | $V_{no}$ | – | 420 | – | μV |
| Audio output voltage | | | | | |
| Δf = 22,5 kHz | $V_O$ | – | 170 | – | mV |
| Δf = 75 kHz | $V_O$ | – | 520 | – | mV |

**A.C. CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| AM suppression | | | | | |
| ratio of the AM output signal referred to the FM signal (m = 0,3) | | | | | |
| $V_i$ = 150 $\mu$V | AMS | – | 46 | – | dB |
| $V_i$ = 1 mV | AMS | – | 62 | – | dB |
| $V_i$ = 10 mV | AMS | – | 58 | – | dB |
| $V_i$ = 100 mV | AMS | – | 60 | – | dB |
| Level detector output voltage (Fig. 4) | | | | | |
| $R_{13\text{-}10}$ = 4,7 k$\Omega$; $V_i$ = 10 mV, FM mode | $V_L$ | – | 6,2 | – | V |
| Level detector output voltage slope | | | | | |
| $R_{13\text{-}10}$ adjusted in FM mode for $V_L$ = 5,5 V at $V_i$ = 10 mV; f = 10,7 MHz | | | | | |
| $V_i$ = 0 V (pin 16) | $V_{L(FM)}$ | – | 130 | – | mV |
| $V_i$ = 140 $\mu$V | $V_{L(FM)}$ | – | 1,3 | – | V |
| $V_i$ = 1 mV | $V_{L(FM)}$ | – | 2,7 | – | V |
| $V_i$ = 3 mV | $V_{L(FM)}$ | – | 4,4 | – | V |
| $R_{13\text{-}10}$ adjusted in FM mode (see above) | | | | | |
| $V_i$ = 0 V, f = 460 kHz (pin 18) | $V_{L(AM)}$ | – | 200 | – | mV |
| $V_i$ = 1 mV, f = 460 kHz (pin 18) | $V_{L(AM)}$ | – | 1,4 | – | V |
| $V_i$ = 10 mV, f = 460 kHz (pin 18) | $V_{L(AM)}$ | – | 2,7 | – | V |
| Frequency counter sensitivity | | | | | |
| AM input voltage (pin 18) | $V_{I(AM)}$ | – | 60 | – | $\mu$V |
| FM input voltage (pin 16) | $V_{I(FM)}$ | – | 80 | – | $\mu$V |
| AM input impedance | $R_i$ | – | 30 | – | k$\Omega$ |
| BUS inputs | | | | | |
| SDA and SCL (pins 9 and 8) | | | | | |
| input voltage HIGH | $V_{IH}$ | 3,0 | – | $V_{P1}$ | V |
| input voltage LOW | $V_{IL}$ | –0,3 | – | 1,5 | V |
| input current HIGH | $I_{IH}$ | – | – | 10 | $\mu$A |
| input current LOW | $I_{IL}$ | – | – | 10 | $\mu$A |
| acknowledge sink current | $I_{ack}$ | – | – | 2 | mA |
| maximum input frequency | $f_{i\,max}$ | 100 | – | – | kHz |
| Output voltage SDA | | | | | |
| HIGH; 4 k$\Omega$ to 8,4 V | $V_{OH}$ | 8,0 | – | – | V |
| LOW; I = 2 mA | $V_{OL}$ | – | – | 0,4 | V |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| A/D converter (pin 5 and 13) | | | | | |
| input resistance | $R_i$ | | t.b.f. | | kΩ |
| input capacitance | $C_i$ | | t.b.f. | | pF |
| Trip levels, sensitivity bit HIGH | | | | | |
| level 1 | $V_T$ | – | 0,6 | – | V |
| level 2 | $V_T$ | – | 1,06 | – | V |
| level 3 | $V_T$ | – | 1,38 | – | V |
| level 4 | $V_T$ | – | 1,84 | – | V |
| level 5 | $V_T$ | – | 2,14 | – | V |
| level 6 | $V_T$ | – | 2,55 | – | V |
| level 7 | $V_T$ | – | 2,97 | – | V |
| Trip levels, sensitivity bit LOW | | | | | |
| level 1 | $V_T$ | – | 0,96 | – | V |
| level 2 | $V_T$ | – | 1,78 | – | V |
| level 3 | $V_T$ | – | 2,44 | – | V |
| level 4 | $V_T$ | – | 3,26 | – | V |
| level 5 | $V_T$ | – | 3,92 | – | V |
| level 6 | $V_T$ | – | 4,63 | – | V |
| level 7 | $V_T$ | – | 5,38 | – | V |
| Crystal oscillator (see Fig. 5) | | | | | |
| reference frequency | $f_{ref}$ | 32 | 32,768 | 40 | kHz |
| temperature coefficient | TC | | t.b.f. | | $10^{-6}$ |
| input resistance | $R_i$ | | t.b.f. | | kΩ |
| input capacitance | $C_i$ | | t.b.f. | | pF |
| Operational amplifier (pins 6 and 7) | | | | | |
| voltage gain | $G_V$ | – | $10^4$ | – | |
| input bias current | $I_{bias}$ | – | 30 | 100 | nA |
| output sink current at $V_o = 1$ V | $I_o$ | – | 0,2 | – | mA |
| output source current at $V_o = 7,4$ V | $I_o$ | 5,5 | 10 | – | mA |
| output voltage swing | $V_{7(p\text{-}p)}$ | – | 5,5 | – | V |
| Frequency measuring system (see pages 8 and 9) | | | | | |
| measuring windows; $f_{ref}$ = 32 or 40 kHz | | | | | |
| AM | | | | | |
| window "0" (LOW) | $t_{gate}$ | – | 4 | – | ms |
| window "1" (HIGH) | $t_{gate}$ | – | 8 | – | ms |
| FM | | | | | |
| window "0" (LOW) | $t_{gate}$ | – | 20 | – | ms |
| window "1" (HIGH) | $t_{gate}$ | – | 40 | – | ms |
| resolution frequency counter | | | | | |
| AM | $f_{s(am)}$ | – | 250 | – | Hz |
| FM | $f_{s(fm)}$ | – | 6,4 | – | kHz |

$t_{gate}$ has to be multiplied by 32 000/32 768 for a $f_{ref}$ of $2^{15}$ Hz.
$f_s$ has to be multiplied by 32 768/32 000 for a $f_{ref}$ of $2^{15}$ Hz.

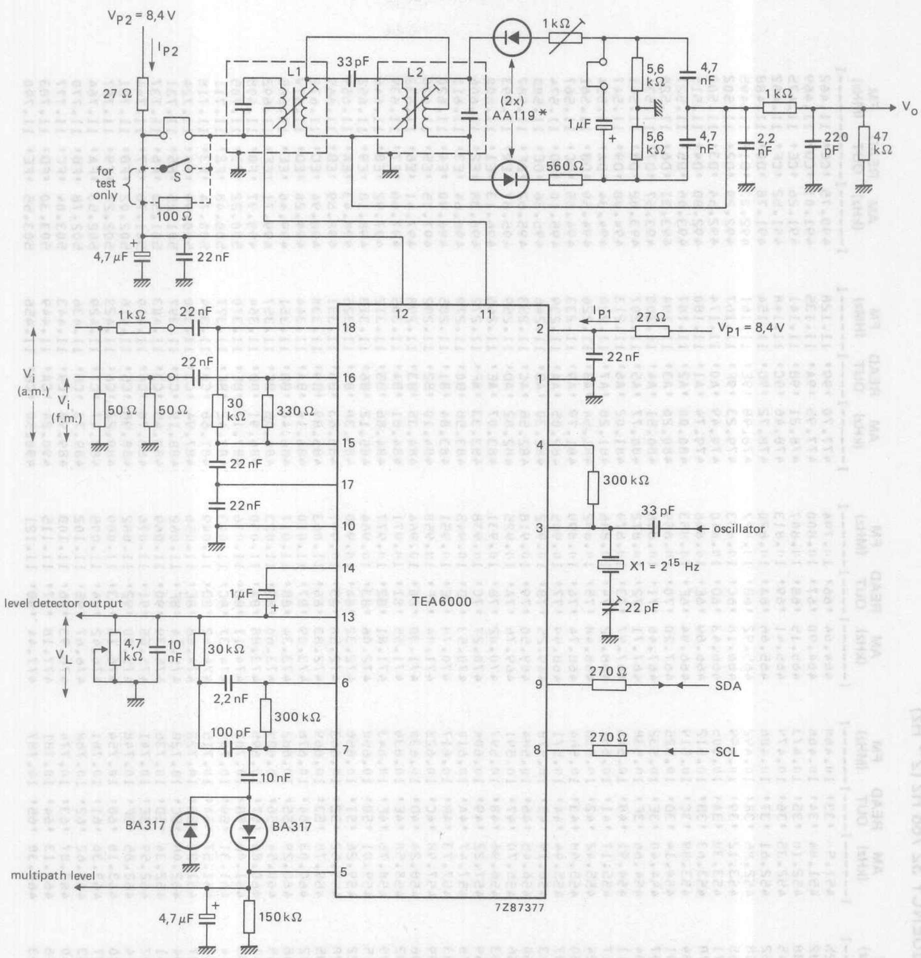
DEVELOPMENT DATA

TABLE 1 REFERENCE FREQUENCY 32 000 Hz (SAA1057)

| AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 428.25 | '00' | 9.888 | 441.00 | '33' | 10.214 | 453.75 | '66' | 10.541 | 466.50 | '99' | 10.867 | 479.25 | 'CC' | 11.194 |
| 428.50 | '01' | 9.894 | 441.25 | '34' | 10.221 | 454.00 | '67' | 10.547 | 466.75 | '9A' | 10.874 | 479.50 | 'CD' | 11.200 |
| 428.75 | '02' | 9.901 | 441.50 | '35' | 10.227 | 454.25 | '68' | 10.554 | 467.00 | '9B' | 10.880 | 479.75 | 'CE' | 11.206 |
| 429.00 | '03' | 9.907 | 441.75 | '36' | 10.234 | 454.50 | '69' | 10.560 | 467.25 | '9C' | 10.886 | 480.00 | 'CF' | 11.213 |
| 429.25 | '04' | 9.914 | 442.00 | '37' | 10.240 | 454.75 | '6A' | 10.566 | 467.50 | '9D' | 10.893 | 480.25 | 'D0' | 11.219 |
| 429.50 | '05' | 9.920 | 442.25 | '38' | 10.246 | 455.00 | '6B' | 10.573 | 467.75 | '9E' | 10.899 | 480.50 | 'D1' | 11.226 |
| 429.75 | '06' | 9.926 | 442.50 | '39' | 10.253 | 455.25 | '6C' | 10.579 | 468.00 | '9F' | 10.906 | 480.75 | 'D2' | 11.232 |
| 430.00 | '07' | 9.933 | 442.75 | '3A' | 10.259 | 455.50 | '6D' | 10.586 | 468.25 | 'A0' | 10.912 | 481.00 | 'D3' | 11.238 |
| 430.25 | '08' | 9.939 | 443.00 | '3B' | 10.266 | 455.75 | '6E' | 10.592 | 468.50 | 'A1' | 10.918 | 481.25 | 'D4' | 11.245 |
| 430.50 | '09' | 9.946 | 443.25 | '3C' | 10.272 | 456.00 | '6F' | 10.598 | 468.75 | 'A2' | 10.925 | 481.50 | 'D5' | 11.251 |
| 430.75 | '0A' | 9.952 | 443.50 | '3D' | 10.278 | 456.25 | '70' | 10.605 | 469.00 | 'A3' | 10.931 | 481.75 | 'D6' | 11.258 |
| 431.00 | '0B' | 9.958 | 443.75 | '3E' | 10.285 | 456.50 | '71' | 10.611 | 469.25 | 'A4' | 10.938 | 482.00 | 'D7' | 11.264 |
| 431.25 | '0C' | 9.965 | 444.00 | '3F' | 10.291 | 456.75 | '72' | 10.618 | 469.50 | 'A5' | 10.944 | 482.25 | 'D8' | 11.270 |
| 431.50 | '0D' | 9.971 | 444.25 | '40' | 10.298 | 457.00 | '73' | 10.624 | 469.75 | 'A6' | 10.950 | 482.50 | 'D9' | 11.277 |
| 431.75 | '0E' | 9.978 | 444.50 | '41' | 10.304 | 457.25 | '74' | 10.630 | 470.00 | 'A7' | 10.957 | 482.75 | 'DA' | 11.283 |
| 432.00 | '0F' | 9.984 | 444.75 | '42' | 10.310 | 457.50 | '75' | 10.637 | 470.25 | 'A8' | 10.963 | 483.00 | 'DB' | 11.290 |
| 432.25 | '10' | 9.990 | 445.00 | '43' | 10.317 | 457.75 | '76' | 10.643 | 470.50 | 'A9' | 10.970 | 483.25 | 'DC' | 11.296 |
| 432.50 | '11' | 9.997 | 445.25 | '44' | 10.323 | 458.00 | '77' | 10.650 | 470.75 | 'AA' | 10.976 | 483.50 | 'DD' | 11.302 |
| 432.75 | '12' | 10.003 | 445.50 | '45' | 10.330 | 458.25 | '78' | 10.656 | 471.00 | 'AB' | 10.982 | 483.75 | 'DE' | 11.309 |
| 433.00 | '13' | 10.010 | 445.75 | '46' | 10.336 | 458.50 | '79' | 10.662 | 471.25 | 'AC' | 10.989 | 484.00 | 'DF' | 11.315 |
| 433.25 | '14' | 10.016 | 446.00 | '47' | 10.342 | 458.75 | '7A' | 10.669 | 471.50 | 'AD' | 10.995 | 484.25 | 'E0' | 11.322 |
| 433.50 | '15' | 10.022 | 446.25 | '48' | 10.349 | 459.00 | '7B' | 10.675 | 471.75 | 'AE' | 11.002 | 484.50 | 'E1' | 11.328 |
| 433.75 | '16' | 10.029 | 446.50 | '49' | 10.355 | 459.25 | '7C' | 10.682 | 472.00 | 'AF' | 11.008 | 484.75 | 'E2' | 11.334 |
| 434.00 | '17' | 10.035 | 446.75 | '4A' | 10.362 | 459.50 | '7D' | 10.688 | 472.25 | 'B0' | 11.014 | 485.00 | 'E3' | 11.341 |
| 434.25 | '18' | 10.042 | 447.00 | '4B' | 10.368 | 459.75 | '7E' | 10.694 | 472.50 | 'B1' | 11.021 | 485.25 | 'E4' | 11.347 |
| 434.50 | '19' | 10.048 | 447.25 | '4C' | 10.374 | 460.00 | '7F' | 10.701 | 472.75 | 'B2' | 11.027 | 485.50 | 'E5' | 11.354 |
| 434.75 | '1A' | 10.054 | 447.50 | '4D' | 10.381 | 460.25 | '80' | 10.707 | 473.00 | 'B3' | 11.034 | 485.75 | 'E6' | 11.360 |
| 435.00 | '1B' | 10.061 | 447.75 | '4E' | 10.387 | 460.50 | '81' | 10.714 | 473.25 | 'B4' | 11.040 | 486.00 | 'E7' | 11.366 |
| 435.25 | '1C' | 10.067 | 448.00 | '4F' | 10.394 | 460.75 | '82' | 10.720 | 473.50 | 'B5' | 11.046 | 486.25 | 'E8' | 11.373 |
| 435.50 | '1D' | 10.074 | 448.25 | '50' | 10.400 | 461.00 | '83' | 10.726 | 473.75 | 'B6' | 11.053 | 486.50 | 'E9' | 11.379 |
| 435.75 | '1E' | 10.080 | 448.50 | '51' | 10.406 | 461.25 | '84' | 10.733 | 474.00 | 'B7' | 11.059 | 486.75 | 'EA' | 11.386 |
| 436.00 | '1F' | 10.086 | 448.75 | '52' | 10.413 | 461.50 | '85' | 10.739 | 474.25 | 'B8' | 11.066 | 487.00 | 'EB' | 11.392 |
| 436.25 | '20' | 10.093 | 449.00 | '53' | 10.419 | 461.75 | '86' | 10.746 | 474.50 | 'B9' | 11.072 | 487.25 | 'EC' | 11.398 |
| 436.50 | '21' | 10.099 | 449.25 | '54' | 10.426 | 462.00 | '87' | 10.752 | 474.75 | 'BA' | 11.078 | 487.50 | 'ED' | 11.405 |
| 436.75 | '22' | 10.106 | 449.50 | '55' | 10.432 | 462.25 | '88' | 10.758 | 475.00 | 'BB' | 11.085 | 487.75 | 'EE' | 11.411 |
| 437.00 | '23' | 10.112 | 449.75 | '56' | 10.438 | 462.50 | '89' | 10.765 | 475.25 | 'BC' | 11.091 | 488.00 | 'EF' | 11.418 |
| 437.25 | '24' | 10.118 | 450.00 | '57' | 10.445 | 462.75 | '8A' | 10.771 | 475.50 | 'BD' | 11.098 | 488.25 | 'F0' | 11.424 |
| 437.50 | '25' | 10.125 | 450.25 | '58' | 10.451 | 463.00 | '8B' | 10.778 | 475.75 | 'BE' | 11.104 | 488.50 | 'F1' | 11.430 |
| 437.75 | '26' | 10.131 | 450.50 | '59' | 10.458 | 463.25 | '8C' | 10.784 | 476.00 | 'BF' | 11.110 | 488.75 | 'F2' | 11.437 |
| 438.00 | '27' | 10.138 | 450.75 | '5A' | 10.464 | 463.50 | '8D' | 10.790 | 476.25 | 'C0' | 11.117 | 489.00 | 'F3' | 11.443 |
| 438.25 | '28' | 10.144 | 451.00 | '5B' | 10.470 | 463.75 | '8E' | 10.797 | 476.50 | 'C1' | 11.123 | 489.25 | 'F4' | 11.450 |
| 438.50 | '29' | 10.150 | 451.25 | '5C' | 10.477 | 464.00 | '8F' | 10.803 | 476.75 | 'C2' | 11.130 | 489.50 | 'F5' | 11.456 |
| 438.75 | '2A' | 10.157 | 451.50 | '5D' | 10.483 | 464.25 | '90' | 10.810 | 477.00 | 'C3' | 11.136 | 489.75 | 'F6' | 11.462 |
| 439.00 | '2B' | 10.163 | 451.75 | '5E' | 10.490 | 464.50 | '91' | 10.816 | 477.25 | 'C4' | 11.142 | 490.00 | 'F7' | 11.469 |
| 439.25 | '2C' | 10.170 | 452.00 | '5F' | 10.496 | 464.75 | '92' | 10.822 | 477.50 | 'C5' | 11.149 | 490.25 | 'F8' | 11.475 |
| 439.50 | '2D' | 10.176 | 452.25 | '60' | 10.502 | 465.00 | '93' | 10.829 | 477.75 | 'C6' | 11.155 | 490.50 | 'F9' | 11.482 |
| 439.75 | '2E' | 10.182 | 452.50 | '61' | 10.509 | 465.25 | '94' | 10.835 | 478.00 | 'C7' | 11.162 | 490.75 | 'FA' | 11.488 |
| 440.00 | '2F' | 10.189 | 452.75 | '62' | 10.515 | 465.50 | '95' | 10.842 | 478.25 | 'C8' | 11.168 | 491.00 | 'FB' | 11.494 |
| 440.25 | '30' | 10.195 | 453.00 | '63' | 10.522 | 465.75 | '96' | 10.848 | 478.50 | 'C9' | 11.174 | 491.25 | 'FC' | 11.501 |
| 440.50 | '31' | 10.202 | 453.25 | '64' | 10.528 | 466.00 | '97' | 10.854 | 478.75 | 'CA' | 11.181 | 491.50 | 'FD' | 11.507 |
| 440.75 | '32' | 10.208 | 453.50 | '65' | 10.534 | 466.25 | '98' | 10.861 | 479.00 | 'CB' | 11.187 | 491.75 | 'FE' | 11.514 |

TABLE 2 REFERENCE FREQUENCY 32 768 Hz ($2^{15}$ Hz)

| AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (MHz) | AM (kHz) | READ OUT | FM (HMz) | AM (kHz) | READ OUT | FM (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 438.53 | '00' | 10.125 | 451.5[illegible] | '33' | 10.460 | 464.64 | '66' | 10.794 | 477.70 | '99' | 11.128 | 490.75 | 'CC' | 11.462 |
| 438.78 | '01' | 10.132 | 451.84 | '34' | 10.466 | 464.90 | '67' | 10.800 | 477.95 | '9A' | 11.135 | 491.01 | 'CD' | 11.469 |
| 439.04 | '02' | 10.138 | 452.10 | '35' | 10.473 | 465.15 | '68' | 10.807 | 478.21 | '9B' | 11.141 | 491.26 | 'CE' | 11.475 |
| 439.30 | '03' | 10.145 | 452.35 | '36' | 10.479 | 465.41 | '69' | 10.813 | 478.46 | '9C' | 11.148 | 491.52 | 'CF' | 11.482 |
| 439.55 | '04' | 10.152 | 452.61 | '37' | 10.486 | 465.66 | '6A' | 10.820 | 478.72 | '9D' | 11.154 | 491.78 | 'D0' | 11.488 |
| 439.81 | '05' | 10.158 | 452.86 | '38' | 10.492 | 465.92 | '6B' | 10.827 | 478.98 | '9E' | 11.161 | 492.03 | 'D1' | 11.495 |
| 440.06 | '06' | 10.165 | 453.12 | '39' | 10.499 | 466.18 | '6C' | 10.833 | 479.23 | '9F' | 11.167 | 492.29 | 'D2' | 11.502 |
| 440.32 | '07' | 10.171 | 453.38 | '3A' | 10.505 | 466.43 | '6D' | 10.840 | 479.49 | 'A0' | 11.174 | 492.54 | 'D3' | 11.508 |
| 440.58 | '08' | 10.178 | 453.63 | '3B' | 10.512 | 466.69 | '6E' | 10.846 | 479.74 | 'A1' | 11.180 | 492.80 | 'D4' | 11.515 |
| 440.83 | '09' | 10.184 | 453.89 | '3C' | 10.519 | 466.94 | '6F' | 10.853 | 480.00 | 'A2' | 11.187 | 493.06 | 'D5' | 11.521 |
| 441.09 | '0A' | 10.191 | 454.14 | '3D' | 10.525 | 467.20 | '70' | 10.859 | 480.26 | 'A3' | 11.194 | 493.31 | 'D6' | 11.528 |
| 441.34 | '0B' | 10.197 | 454.40 | '3E' | 10.532 | 467.46 | '71' | 10.866 | 480.51 | 'A4' | 11.200 | 493.57 | 'D7' | 11.534 |
| 441.60 | '0C' | 10.204 | 454.66 | '3F' | 10.538 | 467.71 | '72' | 10.872 | 480.77 | 'A5' | 11.207 | 493.82 | 'D8' | 11.541 |
| 441.86 | '0D' | 10.211 | 454.91 | '40' | 10.545 | 467.97 | '73' | 10.879 | 481.02 | 'A6' | 11.213 | 494.08 | 'D9' | 11.547 |
| 442.11 | '0E' | 10.217 | 455.17 | '41' | 10.551 | 468.22 | '74' | 10.886 | 481.28 | 'A7' | 11.220 | 494.34 | 'DA' | 11.554 |
| 442.37 | '0F' | 10.224 | 455.42 | '42' | 10.558 | 468.48 | '75' | 10.892 | 481.54 | 'A8' | 11.226 | 494.59 | 'DB' | 11.561 |
| 442.62 | '10' | 10.230 | 455.68 | '43' | 10.564 | 468.74 | '76' | 10.899 | 481.79 | 'A9' | 11.233 | 494.85 | 'DC' | 11.567 |
| 442.88 | '11' | 10.237 | 455.94 | '44' | 10.571 | 468.99 | '77' | 10.905 | 482.05 | 'AA' | 11.239 | 495.10 | 'DD' | 11.574 |
| 443.14 | '12' | 10.243 | 456.19 | '45' | 10.578 | 469.25 | '78' | 10.912 | 482.30 | 'AB' | 11.246 | 495.36 | 'DE' | 11.580 |
| 443.39 | '13' | 10.250 | 456.45 | '46' | 10.584 | 469.50 | '79' | 10.918 | 482.56 | 'AC' | 11.253 | 495.62 | 'DF' | 11.587 |
| 443.65 | '14' | 10.256 | 456.70 | '47' | 10.591 | 469.76 | '7A' | 10.925 | 482.82 | 'AD' | 11.259 | 495.87 | 'E0' | 11.593 |
| 443.90 | '15' | 10.263 | 456.96 | '48' | 10.597 | 470.02 | '7B' | 10.931 | 483.07 | 'AE' | 11.266 | 496.13 | 'E1' | 11.600 |
| 444.16 | '16' | 10.269 | 457.22 | '49' | 10.604 | 470.27 | '7C' | 10.938 | 483.33 | 'AF' | 11.272 | 496.38 | 'E2' | 11.606 |
| 444.42 | '17' | 10.276 | 457.47 | '4A' | 10.610 | 470.53 | '7D' | 10.945 | 483.58 | 'B0' | 11.279 | 496.64 | 'E3' | 11.613 |
| 444.67 | '18' | 10.283 | 457.73 | '4B' | 10.617 | 470.78 | '7E' | 10.951 | 483.84 | 'B1' | 11.285 | 496.90 | 'E4' | 11.620 |
| 444.93 | '19' | 10.289 | 457.98 | '4C' | 10.623 | 471.04 | '7F' | 10.958 | 484.10 | 'B2' | 11.292 | 497.15 | 'E5' | 11.626 |
| 445.18 | '1A' | 10.296 | 458.24 | '4D' | 10.630 | 471.30 | '80' | 10.964 | 484.35 | 'B3' | 11.298 | 497.41 | 'E6' | 11.633 |
| 445.44 | '1B' | 10.302 | 458.50 | '4E' | 10.636 | 471.55 | '81' | 10.971 | 484.61 | 'B4' | 11.305 | 497.66 | 'E7' | 11.639 |
| 445.70 | '1C' | 10.309 | 458.75 | '4F' | 10.643 | 471.81 | '82' | 10.977 | 484.86 | 'B5' | 11.312 | 497.92 | 'E8' | 11.646 |
| 445.95 | '1D' | 10.315 | 459.01 | '50' | 10.650 | 472.06 | '83' | 10.984 | 485.12 | 'B6' | 11.318 | 498.18 | 'E9' | 11.652 |
| 446.21 | '1E' | 10.322 | 459.26 | '51' | 10.656 | 472.32 | '84' | 10.990 | 485.38 | 'B7' | 11.325 | 498.43 | 'EA' | 11.659 |
| 446.46 | '1F' | 10.328 | 459.52 | '52' | 10.663 | 472.58 | '85' | 10.997 | 485.63 | 'B8' | 11.331 | 498.69 | 'EB' | 11.665 |
| 446.72 | '20' | 10.335 | 459.78 | '53' | 10.669 | 472.83 | '86' | 11.003 | 485.89 | 'B9' | 11.338 | 498.94 | 'EC' | 11.672 |
| 446.98 | '21' | 10.342 | 460.03 | '54' | 10.676 | 473.09 | '87' | 11.010 | 486.14 | 'BA' | 11.344 | 499.20 | 'ED' | 11.679 |
| 447.23 | '22' | 10.348 | 460.29 | '55' | 10.682 | 473.34 | '88' | 11.017 | 486.40 | 'BB' | 11.351 | 499.46 | 'EE' | 11.685 |
| 447.49 | '23' | 10.355 | 460.54 | '56' | 10.689 | 473.60 | '89' | 11.023 | 486.66 | 'BC' | 11.357 | 499.71 | 'EF' | 11.692 |
| 447.74 | '24' | 10.361 | 460.80 | '57' | 10.695 | 473.86 | '8A' | 11.030 | 486.91 | 'BD' | 11.364 | 499.97 | 'F0' | 11.698 |
| 448.00 | '25' | 10.368 | 461.06 | '58' | 10.702 | 474.11 | '8B' | 11.036 | 487.17 | 'BE' | 11.370 | 500.22 | 'F1' | 11.705 |
| 448.26 | '26' | 10.374 | 461.31 | '59' | 10.709 | 474.37 | '8C' | 11.043 | 487.42 | 'BF' | 11.377 | 500.48 | 'F2' | 11.711 |
| 448.51 | '27' | 10.381 | 461.57 | '5A' | 10.715 | 474.62 | '8D' | 11.049 | 487.68 | 'C0' | 11.384 | 500.74 | 'F3' | 11.718 |
| 448.77 | '28' | 10.387 | 461.82 | '5B' | 10.722 | 474.88 | '8E' | 11.056 | 487.94 | 'C1' | 11.390 | 500.99 | 'F4' | 11.724 |
| 449.02 | '29' | 10.394 | 462.08 | '5C' | 10.728 | 475.14 | '8F' | 11.062 | 488.19 | 'C2' | 11.397 | 501.25 | 'F5' | 11.731 |
| 449.28 | '2A' | 10.401 | 462.34 | '5D' | 10.735 | 475.39 | '90' | 11.069 | 488.45 | 'C3' | 11.403 | 501.50 | 'F6' | 11.737 |
| 449.54 | '2B' | 10.407 | 462.59 | '5E' | 10.741 | 475.65 | '91' | 11.076 | 488.70 | 'C4' | 11.410 | 501.76 | 'F7' | 11.744 |
| 449.79 | '2C' | 10.414 | 462.85 | '5F' | 10.748 | 475.90 | '92' | 11.082 | 488.96 | 'C5' | 11.416 | 502.02 | 'F8' | 11.751 |
| 450.05 | '2D' | 10.420 | 463.10 | '60' | 10.754 | 476.16 | '93' | 11.089 | 489.22 | 'C6' | 11.423 | 502.27 | 'F9' | 11.757 |
| 450.30 | '2E' | 10.427 | 463.36 | '61' | 10.761 | 476.42 | '94' | 11.095 | 489.47 | 'C7' | 11.429 | 502.53 | 'FA' | 11.764 |
| 450.56 | '2F' | 10.433 | 463.62 | '62' | 10.768 | 476.67 | '95' | 11.102 | 489.73 | 'C8' | 11.436 | 502.78 | 'FB' | 11.770 |
| 450.82 | '30' | 10.440 | 463.87 | '63' | 10.774 | 476.93 | '96' | 11.108 | 489.98 | 'C9' | 11.443 | 503.04 | 'FC' | 11.777 |
| 451.07 | '31' | 10.446 | 464.13 | '64' | 10.781 | 477.18 | '97' | 11.115 | 490.24 | 'CA' | 11.449 | 503.30 | 'FD' | 11.783 |
| 451.33 | '32' | 10.453 | 464.38 | '65' | 10.787 | 477.44 | '98' | 11.121 | 490.50 | 'CB' | 11.456 | 503.55 | 'FE' | 11.790 |




L1 = 3122 138 2021/TOKO 85 ACS-4238 A
L2 = 3122 138 2022/TOKO 85 ACS-4260 SEJ

Fig. 6 MUSTI test and application circuit.
Germanium diodes AA119 are required in the test circuit only.
In a complete FM channel (inclusive FM front end) the silicon diodes BA281 are recommended.

S open = without muting
S closed = with muting } for measuring purpose only.

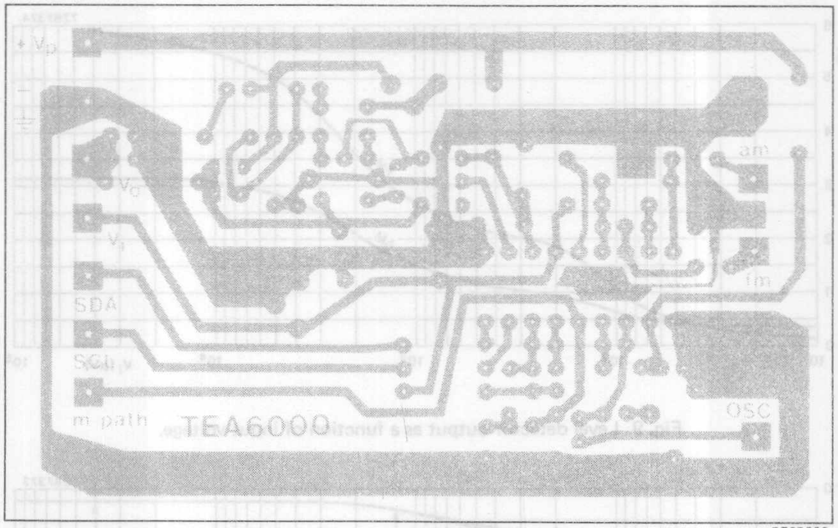



Fig. 7 Track side of printed-circuit board.

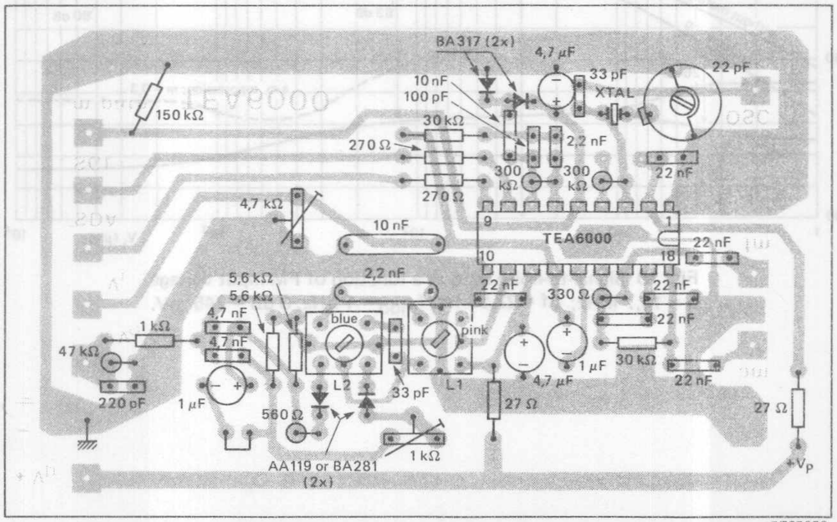



Fig. 8 Component side of printed-circuit board.

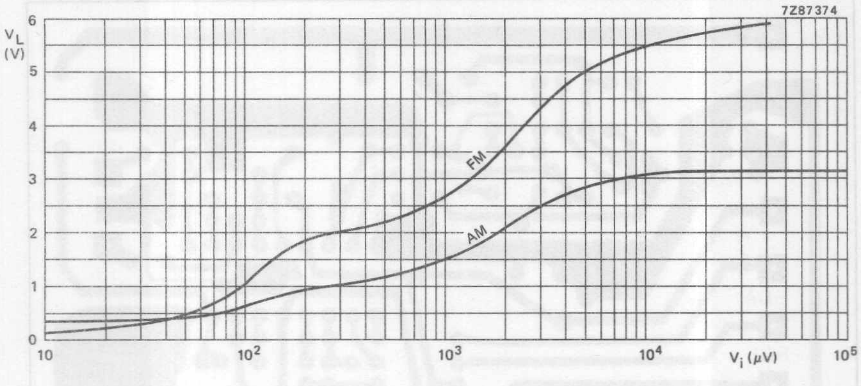



Fig. 9 Level detector output as a function of input voltage.

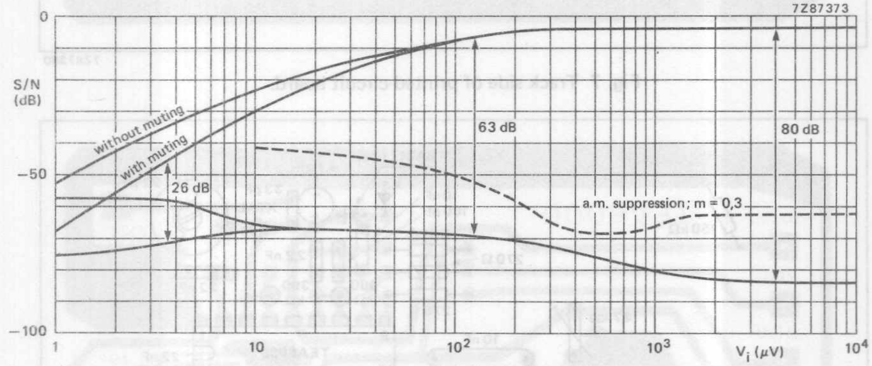
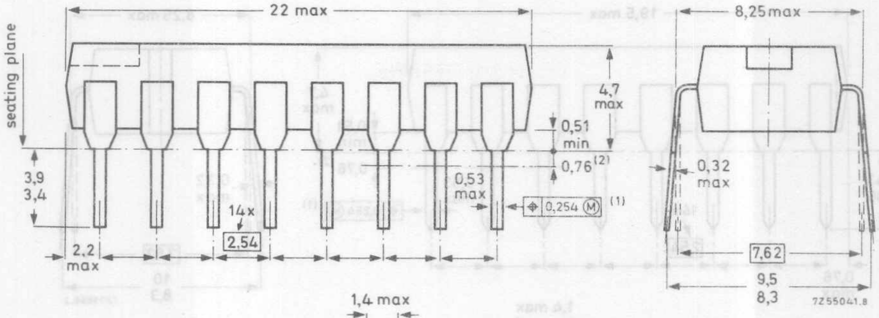


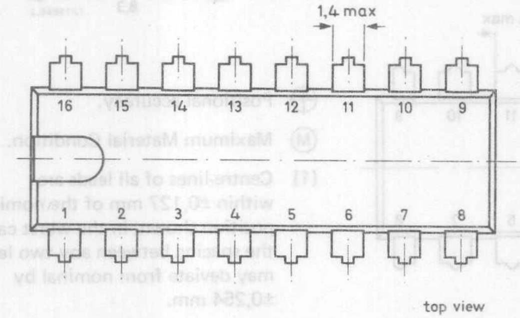

Fig. 10 Signal-to-noise ratio as a function of FM input voltage.
$f_i$ = 10,7 MHz; $\Delta f$ = 22,5 kHz; $f_{mod}$ = 1 kHz; 0 dB = 245 mV.

Purchase of Philips' $I^2C$ components conveys a license under the Philips' $I^2C$ patent to use the components in the $I^2C$-system provided the system conforms to the $I^2C$ specifications defined by Philips.

PACKAGE OUTLINES

## 16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

### SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

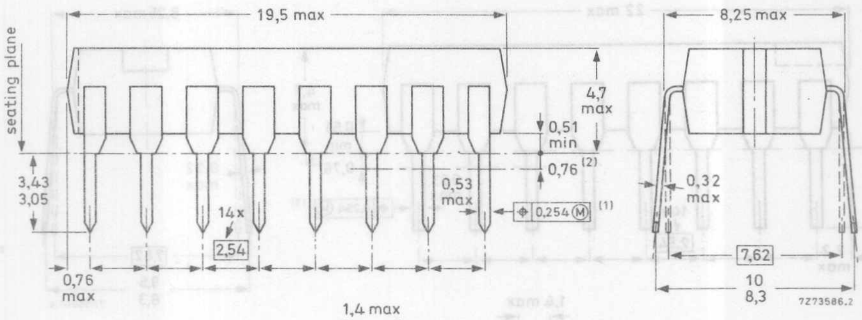
**2. By dip or wave**

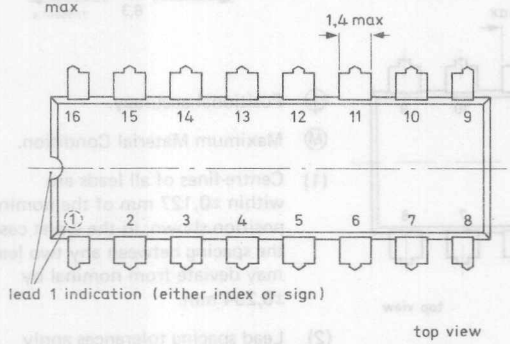
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

## 16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

### SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

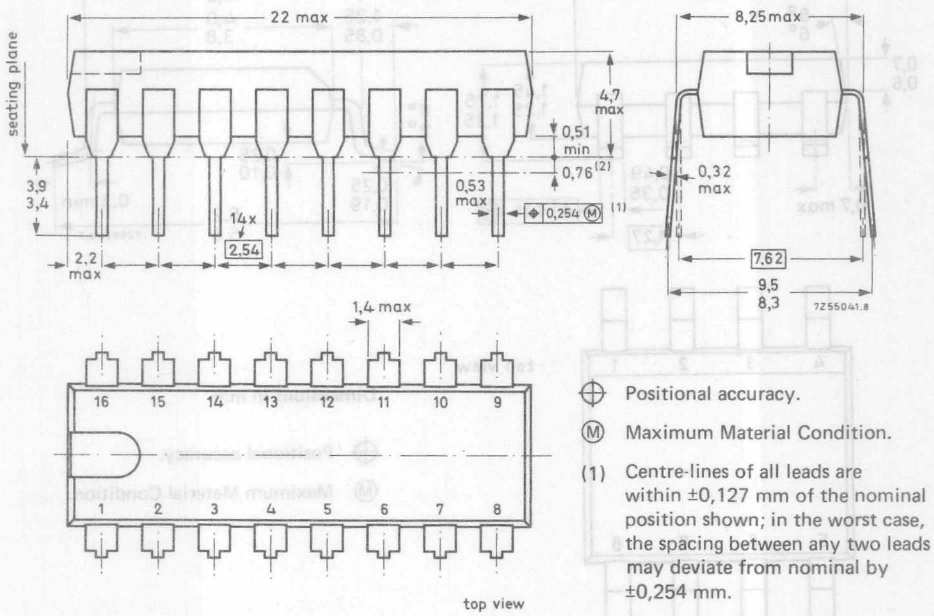
**2. By dip or wave**

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

# 16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT-38WE-2)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

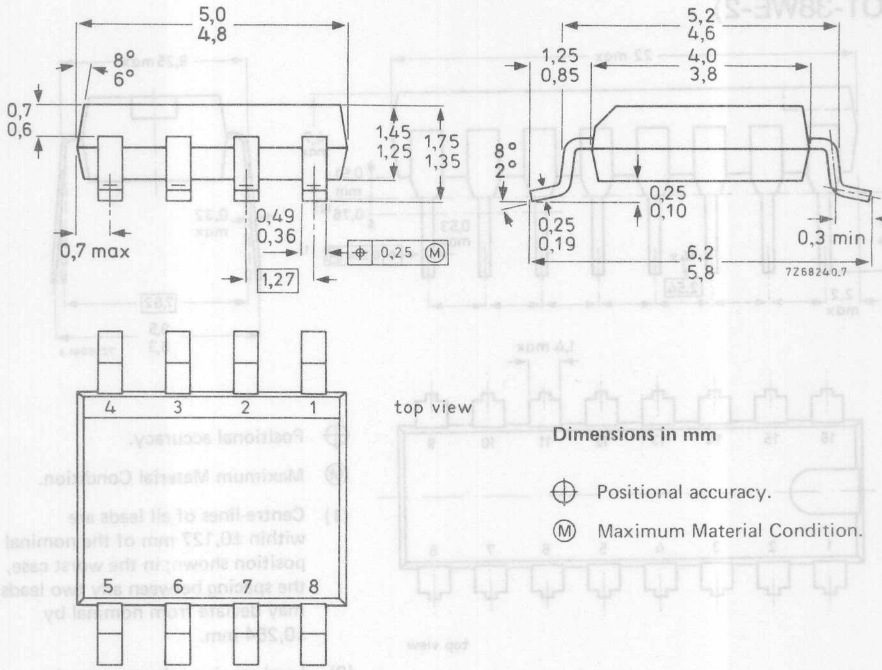
**2. By dip or wave**

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

# 8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)




## SOLDERING

**The reflow solder technique**

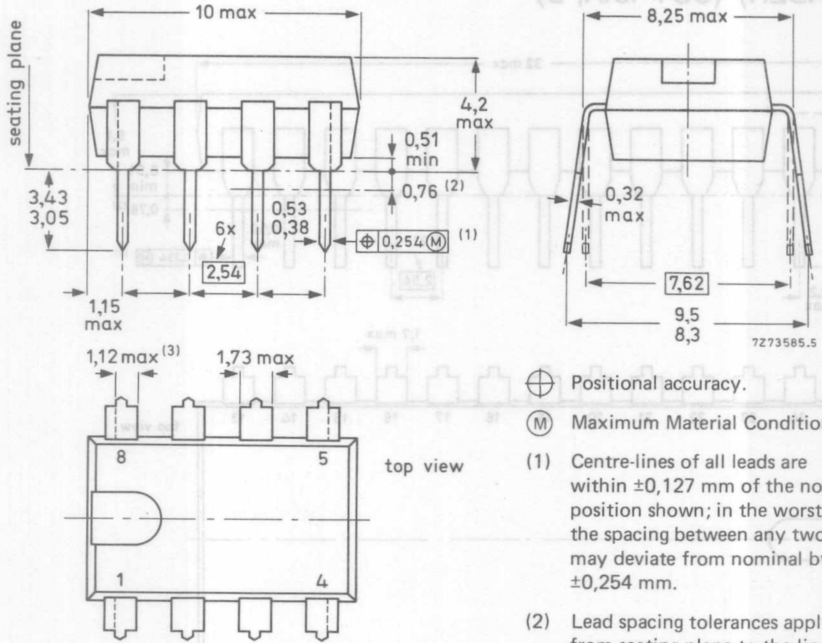
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 $\mu$m is used for which the emulsion thickness should be about 50 $\mu$m. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

## 8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

**Dimensions in mm**

### SOLDERING

**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

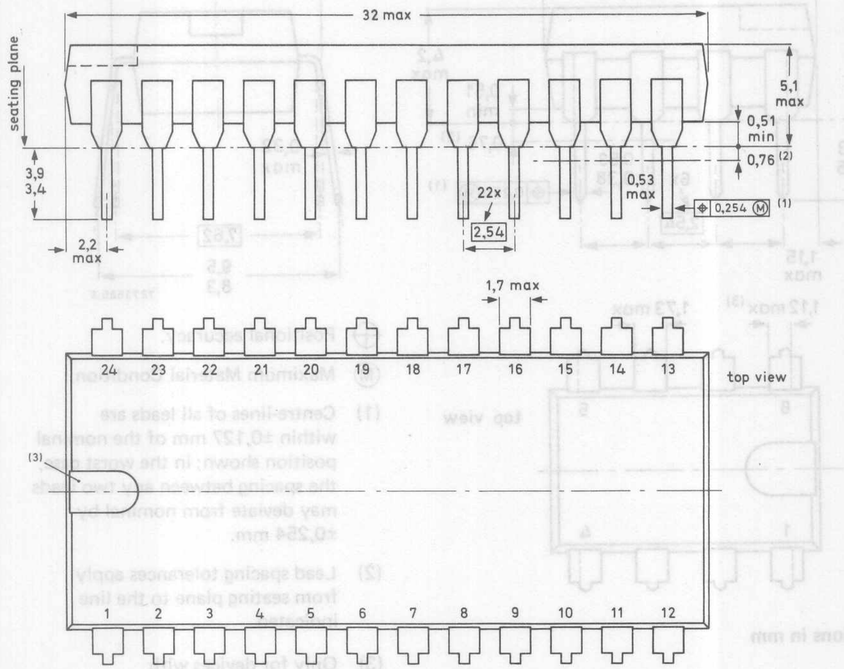
**2. By dip or wave**

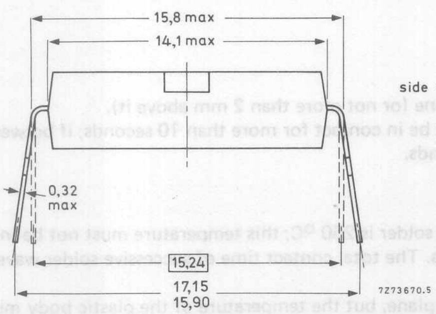
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.

# 24-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-101A, B)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

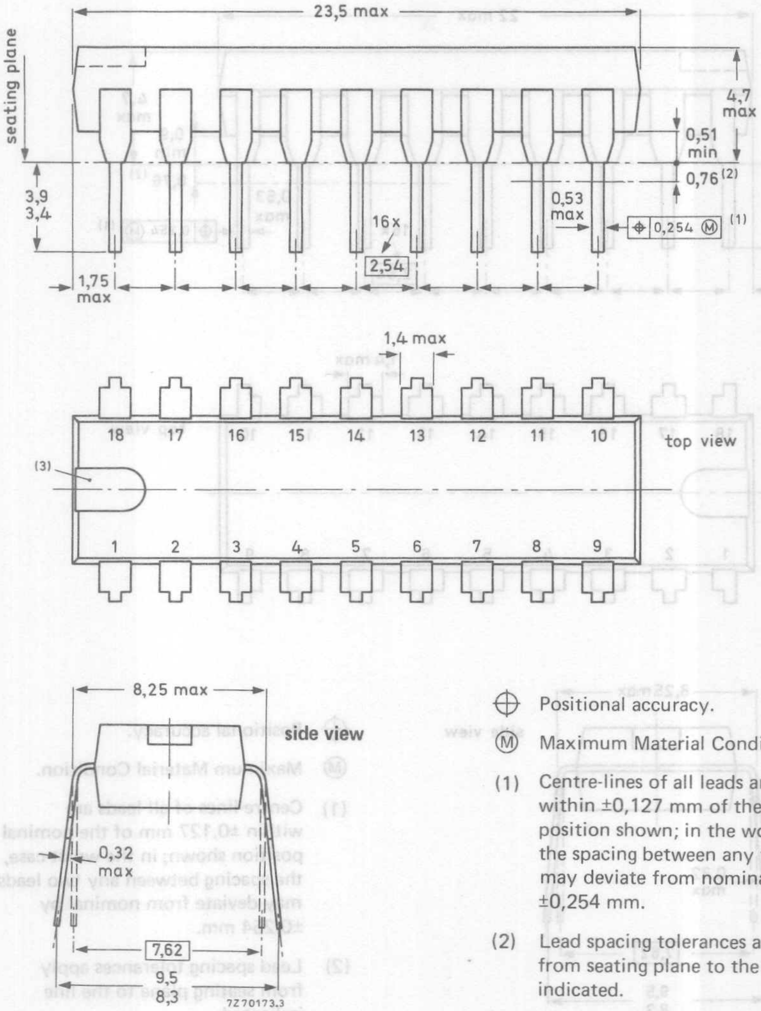
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

## 18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

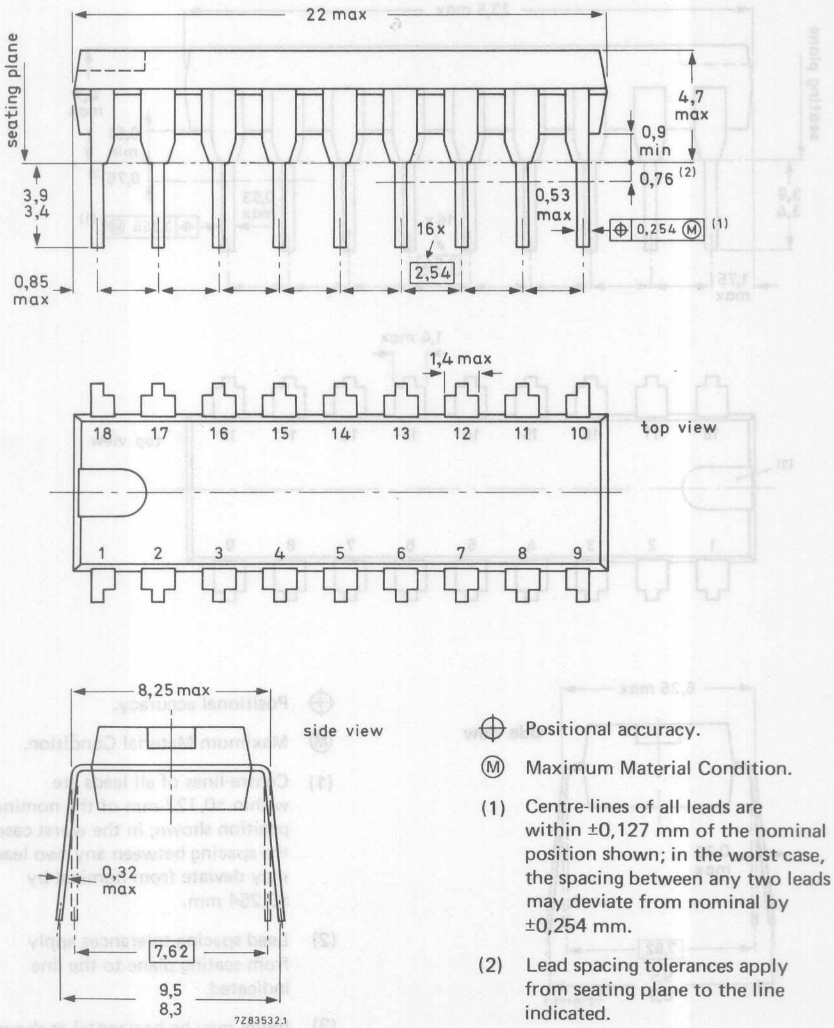
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

## 18-LEAD DUAL IN-LINE; PLASTIC(SOT-102CS,HE,KE)




⊕ Positional accuracy.

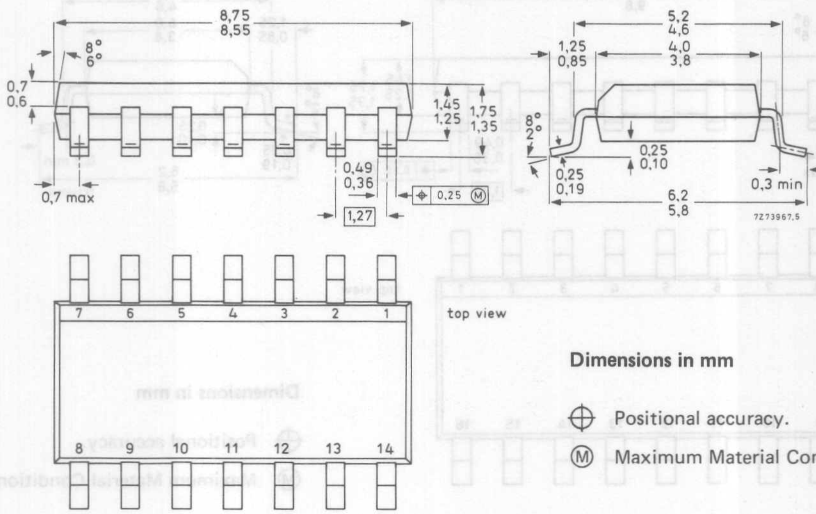
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

# 14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

**The reflow solder technique**

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

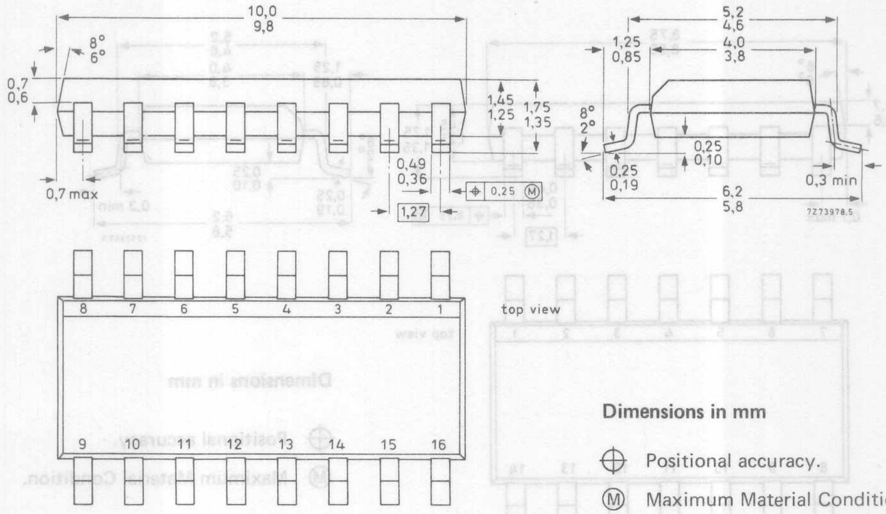
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 $\mu$m is used for which the emulsion thickness should be about 50 $\mu$m. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.

After soldering, the substrate must be cleaned of any remaining flux.

## 16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

### SOLDERING

#### The reflow solder technique

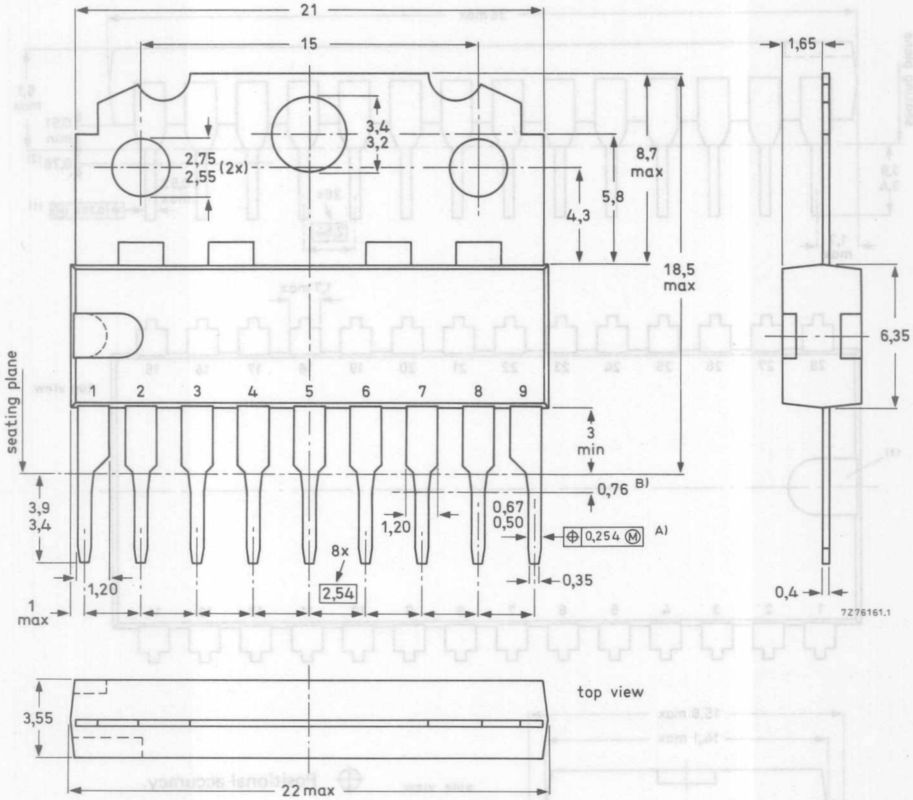
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

# 9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)




**Dimensions in mm**

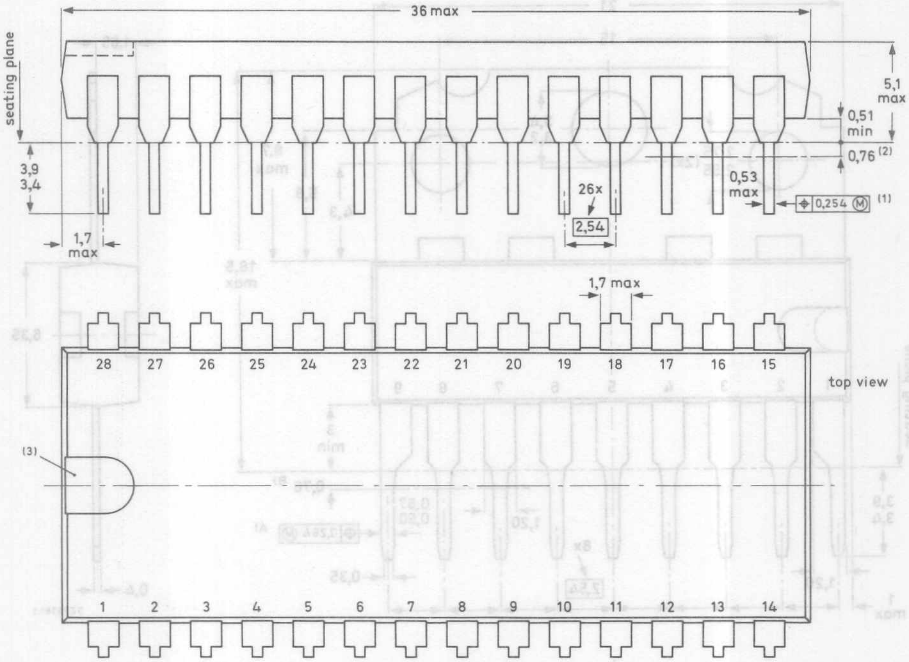
⊕ Positional accuracy.

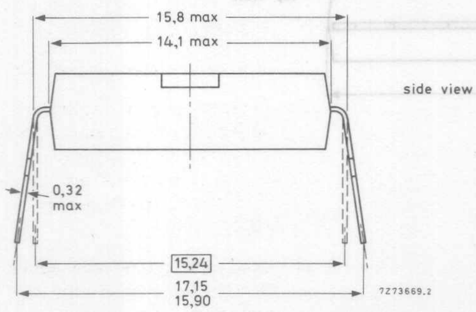
Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

# 28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

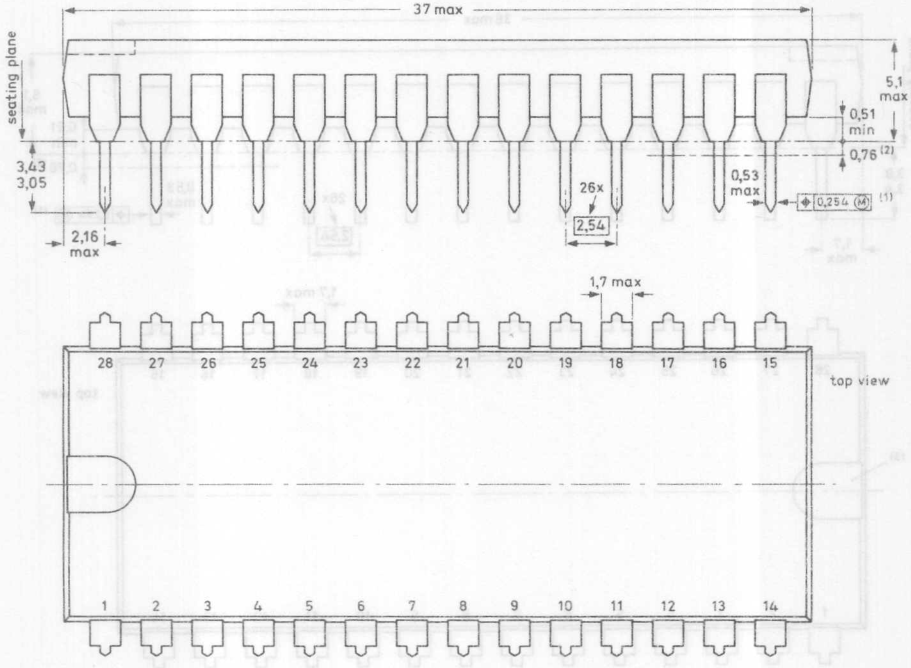
(2) Lead spacing tolerances apply from seating plane to the line indicated.

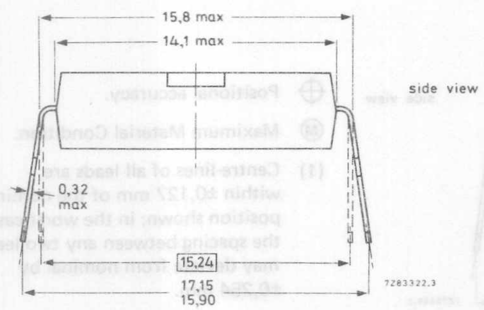
(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

**SOLDERING** see SOT-38

# 28-LEAD DUAL IN-LINE; PLASTIC (SOT-117A,D)




⊕ Positional accuracy.

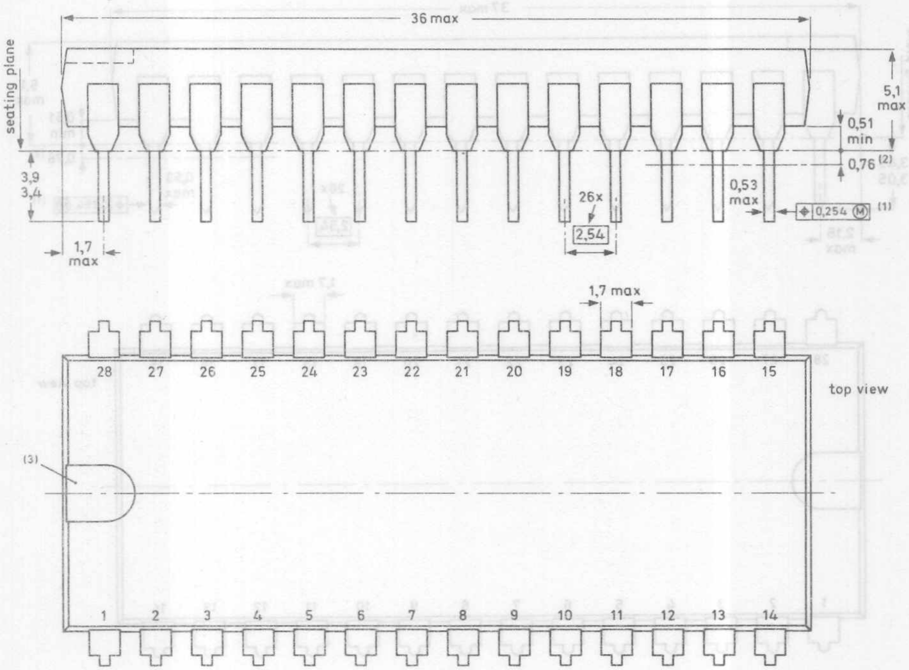
Ⓜ Maximum Material Condition.

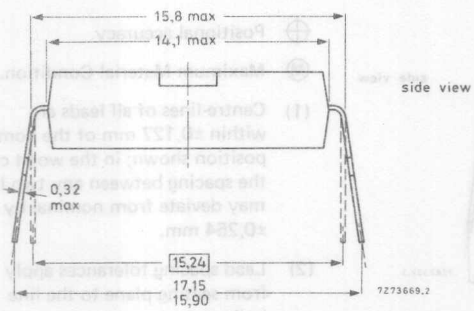
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## 28-LEAD DUAL IN-LINE; PLASTIC (SOT-117BE)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

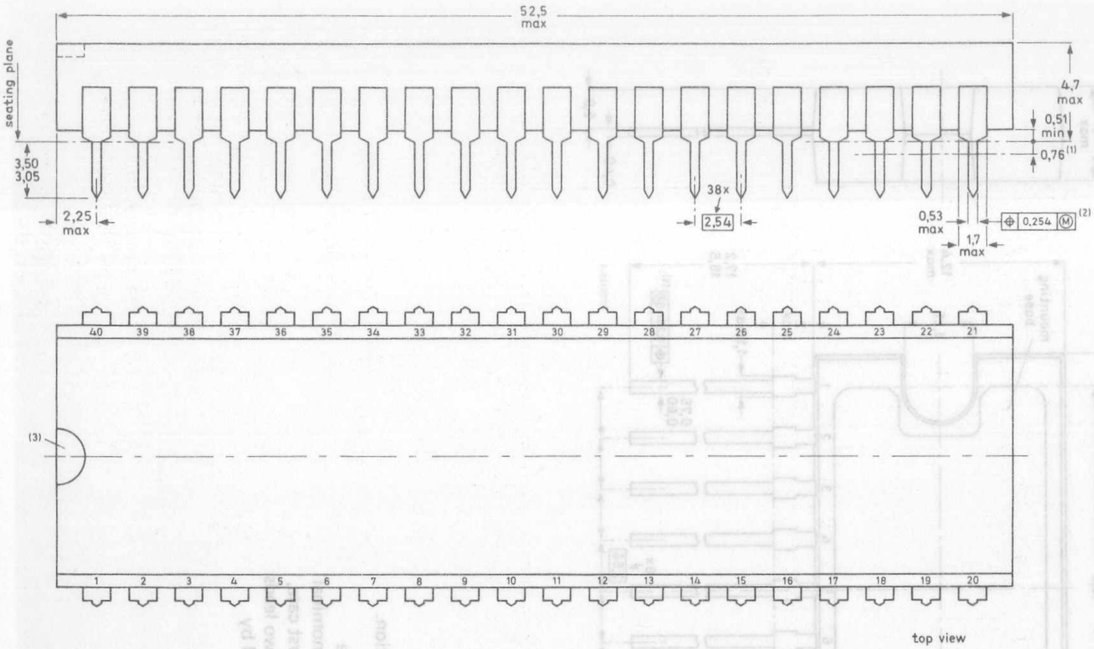
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

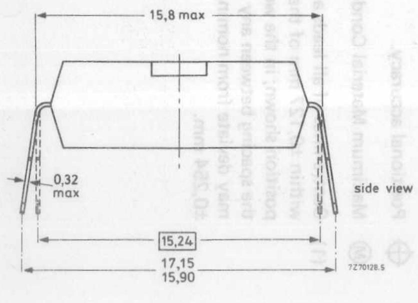
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

# 40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)




⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

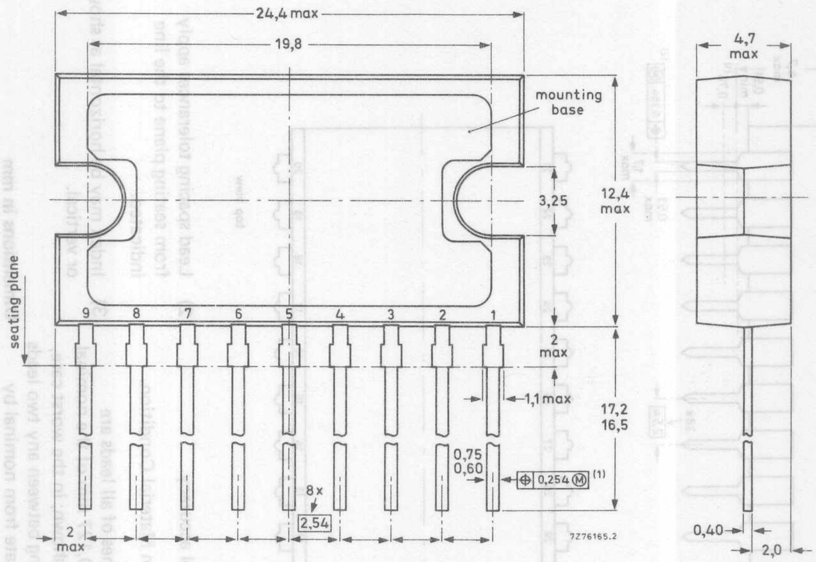
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

# 9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)



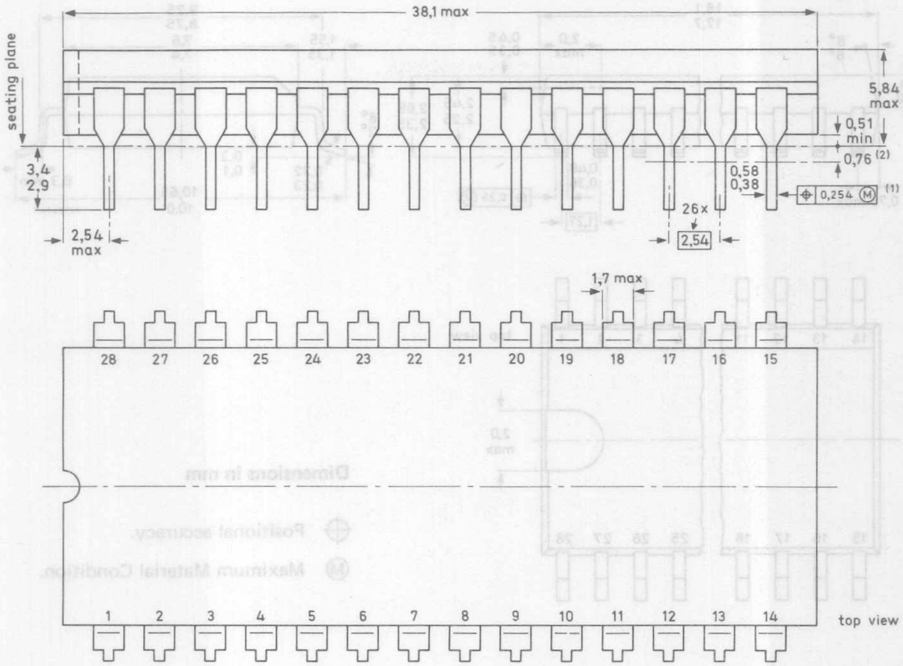

**Dimensions in mm**

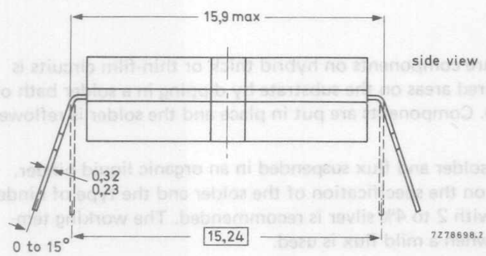
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

## 28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)




⊕ Positional accuracy.

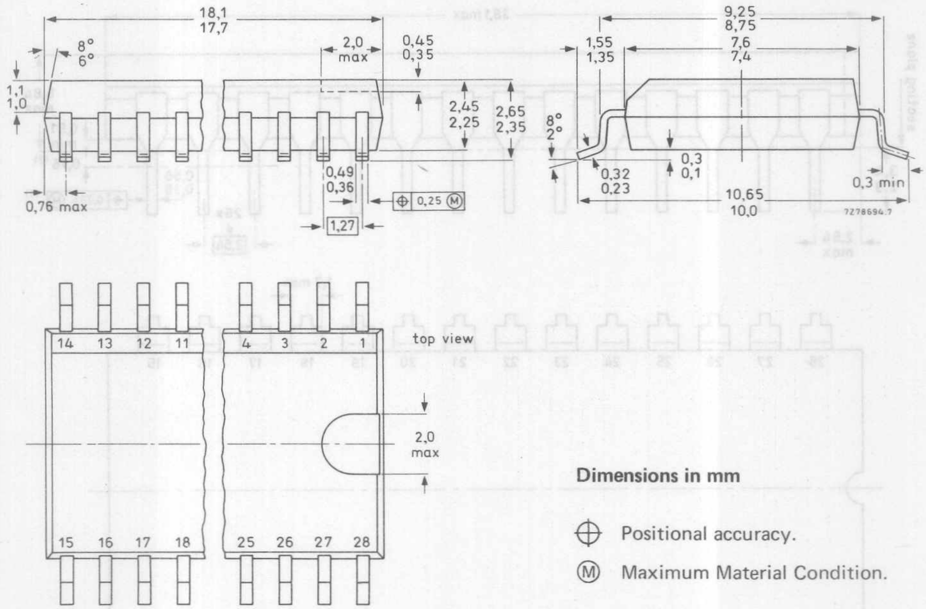
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

# 28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

### The reflow solder technique

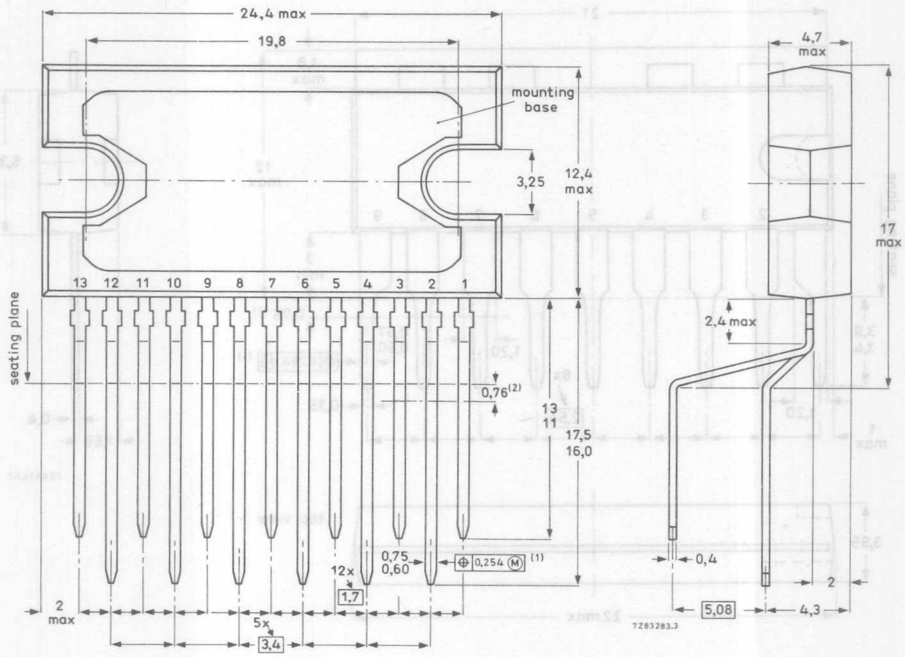
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 $\mu$m is used for which the emulsion thickness should be about 50 $\mu$m. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

# 13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)




**Dimensions in mm**

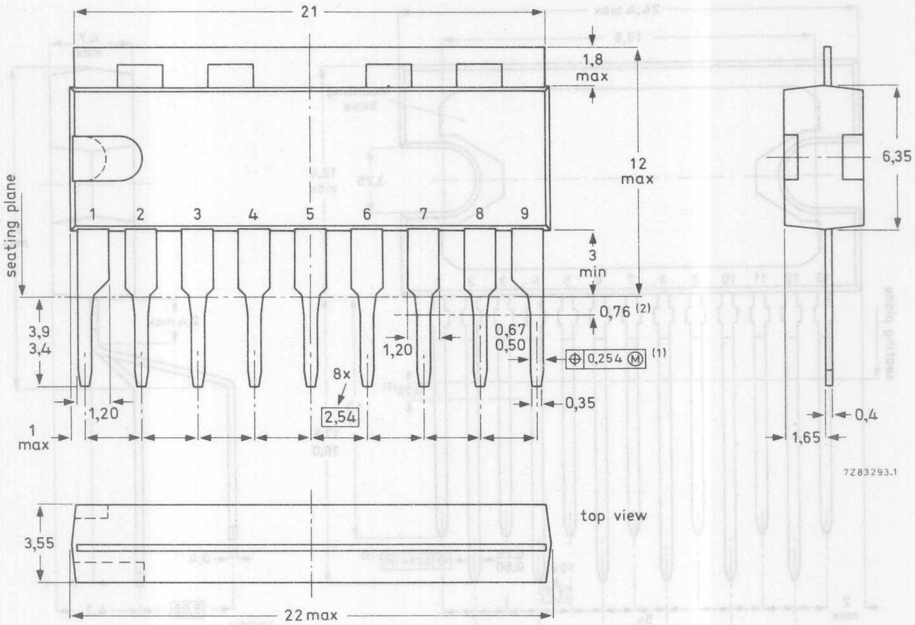
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

## 9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)




**Dimensions in mm**

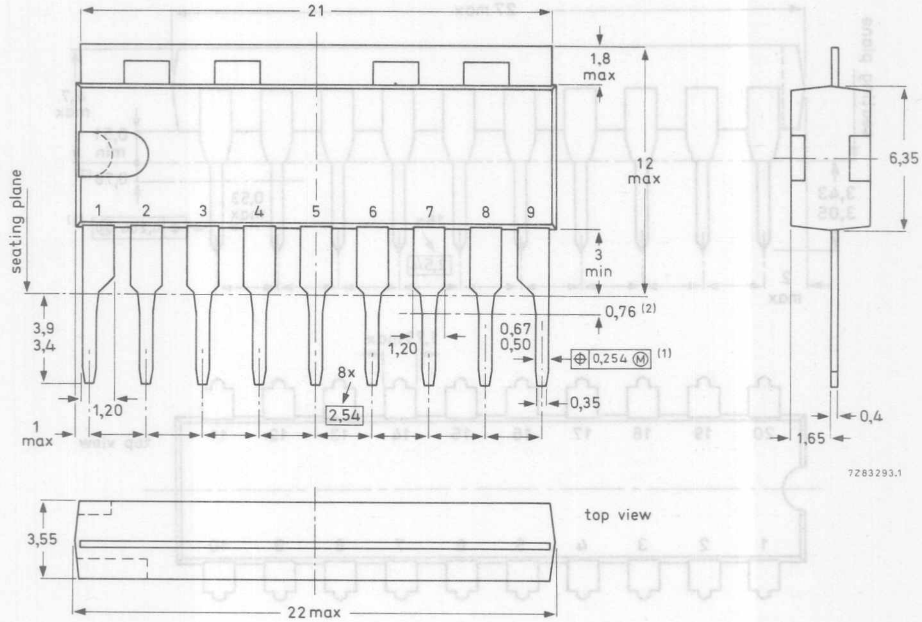
⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

# 9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142B)




**Dimensions in mm**

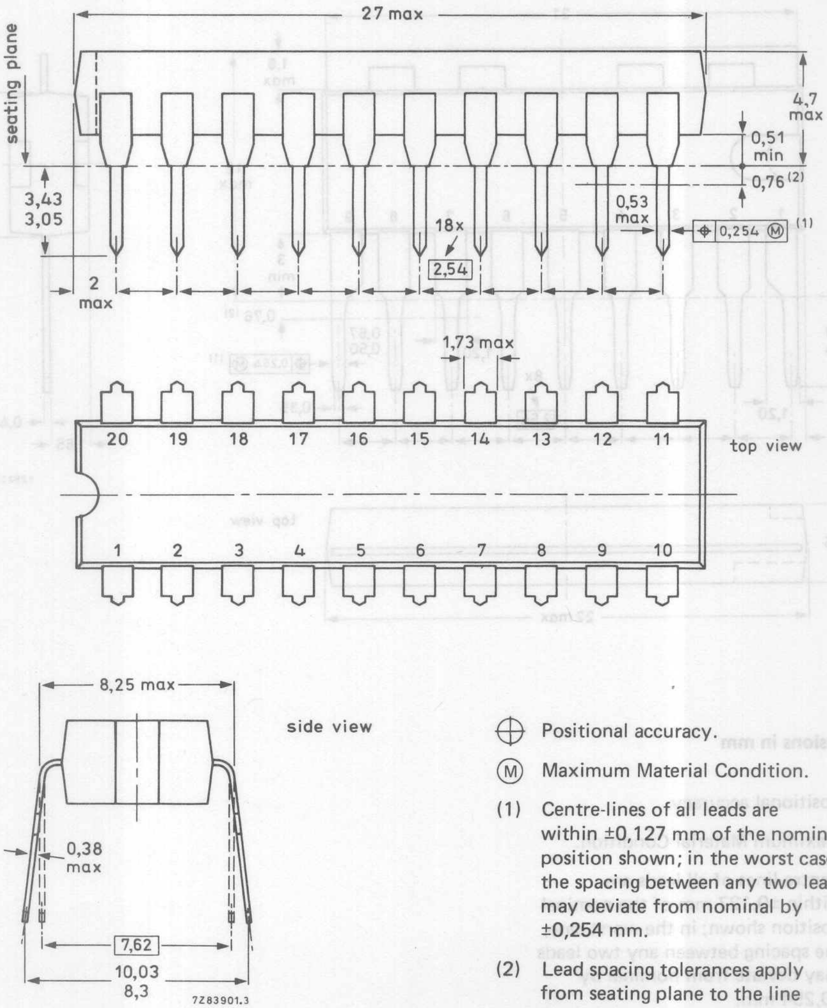
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

# 20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)




⊕ Positional accuracy.

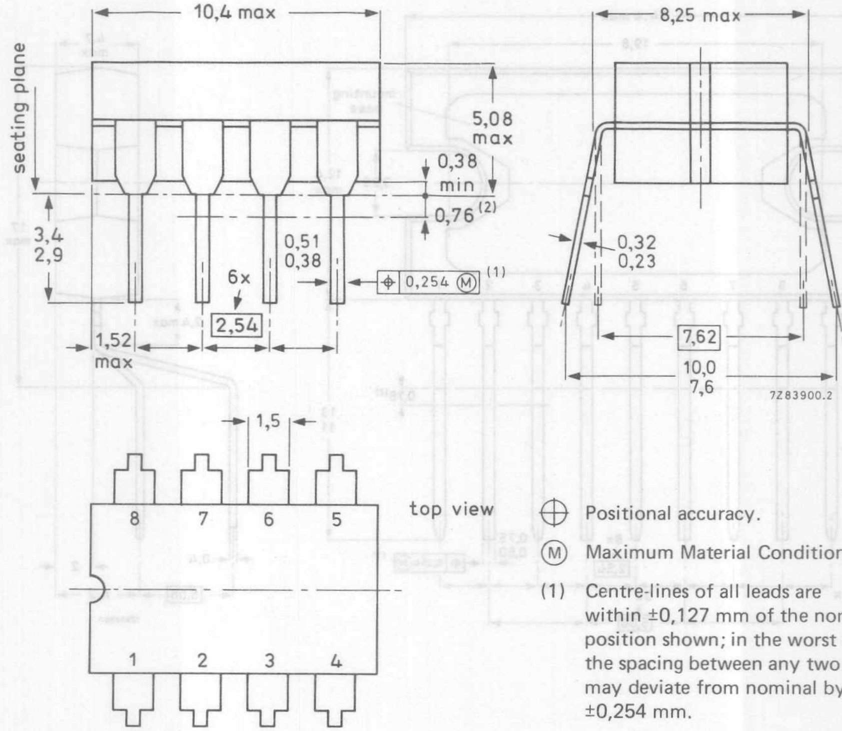
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## 8-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-151A)




⊕ Positional accuracy.

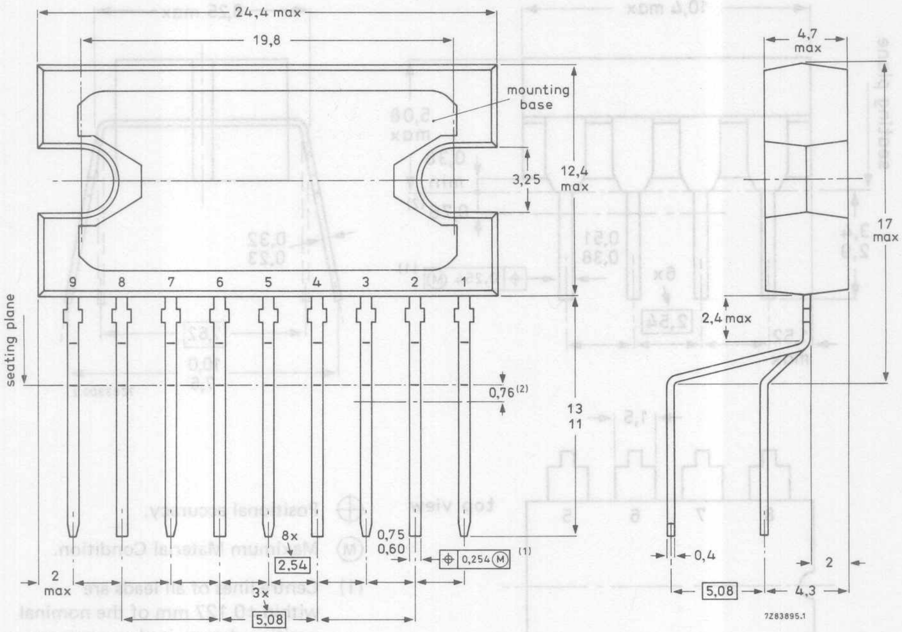
(M) Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

# 9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157A,B)




**Dimensions in mm**

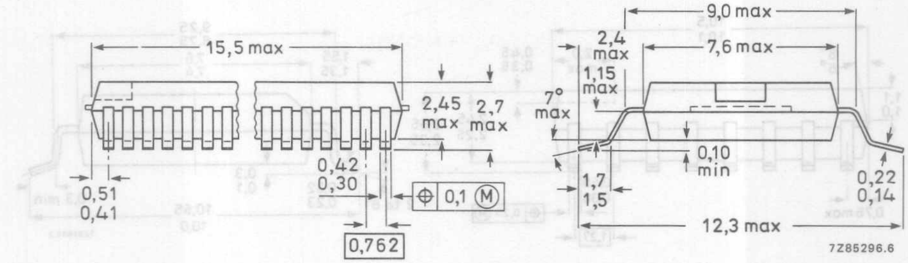
⨁ Positional accuracy.

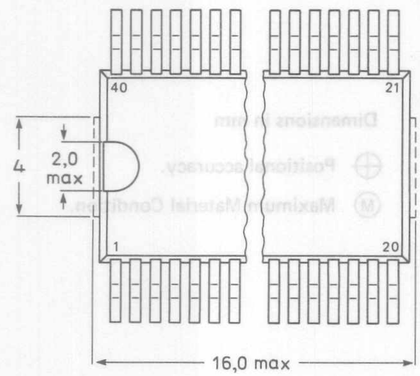
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

# 40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)




top view

**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

### The reflow solder technique

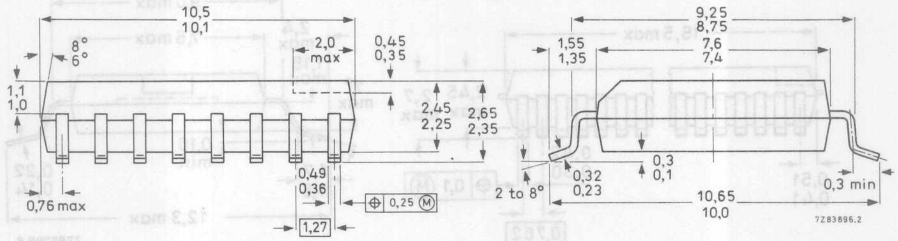
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

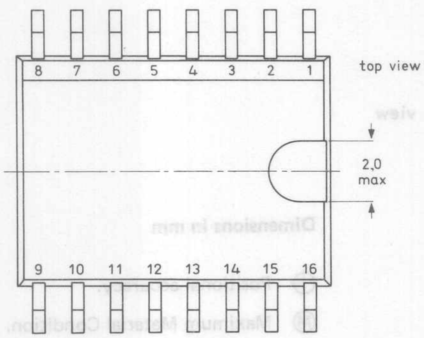
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 $^{o}$C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 $\mu$m is used for which the emulsion thickness should be about 50 $\mu$m. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

## 16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

### SOLDERING

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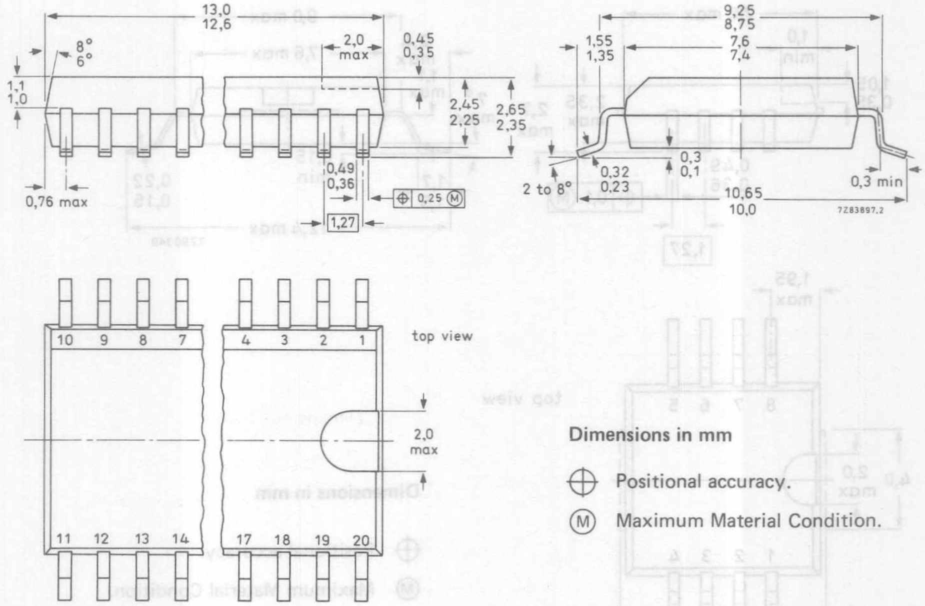
# 20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

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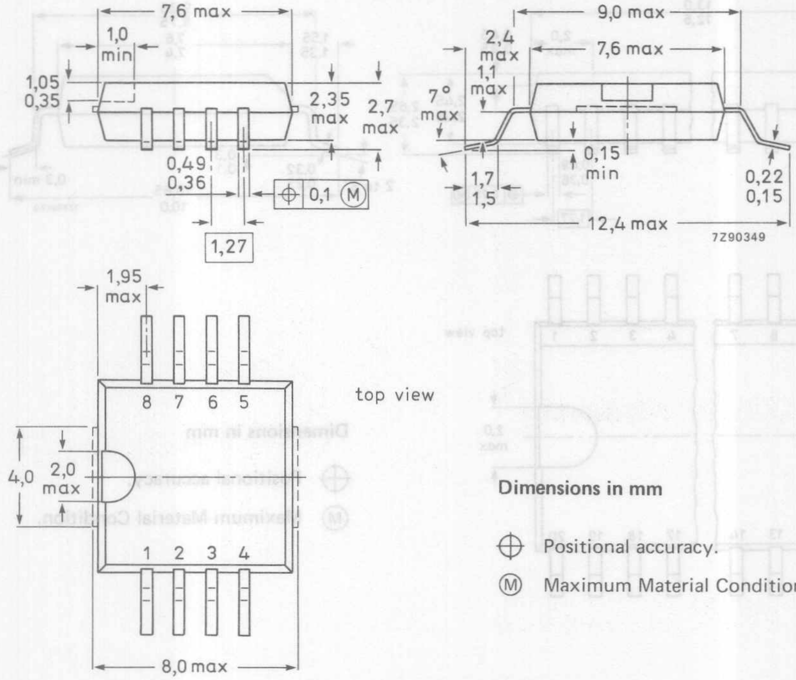
After soldering, the substrate must be cleaned of any remaining flux.

# 8-LEAD MINI-PACK; PLASTIC (VSO-8; SOT-176)




Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

### The reflow solder technique

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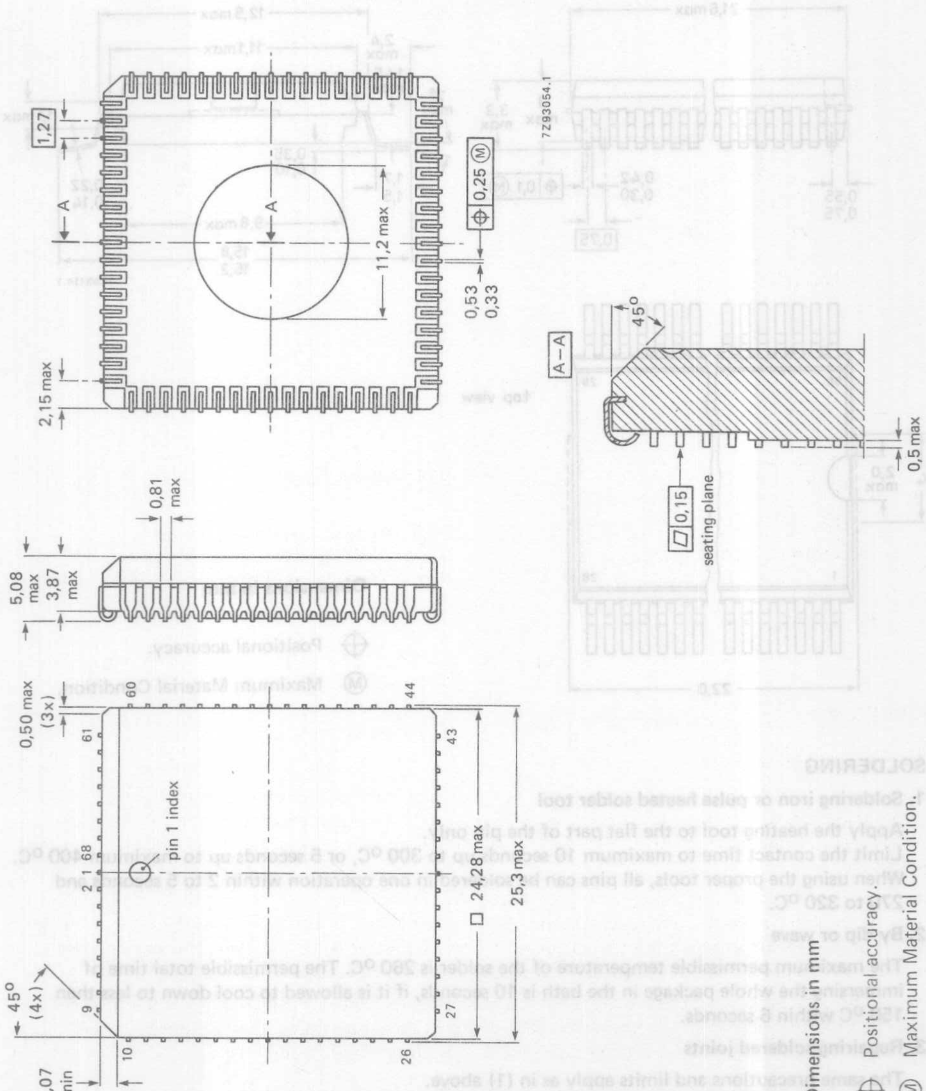
After soldering, the substrate must be cleaned of any remaining flux.

## 68-LEAD PLASTIC LEADED-CHIP-CARRIER (PLCC); SOT-188A

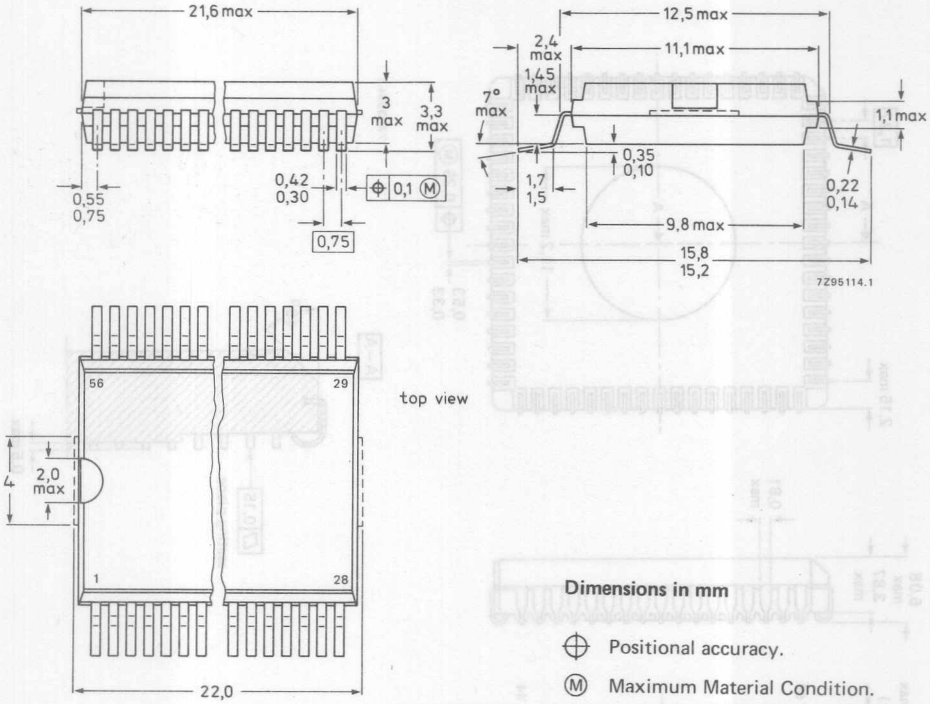



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

# 56-LEAD MINI-PACK; PLASTIC (VSO-56; SOT-190)




**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

**1. Soldering iron or pulse heated solder tool**

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, all pins can be soldered in one operation within 2 to 5 seconds and 270 to 320 °C.

**2. By dip or wave**

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

**3. Repairing soldered joints**

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.